TileCal High Voltage System LIP - Summer Student Program 2020

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ATLAS Group



LABORATÓRIO DE INSTRUMENTAÇÃO E FÍSICA EXPERIMENTAL DE PARTICULAS



ATLAS Group

Outline

- TileCal Structure and Electronics;
- New HL-LHC Upgrade;
- HV Working Scheme;
- Goal of this Work
- Set Up;
- Data Aquisition;
- Analysis Algorithm;
- Results;
- Further Steps;

ATLAS - TileCal - Hadronic Calorimeter



 TileCal is an hadronic calorimeter inside ATLAS. Helena Santos begun her mission, as run coordinator of TileCal, last week.

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TileCal Stucture and Electronics



Figure 1: Mechanical structure and electronic boards inside TileCal.

- Almost 10000 photomultipliers ⇒ HV supply!
- Electronics implemented in the 90's, mostly inside the detector, designed to last for 10 years.
- Already acomplished 20 years of radiation exposure!

New HL-LHC Upgrade

- Development of **new system** that manages **High Luminosity** from LHC upgrade.
- HV electronics moved to cavern USA15 far away from radiation exposure.
- New 100 *m* cables guide HV from cavern to detector.
- New HV supplies & regulator boards, with 48 channels, developed and tested at LIP!



Figure 2: USA15 cavern, new HV regulator board and 100 m cable model.

- New **HV regulation boards (HVremote)** provides 48 individual voltages for PMT's.
- Each HVremote board has input of 2 primary HVin (800 950) V privided by an HVsupply board.
- **HVremote** regulates each channel **voltage in range** [HVin-360; HVin].
- DACs are used to control the individual voltages of each channel.
- 1 ADC is used to read back the voltages of all the 48 channels
- Selection of channel via MUX.

Voltage Calibration!

- To allow precise voltage setting and reading, the **mappings DAC vs ChVoltage** and **ADC vs ChVoltage** are needed for **all channels**.
- Voltmeter used to read voltage, connected to a PC through GPIB.
- DAC control and ADC readings via Raspberry Pi.
- Offline synchronization of data required!

Set Up



Figure 3: Our set-up at LIP-FCUL.

- 2 HV generators supply each side of the board (2×24 channels).
- 1 RaspberryPi manages readout, stability control and calibration software.
- 1 RaspberryPi dedicated to temperature measurements.
- 1 Voltmeter comunicates with a PC running LabView to readout channel HV output.

Data Aquisition

- 4 main runs for each channel, with different sets of parameters.
- DAC value vary acordingly to HVin, on a specific channel. Other DAC kept "static", in most of the runs.
- Board's HVin is set to 560 V (DAC vary from 800 to 2300), 800 V (DAC vary from 1900 to 3400) and 960 V (DAC vary from 2500 to 4000).
- 2 runs with Other DAC fixed at 2100 (wich corresponds to a certain HV in those channels) for HVin = 560 and 800 V.
- 2 runs with Other DAC at 3100 for HVin = 800 and 960 V.
- The software on Pi, **iterates DAC value**, with step 50, holding each iteration enough to stabilize.

ADC "Stair" Pattern



Figure 4: DAC iterations pattern over one run.

• Using **Begin Run Time** and **End Run Time** from logbook (acording to Pi's clock), events are **indexed in seconds**, since midnight.

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HVoutput Plot



Figure 5: HVouput, from LabView, of several runs.

- Using **Begin Run Time** and **End Run Time** from logbook (acording to Windows' clock), events are **indexed in seconds**, since midnight.
- User must **identify the corresponding run** and insert, in the software, begin run time acording to Windows (LabView).
- ADC and channel HVout events get sincronized!

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HVout "Stair" Pattern - Run Selected



Figure 6: Corresponding HVout selected within the same time frame as ADC.

- As it shoud be, the same pattern of ADC appears within the same period.
- The algorithm calculates average and rms values for each "step".

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Figure 7: Calibration plot.

- Resulting plot of **HVout vs ADC** averages in each iteration.
- Linear regression parameters calibrate channel output acording to ADC suply, in a range, while other channels are kept at a certain mean value.

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Table 1: Calibration table of channel 38 with HVin from 560 to 960 V.

Channel	HVin [V]	Other DAC	Slope [V]	Intercept [V]	r ²
38	960	3100	0.2421	4.318 ± 0.008	0.9999
38	800	3100	0.2422	4.147 ± 0.007	0.9999
38	800	2100	0.2422	3.964 ± 0.006	0.9999
38	560	2100	0.2423	3.803 ± 0.003	0.9999

- Aquiered data to calibrate 25 channels.
- 16 already analysed!

Channel 8 "Fried"



Figure 8: Channel 8 at 560 V.

• Even so: slope = 0.2428 V || $r^2 = 0.9999$

Image: Image:

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100 m Cable Effect



Figure 9: Channel 28 at 800 V.

• With Cable (and PMT as load):

slope = 0.2429 V $r^2 = 0.9999$ • No Cable (only PMT divider as load):

slope =
$$0.2429 V$$

 $r^2 = 0.9999$

- Considering fit interceptions, compile DAC 2100 and DAC 3100 fits.
- Extrapolate final calibration line for each channel.
- A channel voltage is slightly affected by the voltages applied to otherchannels.
- Compute dependency on other channels average voltage.



Figure 10: Full range channel calibration.

Further Steps

- Enhance analysis software, including DAC vs HVout and DAC vs ADC study.
- Fullfill the channel calibration table!

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Figure 11: Channel calibration table.

Wake Up the board!



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