The Readout Electronics of The Mu2e Electromagnetic Calorimeter

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INFN – Sezione di Pisa

22nd edition
PANIC Lisbon Portugal
Particles and Nuclei International Conference

Outline

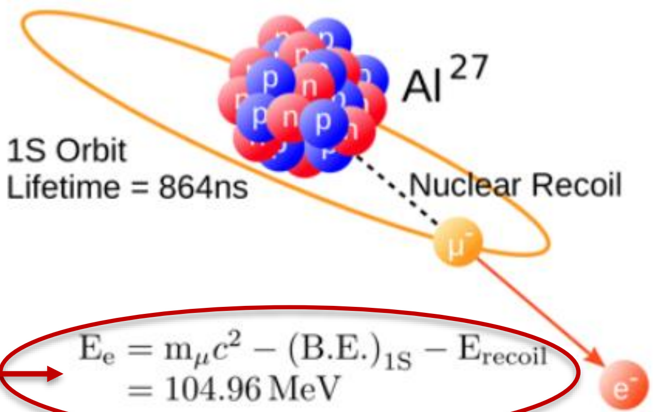
- The Mu2E experiment: goal and experiment layout
- The Electromagnetic Calorimeter
- Calorimeter electronics scheme
- Which requirements?
- Front End electronics
- Mezzanine Board
- Digitizer spec, architecture and design
- Qualification tests
- Vertical Slice Test

The Mu2e Experiment

- Mu2e searches for Charged Lepton Flavor Violation (CLFV) via the coherent conversion:

$$\mu^- \mathrm{N} \rightarrow e^- \mathrm{N}$$

at Fermilab muon campus..



Clear experimental signature!

$$\mathrm{E_e} = \mathrm{m}_\mu c^2 - (\mathrm{B.E.})_{1S} - \mathrm{E_{recoil}} = 104.96\,\mathrm{MeV}$$

- Since the Standard Model prediction is ~ $(\Delta m_\nu^2 / M_W^2)^2 < 10^{-54}$, far beyond experimental reach, any observation will be clear evidence for New Physics.

- In case of no observations, Mu2e will improve by a factor 10^4 the current world best limit from Sindrum II experiment:

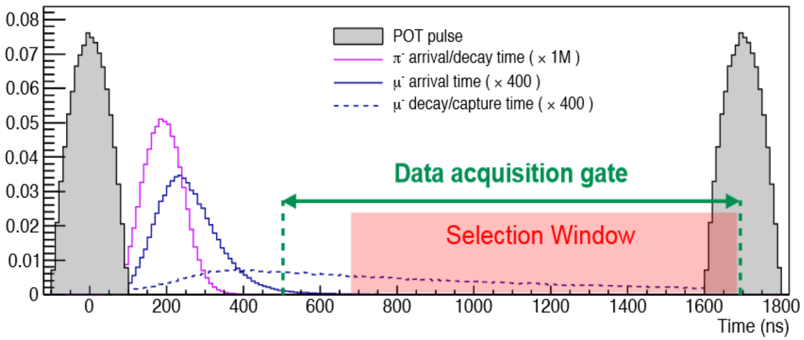
$$R_{\mu e} = \frac{\Gamma(\mu^- + \mathrm{N(A,Z)}) \rightarrow e^- + \mathrm{N(A,Z)}}{\Gamma(\mu^- + \mathrm{N(A,Z)}) \rightarrow \text{all muon captures})} \leq 8\times 10^{-17} \text{ @ } 90\% \text{ C.L.}$$

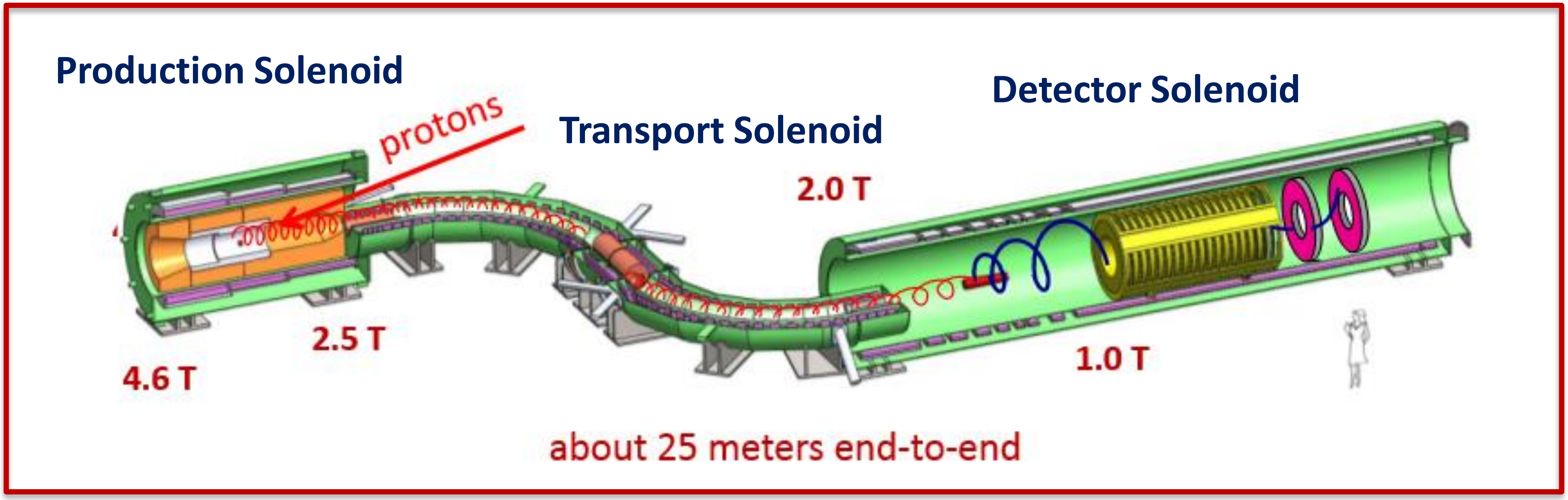
Mu2e Technique

1. Generate a beam of low momentum muons
   - High intensity, high purity, pulsed
2. Transport and stop the muons in aluminum target
   - Muonic Atom mean life: **τ_μ^A = 864 ns**
3. Look for events consistent with a conversion electron:
   - In case of aluminum: **E_{CE} = 104.96 MeV**
   - Signal windows of few hundreds of keV below E_{CE}

Pulsed beam and a delayed live gate:

Beam Period: 1700 ns ~ 2 x τ_μ^{Al}
Beam Intensity: 40 Mp/bunch

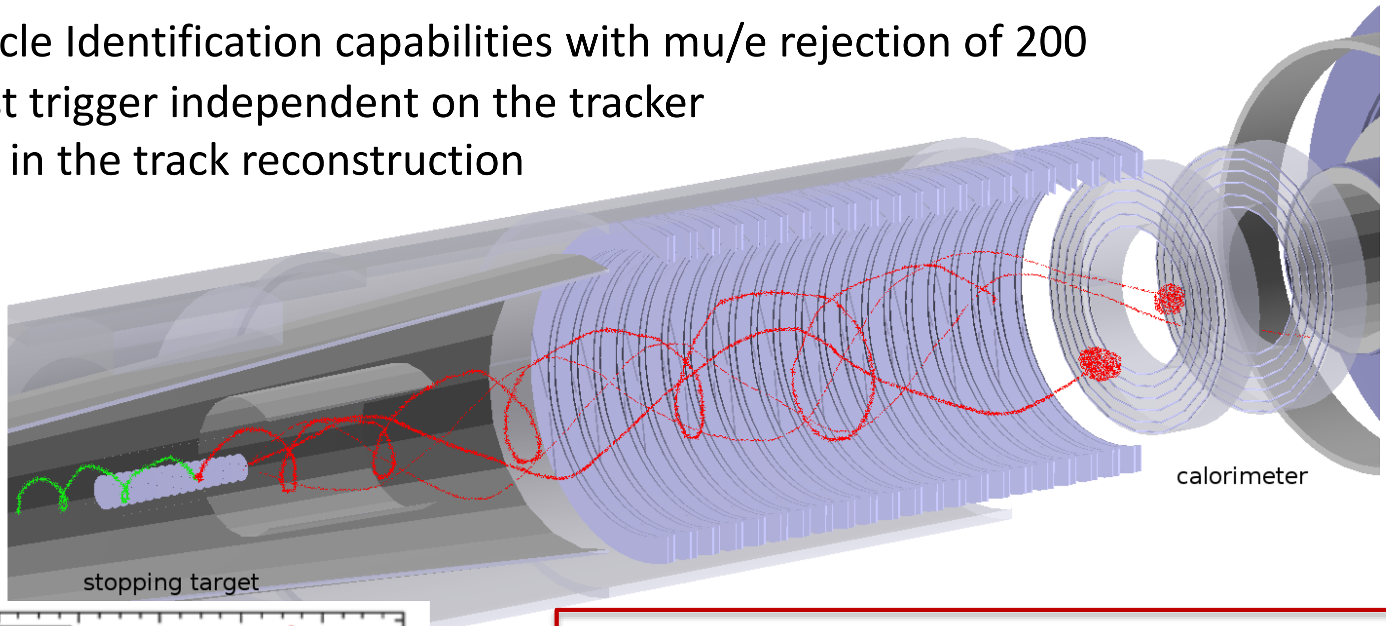


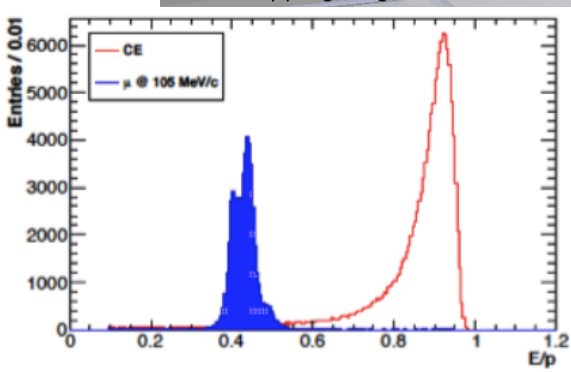


Calorimeter Requirements

For the muon to electron conversion search, the calorimeter has to add redundancy and complementary measures with respect to the tracker:

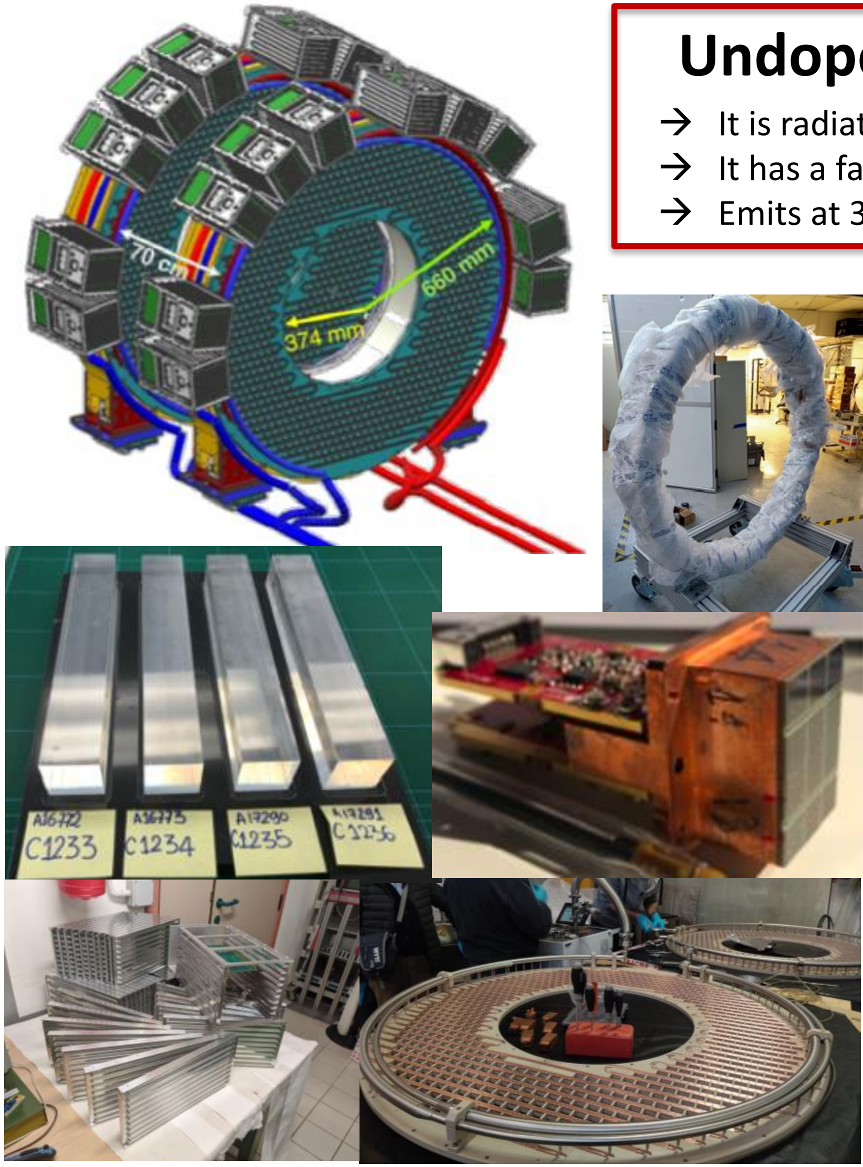
- Particle Identification capabilities with mu/e rejection of 200
- A fast trigger independent on the tracker
- Help in the track reconstruction





→ Provide energy resolution σ_E/E of O(10 %)
→ Provide timing resolution σ(t) < 500 ps
→ Provide position resolution < 1 cm
→ Work in vacuum @ 10^{-4} Torr and 1 T B-Field
→ Survive the harsh radiation environment

Calorimeter Design

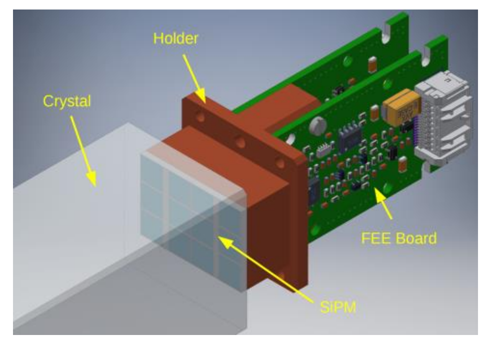


Undoped CsI + UV-extended SiPMs

- → It is radiation hard
- → It has a fast emission time
- → Emits at 310 nm

- → 30 % PDE @ 310 nm
- → New silicon resin window
- → TSV readout, Gain = 10^6

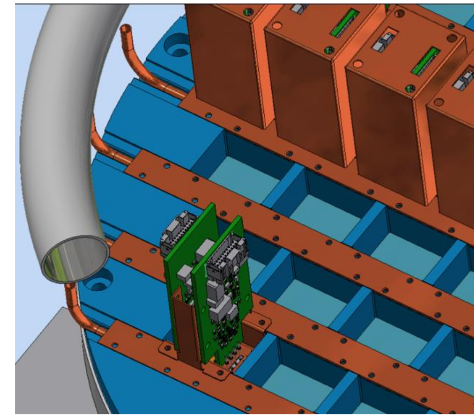
- ❑ Two annular disks, R_{in}=374 mm, R_{out}=660 mm, 10 X_0 length, ~ 70 cm separation
- ❑ 674 + 674 square x-sec pure CsI crystals, (34×34×200) mm^3, Tyvek + Tedlar wrapping
- ❑ Each crystal is read out by two large area UV extended Mu2e SiPM's (14x20 mm^2)

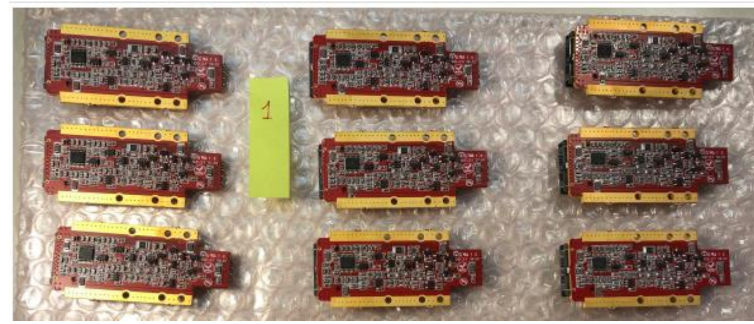


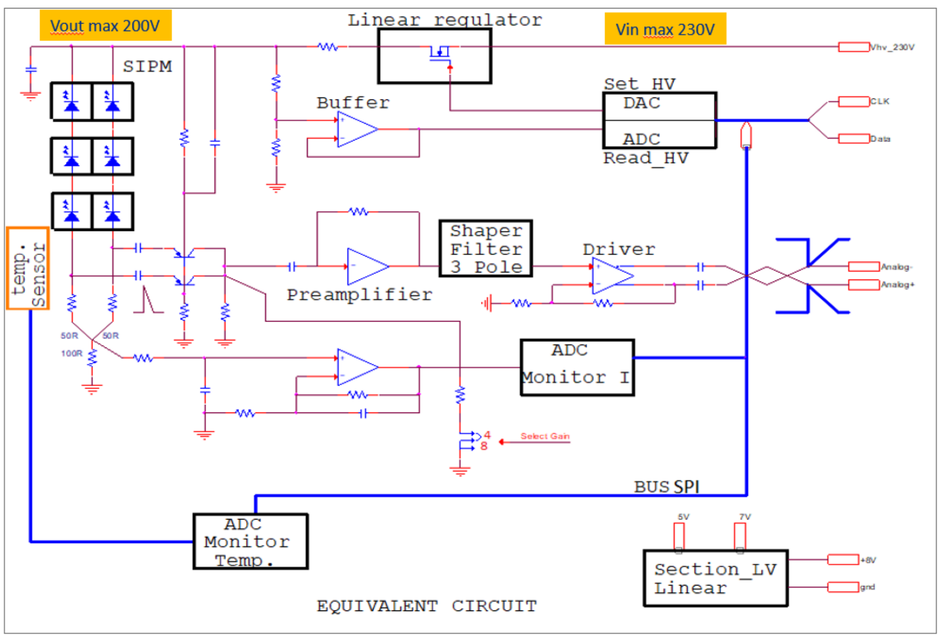
- ❑ Redundant readout: For each crystal, two custom arrays (2×3 of 6×6 mm2) large area UV-extended SiPMs

Front End Electronics

- FE boards connected directly to SiPMs to provide:
  - ❑ Local **linear regulation** of the ***bias* voltage**
  - ❑ Amplification & shaping (25 ns rise)
  - ❑ Monitoring of current and temperature
  - ❑ Test pulse
- 2696 chips + 800 spares produced..





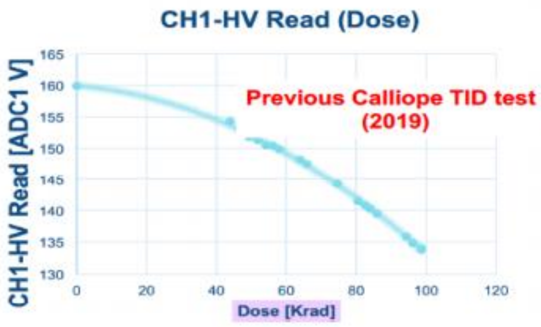


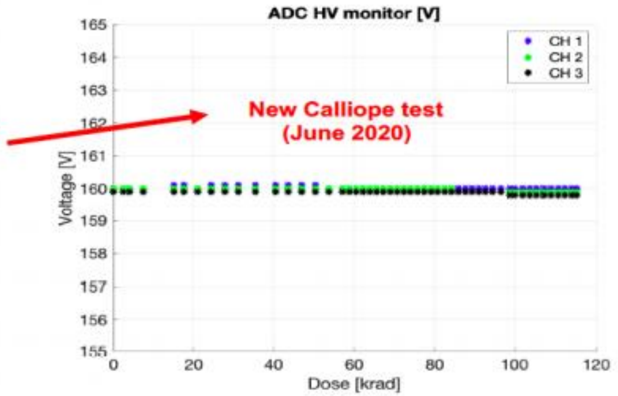
- ○ ***Magnetic field*** *of* ***1 T*** *and* 10^{-4} *Torr vacuum*
- ○ ***Total Ionizing Dose (TID):***
  - ➢ *1,8 krad/yr x 12 SF x 5 years*
  - ➢ *TID requirement of* ***100 krad***
- ○ ***Neutron flux*** 5×10^{11} *1 MeV (Si)*

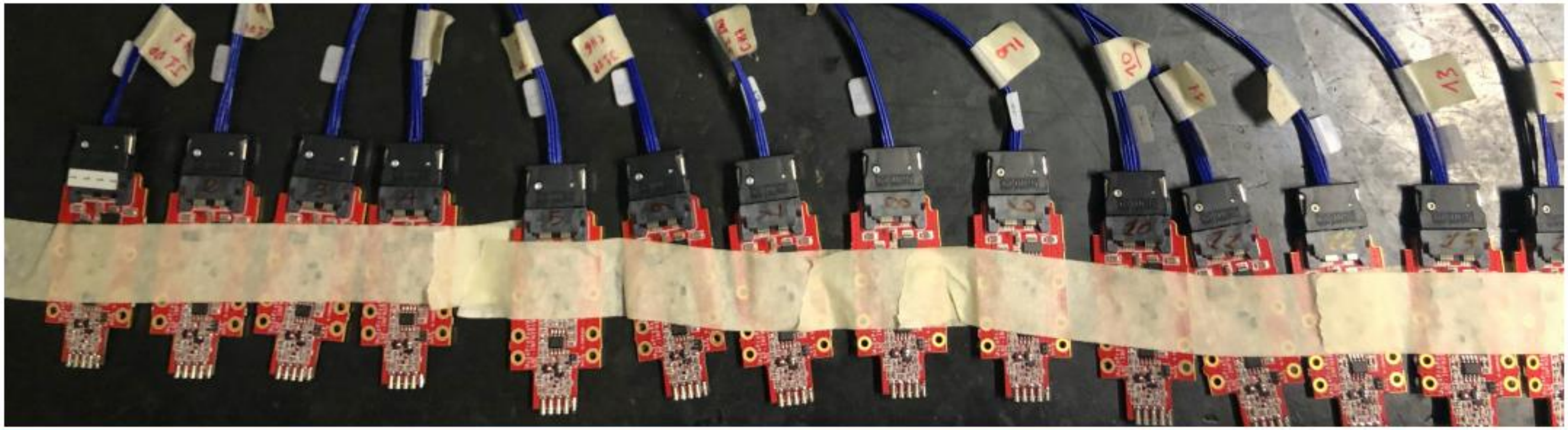
Front End Electronics Qualification

- Several irradiation campaigns have been carried out at the Calliope facility (ENEA Casaccia) and FNG (ENEA Frascati)

- Failures of single components observed in first prototypes, replaced with rad-hard components
- Last test in October 2020 satisfies the experimental requirements (100 krad)



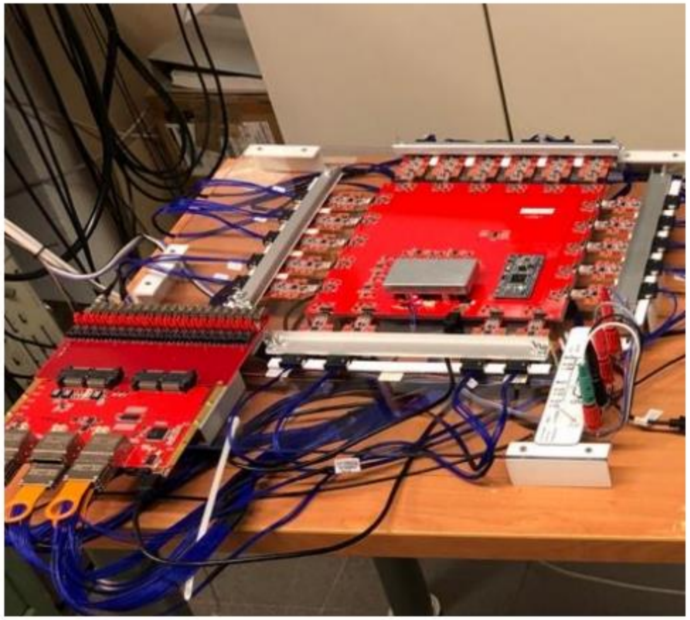




Front End Electronics Qualification

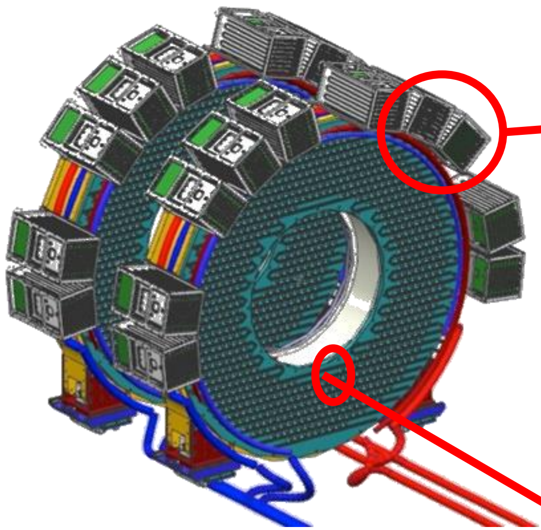
QC test station automatizing the work done during test phase with ALB – Active Load Board. It allows to set, read HV and to read the signal in groups of 20 channels. Three kinds of tests:

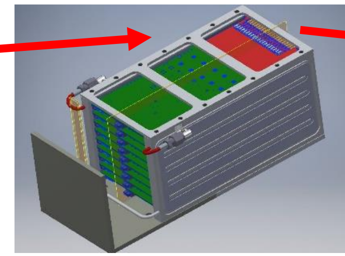
1. BURN-IN with HV on (six hours @ 65 C)
2. Determination of calibration values for HV setting/reading + T and I reading
3. Pulsing the FEE boards and extracting Gain (x1,x2), linearity and signal shape

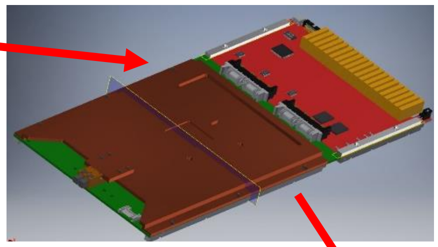


Burn-IN test completed on 750 FEE boards, only 1 dead channel

Readout Electronics Design



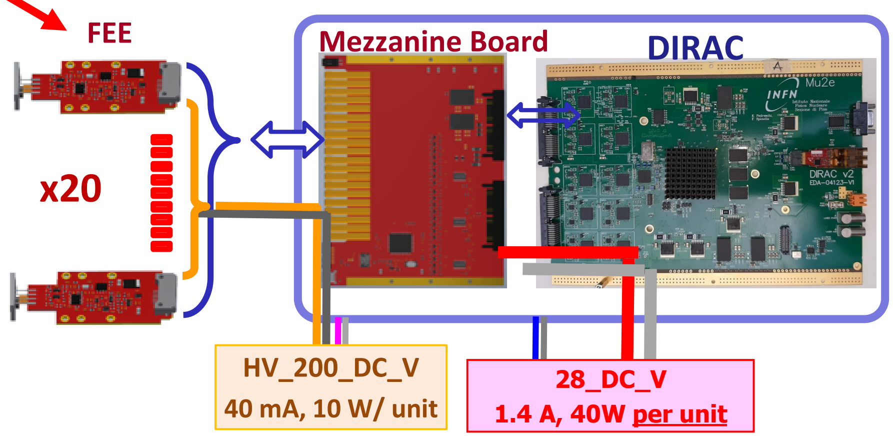




10 crates per disk with 6/8 boards/crate

- A digitizer system is needed due to the high expected pileup
  - About 2700 channels, 136 boards
  - Sampling frequency of 200 MHz
  - ADC with 12 bits resolution
- Mechanical constraints → DAQ crates located inside the cryostat:
  - *Limited space* → 20 ADC channels/board
  - Limited access for maintenance → *Highly Reliable Design* mandatory
  - Close to stopping target -> **Radiation hard electronics!**

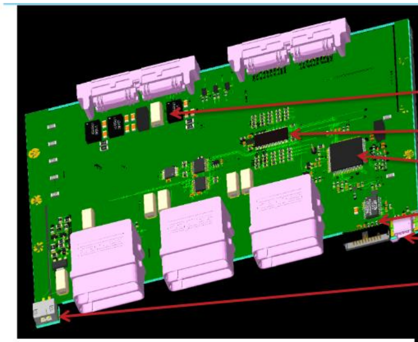
20 SiPM+FEE channels per board



Mezzanine Board

- ARM processor to control/set HV on FEE
- interface analog signals to DIRAC

- *Magnetic field of 1 T and 10^{-4} Torr vacuum*
- *Total Ionizing Dose (TID):*
  - *0,2 krad/yr x 12 SF x 5 years*
  - *TID requirement of **12 krad***
- ***Neutron flux** $5x10^{11}$ 1 MeV (Si)/yr*
- *Same number for DiRAC*

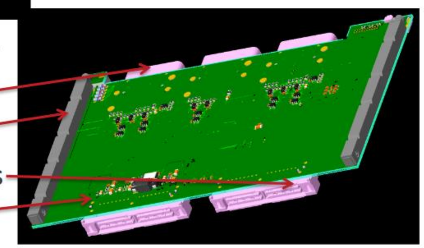


Mezzanine bottom view

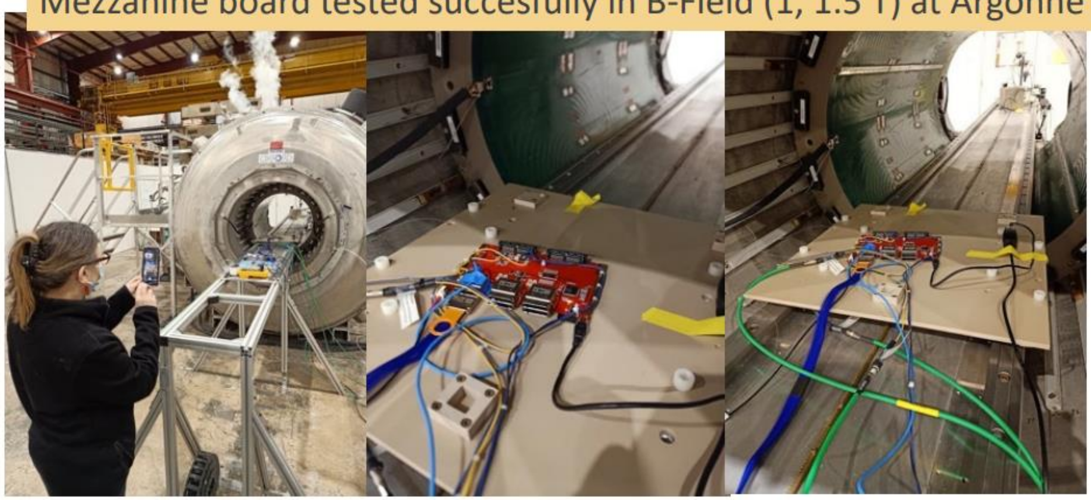
- Switching regulators
- Address selector
- Cpu ARM
- Jtag interface
- Serial interface
- High Voltage input

Top view

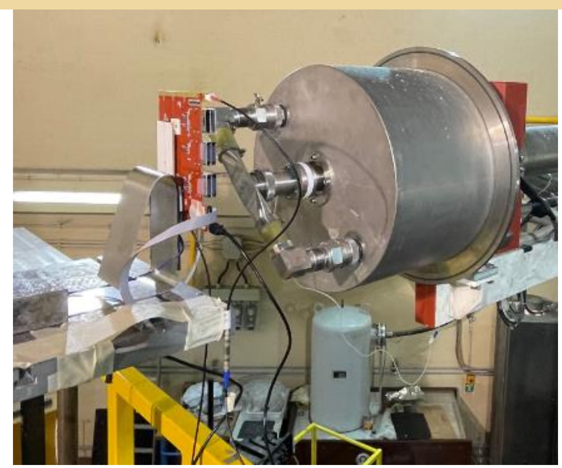
Front-end connectors
Card lock position
Digitizer interface connectors
Protection nets



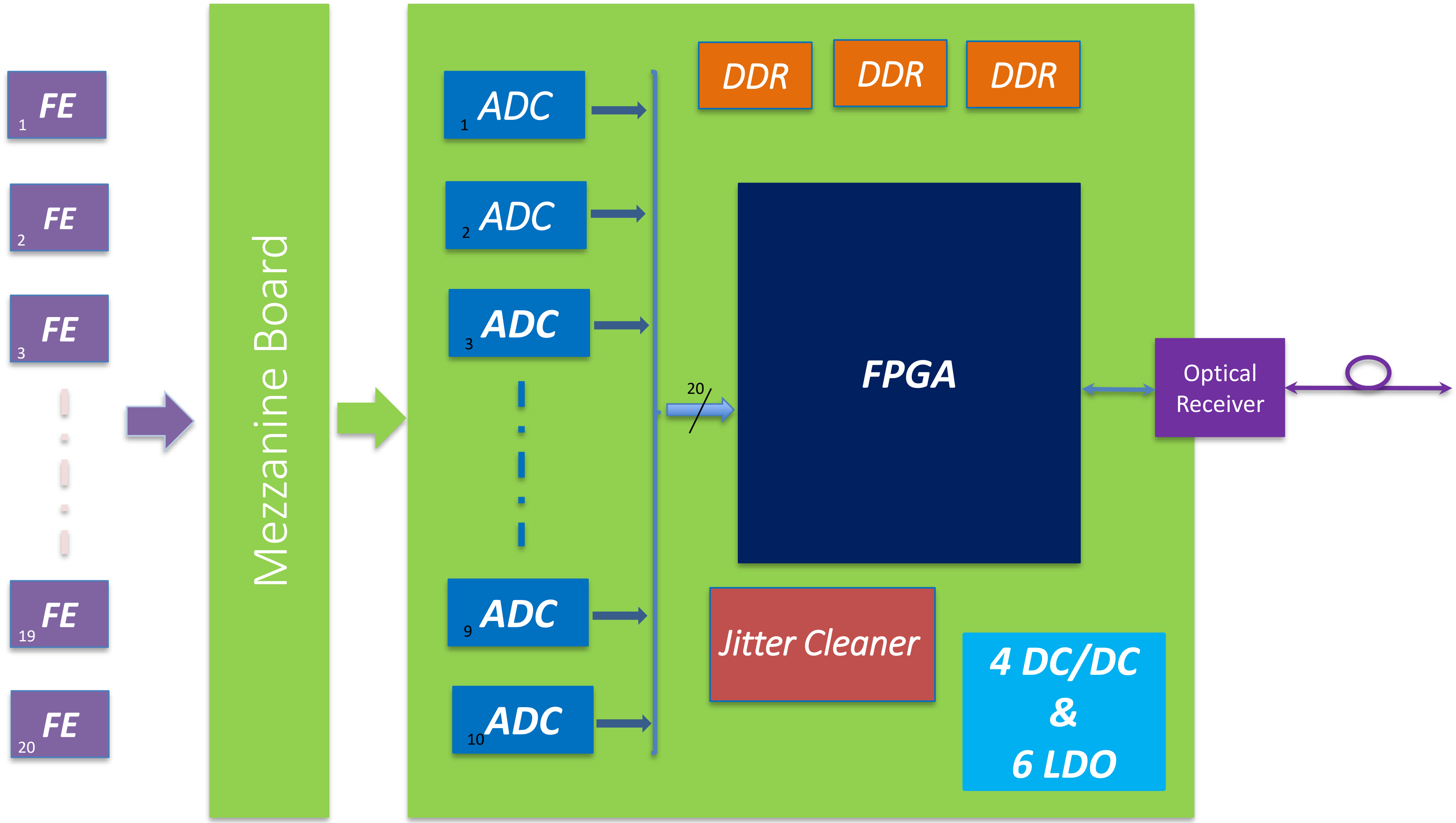
Mezzanine board tested succesfully in B-Field (1, 1.5 T) at Argonne



- **FNG @ENEA**
  - 14 MeV neutrons from D+T



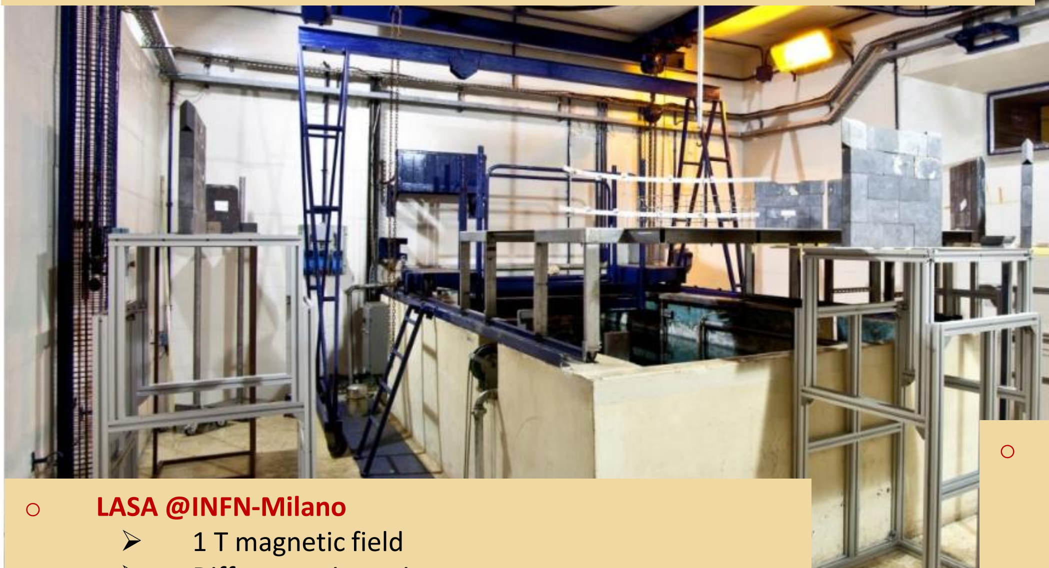
DiRAC Design



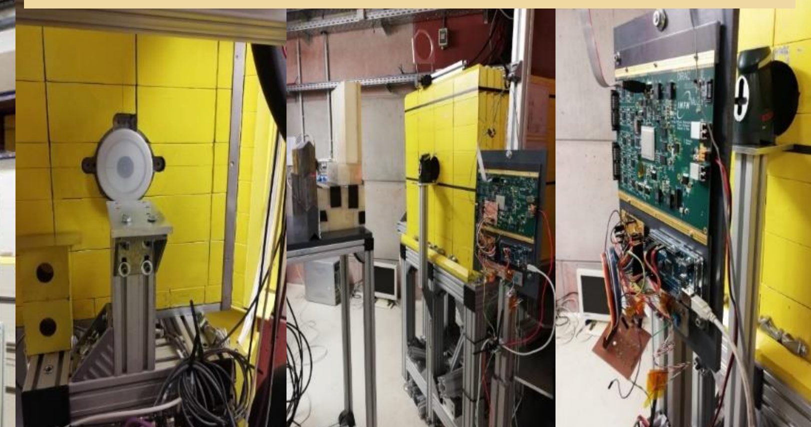
Sampling frequency of ***200 MHz,*** with ***12 bits resolution***

DiRAC Qualification Campaign

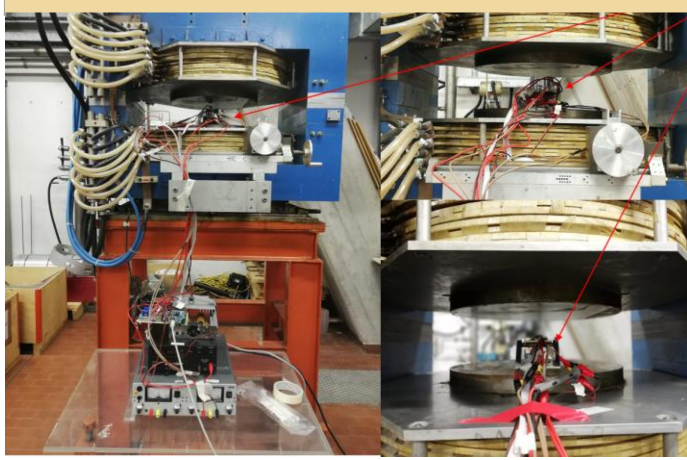
- **Calliope @ENEA**
  - Co60 source
  - Dose in function of distance: Max 2krad/h, requested 1krad/h
  - Full V1 board test

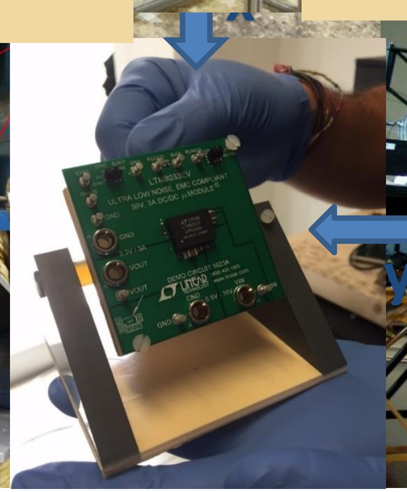


- **YELBE @HZDR**
  - γ from Bremsstrahlung (0<E<14MeV)
  - Estimated dose ≈ 20 krad/h @ 600µA
  - Single components test



- **LASA @INFN-Milano**
  - 1 T magnetic field
  - Different orientations





- **FNG @ENEA**
  - 14 MeV neutrons from D+T
  - Total neutron flux of 1.2 x10^12 n 1 MeV (Si) / cm^2
  - Total neutron flux of 6x10^11 n 1 MeV (Si) / cm^2

DiRAC V2

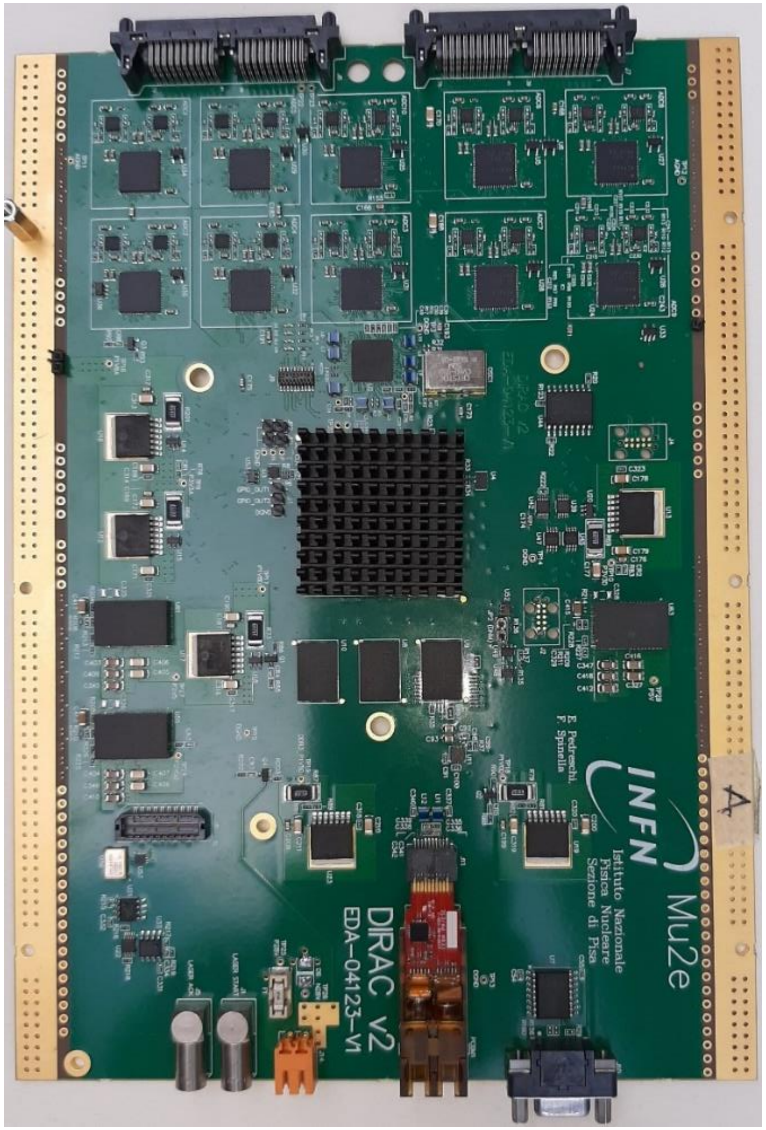
After an intense campaign of tests:

- ***ADC***: ADS4229 (Texas Instruments®)
- ***FPGA***: Polarfire MPF300 (Microsemi®)
- ***DC-DC***: LMZM33606
- ***LDO***: MIC69502 (Micrel®)
- ***Jitter Cleaner***: LMK04828 (Texas Instruments®)
- ***Optical Transceiver***: CERN VTRX

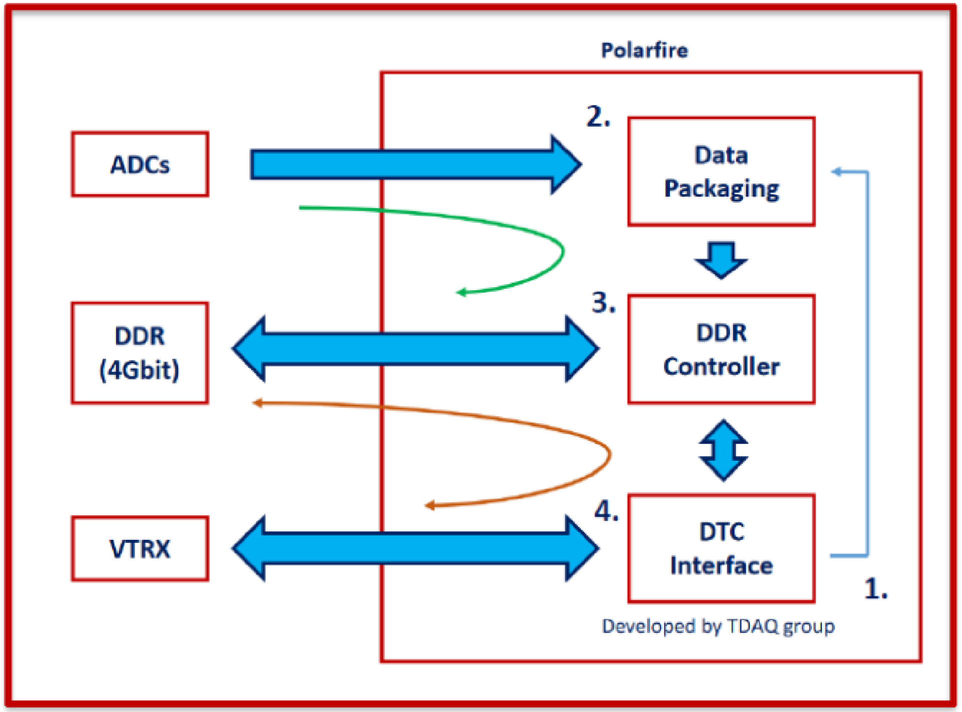
DIRAC V3 is under design to solve minor issues

<u>PCB specs:</u>

- ***Material:*** *FR408-HR*
- ***Layers:*** *16*
- ***Dimensions:*** *233x165 mm*
- ***Thickness:*** *2.127 mm*
- ***Differential lines***: 100 *Ω*
- ***Single ended lines***: *50 Ω*



Dirac Firmware Main Flow



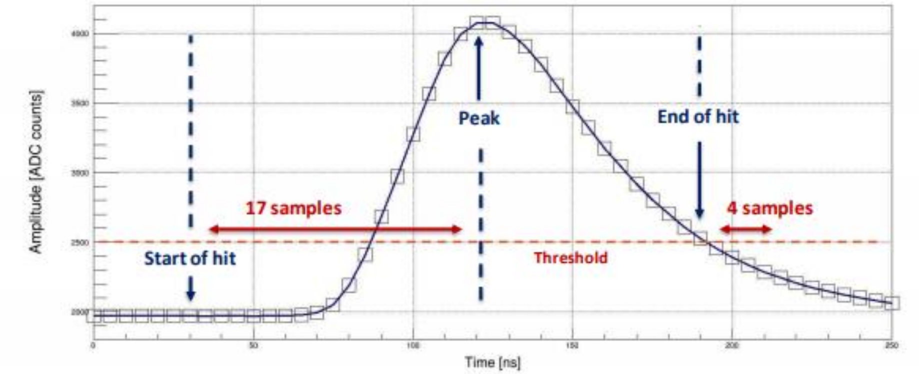
1. TDAQ sends Heartbeat packet that contains EVENT TAG and EVENT WINDOWS
2. DiRAC builds the calo hit applying a zero suppression and pre-processing data
3. Data are stored in the DDR
4. TDAQ sends Data Request for a specific EVENT TAG, and DiRAC retrieve requested Data Packet from DDR and sends it out to DTC

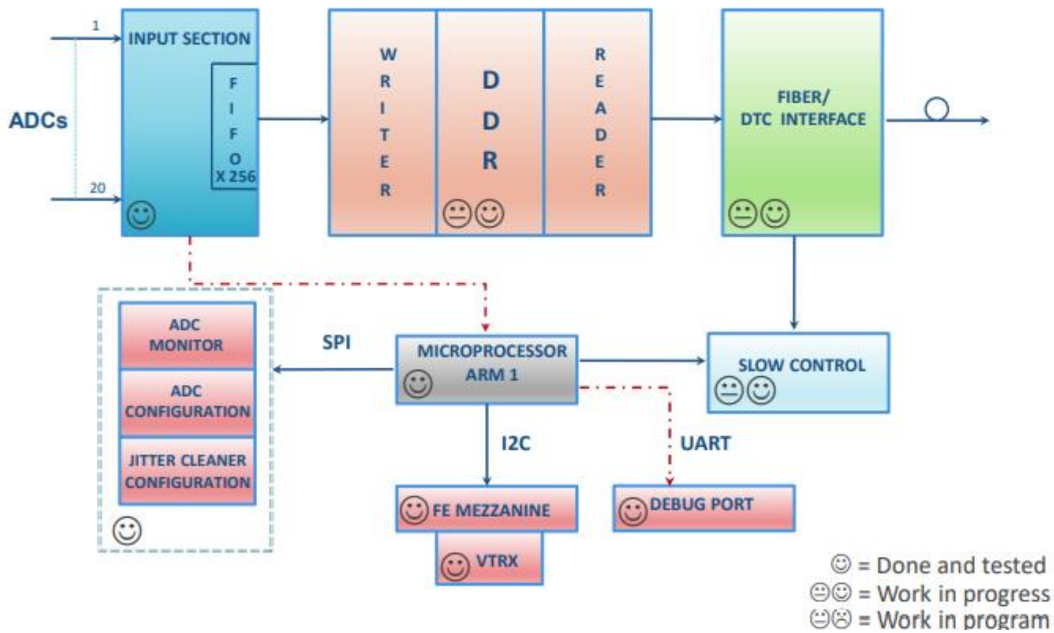
DiRAC Firmware Status

- ❑ Slow Speed serial communication @1Mbits

1. Initialization of ADCs and Jitter cleaner
2. Synchronization of the clock phase
3. Digitization of 20 chs @ 200 MHz
4. Zero suppression
5. Event window according to selected running mode
6. Reading of monitoring ADCs

- ❑ **Implementation of Interface for the DTC readout via fiber and VTRX in progress**

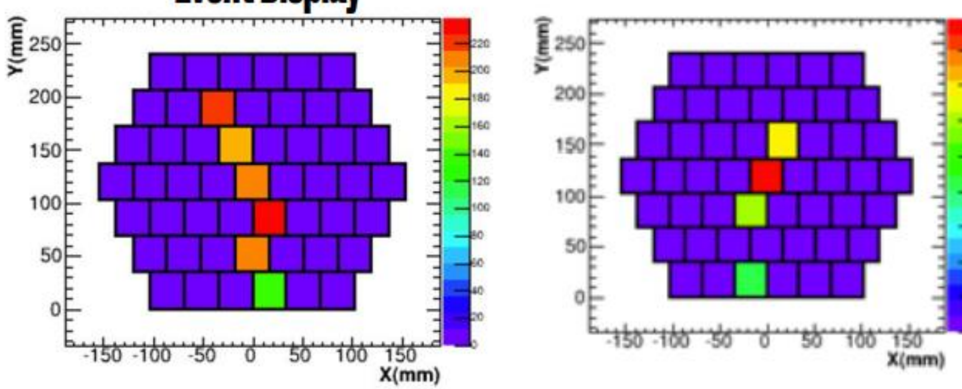




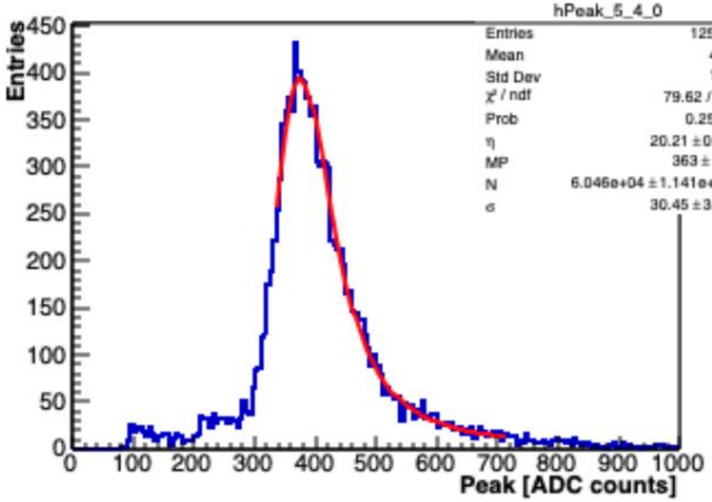
Vertical Slice Test

20 channels of the Module-0 with Final Mezzanine Board and Dirac have been tested with cosmic rays..

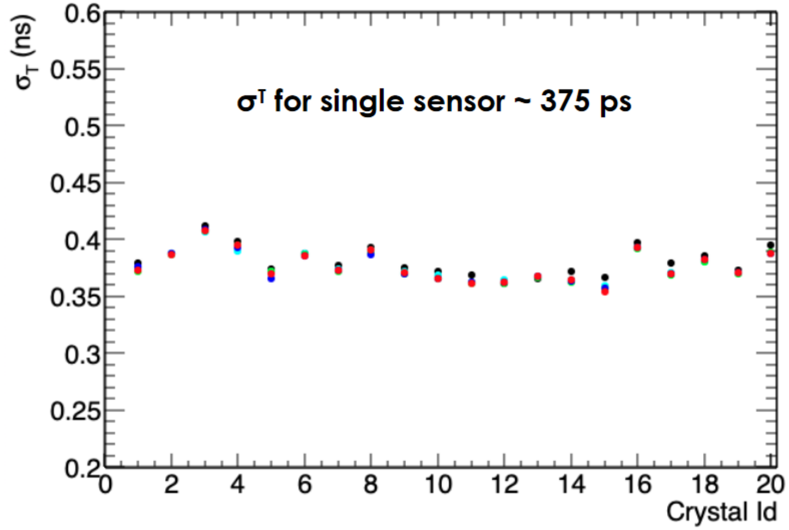
Event Display



Vertical Slice Test



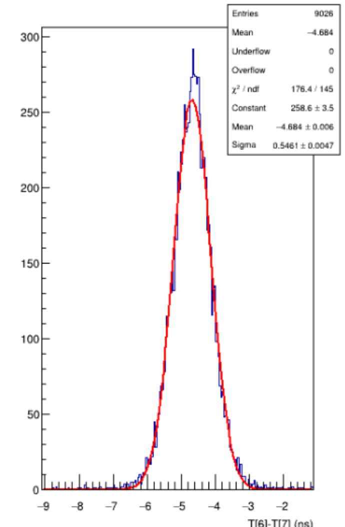
Energy distribution deposited by cosmic rays



Time resolution for different channels

1. Comparison with commercial digitizer showed no differences in performances
2. Obtained time resolution in accordance with expectations
3. Noise level and dynamic scale as expected

- **We can proceed with the production..**



$\sigma_T \sim 390$ ps

Conclusions

- The Electronics of the Mu2e calorimeter has been presented.
- The presence of vacuum (10^{-4} Torr), high magnetic fields (1T) and radiation (Non-Ionizing Energy Loss $5x10^{11}$ n/cm^{2} @ 1 MeV$_{eq}$ (Si)/y and Total Ionizing Dose 12 Krad) makes the environment particularly harsh and the design of the board very challenging
- The DIRAC is designed to sample @200 MHz – 12 bit differential signals coming from SiPM and amplified by a custom FEE.
- We described the apparatus, the design specification, the architecture and the technical choice
- The system has been qualified

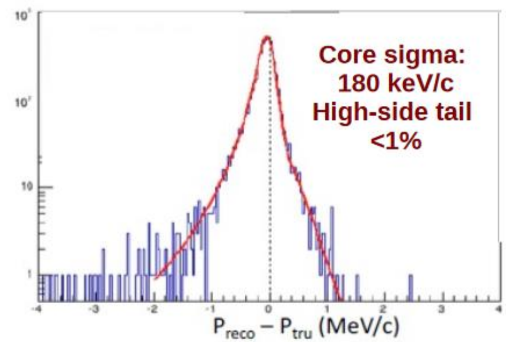
This work was supported by the European Union's Horizon 2020 research and innovation programme under the Marie Sklodowska-Curie Grant Agreement no 734303, 822185, 858199, 101003460

Additional Slides

The Mu2e Detector

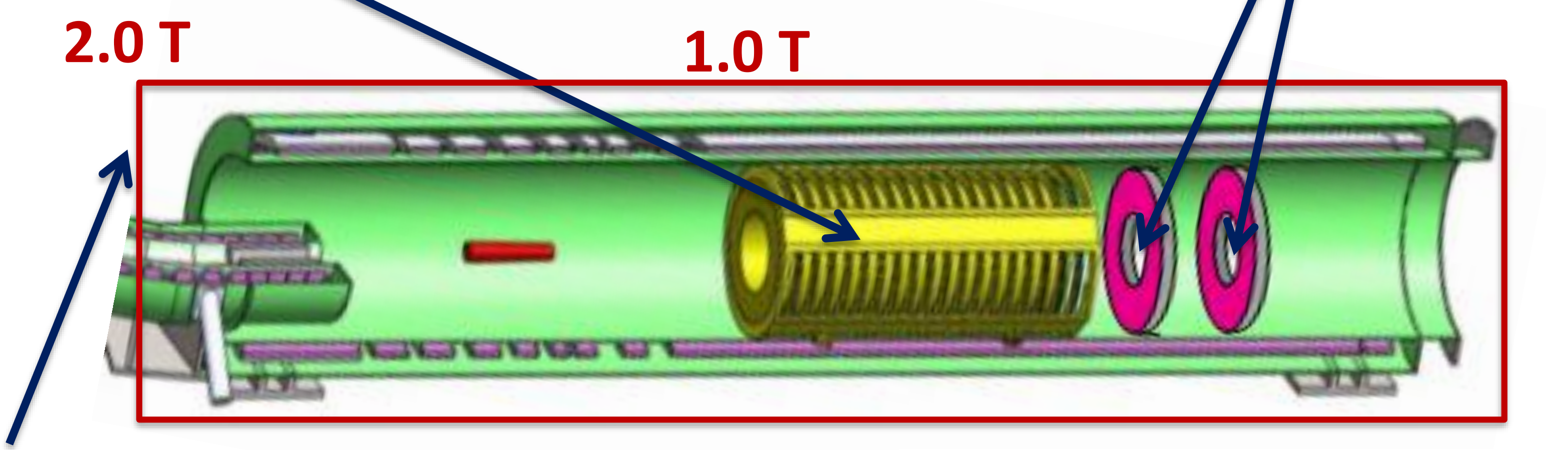
Straw Tracker:

- High precision momentum measurement
- 20000 low mass straw drift tubes



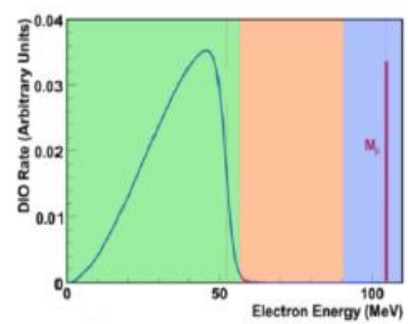
Crystal Calorimeter:

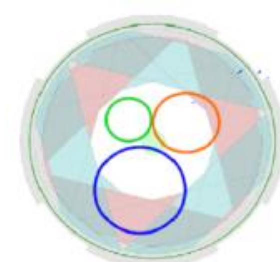
- Energy, time and position measurements



- A **Cosmic Ray Veto System** surrounds the detector solenoid:
  - **veto inefficiency < 10^{-4}**

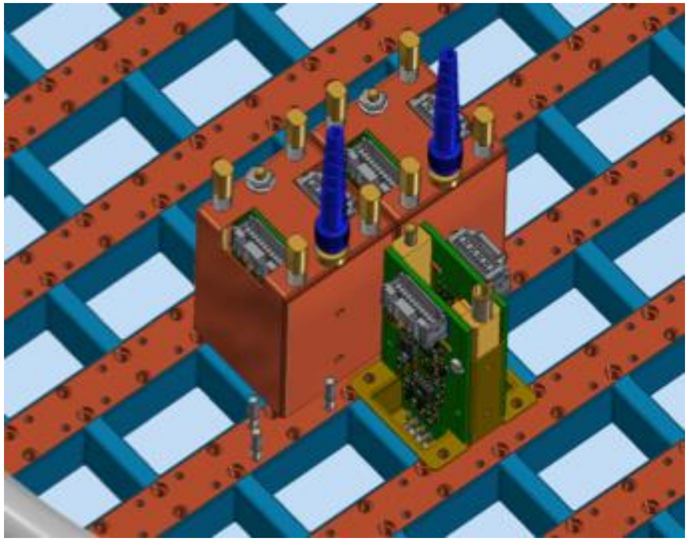
The detectors have an annular geometry, in order to be blind to low momentum particles coming from muon decays

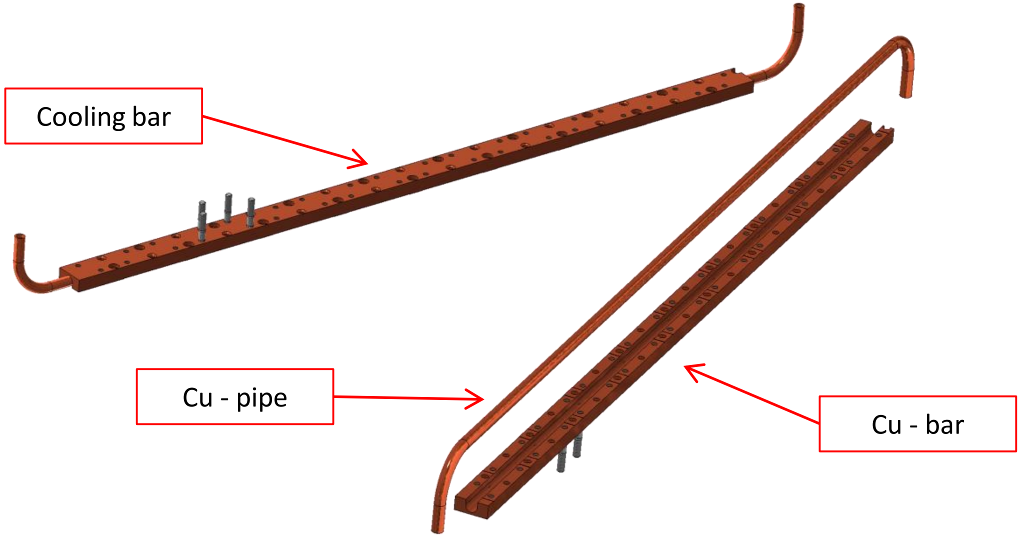


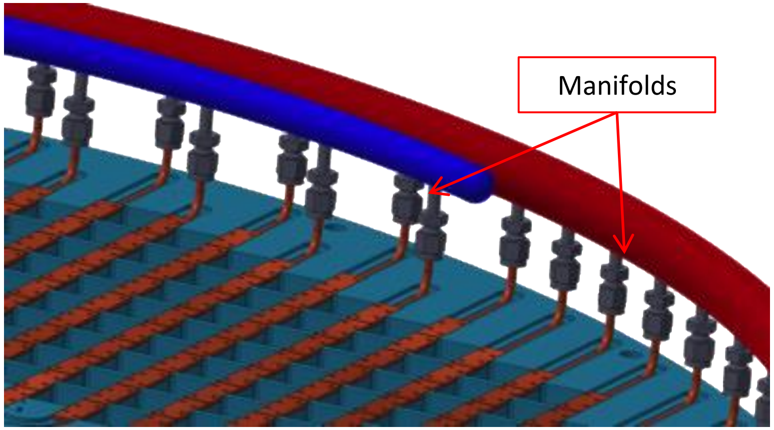


Calorimeter Cooling

- The FEE plate houses the Front End electronics and photosensors holders and provides cooling.
- The coolant runs inside the cooling channels, at ~ -10ºC.
- The manifolds are jointed to the cooling channels by means of tube fittings (Swagelok type).
- The SiPM holders are bolted to the cooling channels by means four stud screws. It is in thermal contact with the cooling channels.
- The plate is thermally isolated from the outer ring and from the crystals.







DiRAC Design

- **A digitizer system is needed due to the high expected pileup**
- Simulation results show that a digitizer with:
  - Sampling frequency of ***200 MHz***
  - ADC with ***12 bits resolution***

  Matches the calorimeter requirements on time and energy resolution

	150 MHz	200 MHz	250 MHz
8 bits	470 ps	440 ps	440 ps
10 bits	370 ps	250 ps	250 ps
12 bits	300 ps	170 ps	170 ps

Time resolution versus sampling frequency and ADC-bits

- ***Time*** is reconstructed by a template fit of the rising edge
- Time resolution for CE @105 MeV

	150 MHz	200 MHz	250 MHz
8 bits	9.8 MeV	8.0 MeV	7.8 MeV
10 bits	6.5 MeV	5.5 MeV	5.5 MeV
12 bits	6.2 MeV	5.5 MeV	5.5 MeV

Energy resolution versus sampling frequency and ADC-bits

- ***Energy*** is reconstructed by the normalization of a template fit
- Energy resolution (FWHM/2.35) for CE @105 MeV