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The upgrade on the ATLAS electronic systems in view of the High Luminosity challenge

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To maximize the physics reach, the LHC plans to increase its instantaneous luminosity to $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, delivering from 3 to 4 ab^{-1} of data at $\sqrt{s} = 14 \text{ TeV}$. In order to cope with this operation condition, the ATLAS detector will require new sets of both front-end and back-end electronics. A new trigger and DAQ system will also be implemented with a single-level hardware trigger featuring a maximum rate of 1 MHz and 10 μs latency. Enhanced software algorithms will further process and select events, storing them at a rate of 10 kHz for offline analysis. The large number of detector channels, huge volumes of input and output data, short time available to process and transmit data, harsh radiation environment and the need of low power consumption all impose great challenges on the design and operation of electronic systems. This talk will focus on these challenges, the proposed solutions and the latest results obtained from the prototypes.

This abstract is being submitted by the ATLAS Upgrade Speaker Committee representative. If approved, the speaker will be selected from ATLAS Collaboration and the conference will be informed.

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