The upgrade on the ATLAS electronic systems in view of the High Luminosity challenge

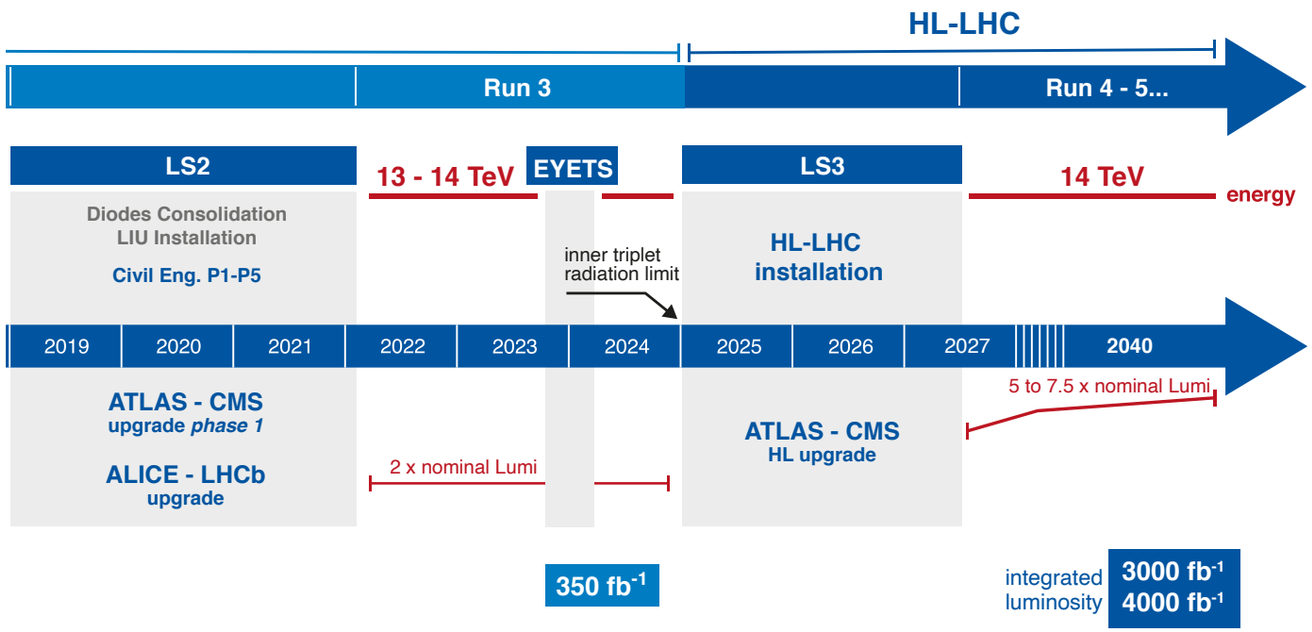
Stefan Guindon (CERN)

On behalf of the ATLAS Collaboration

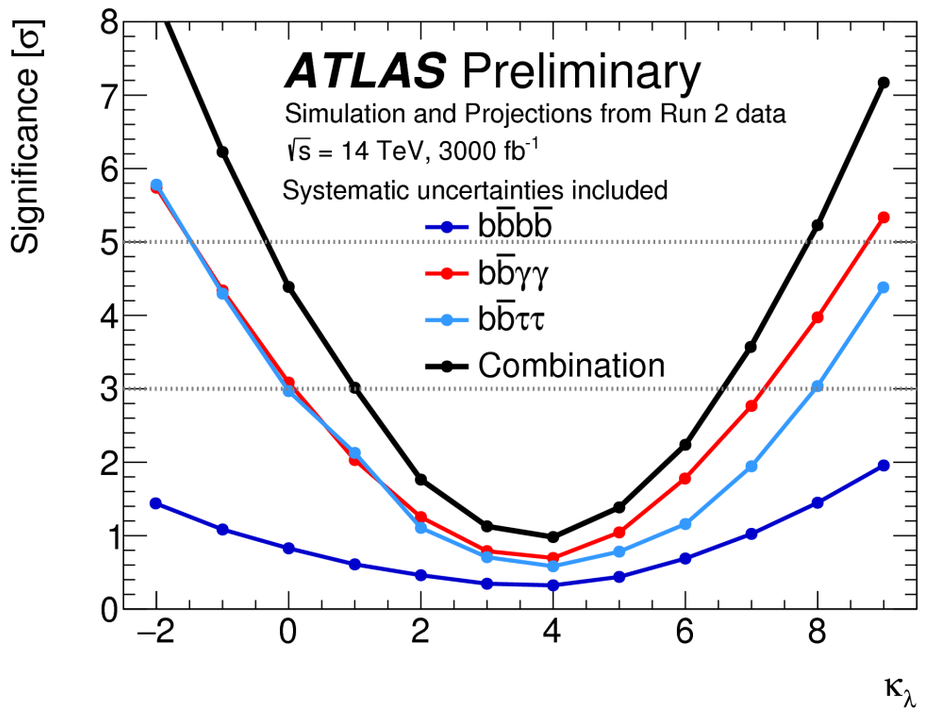
PANIC 2021
September 5th, 2021

Motivation for HL-LHC

- **High Luminosity LHC: 2027 and beyond**
  - Instantaneous luminosities up to L ≃ 7.5×10^{34} cm^{-2} s^{-1} (currently ~ 2×10^{34})
  - Pile-up $<\mu>$ = 200 interactions per bunch crossing (currently ~ 34)
  - Deliver 4000 fb^{-1} integrated luminosity at 14 TeV



- **Fully exploit the physics potential of the HL-LHC:**
- ***Continued extensive test of SM at the TeV scale***
  - Precise measurements of Higgs couplings, including self-coupling
  - Precision SM measurements
  - Searches for new physics
  - Higgs as a portal to the dark sector



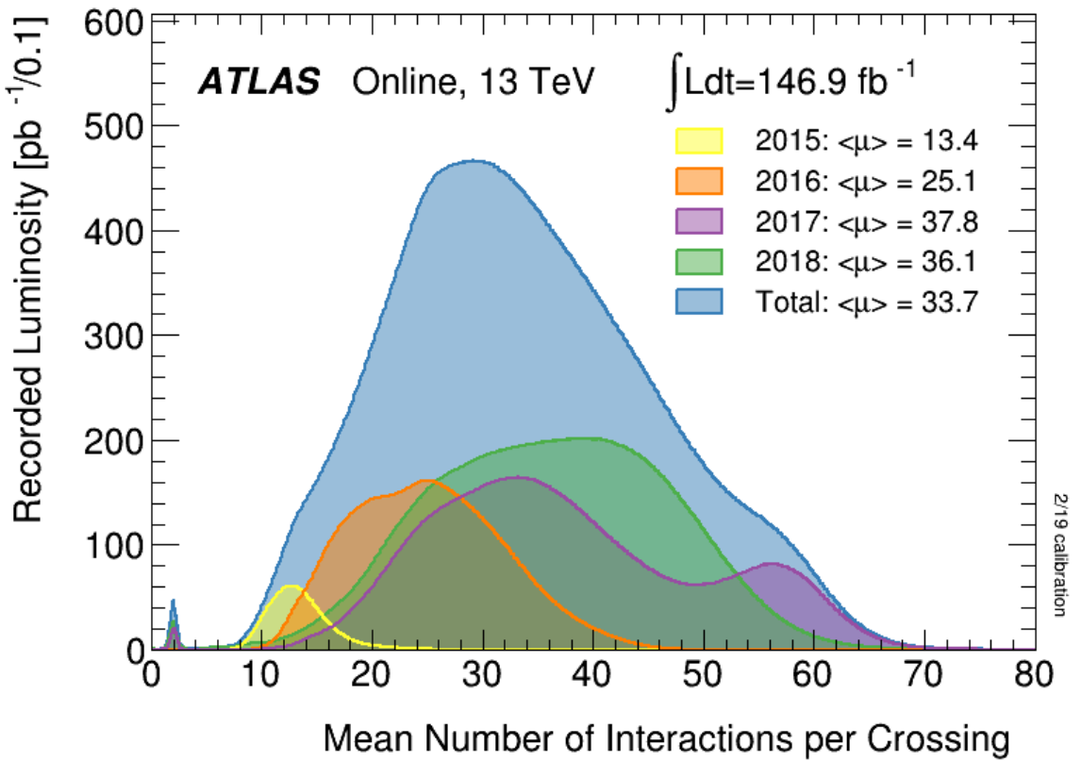
CERN-LPCC-2019-01

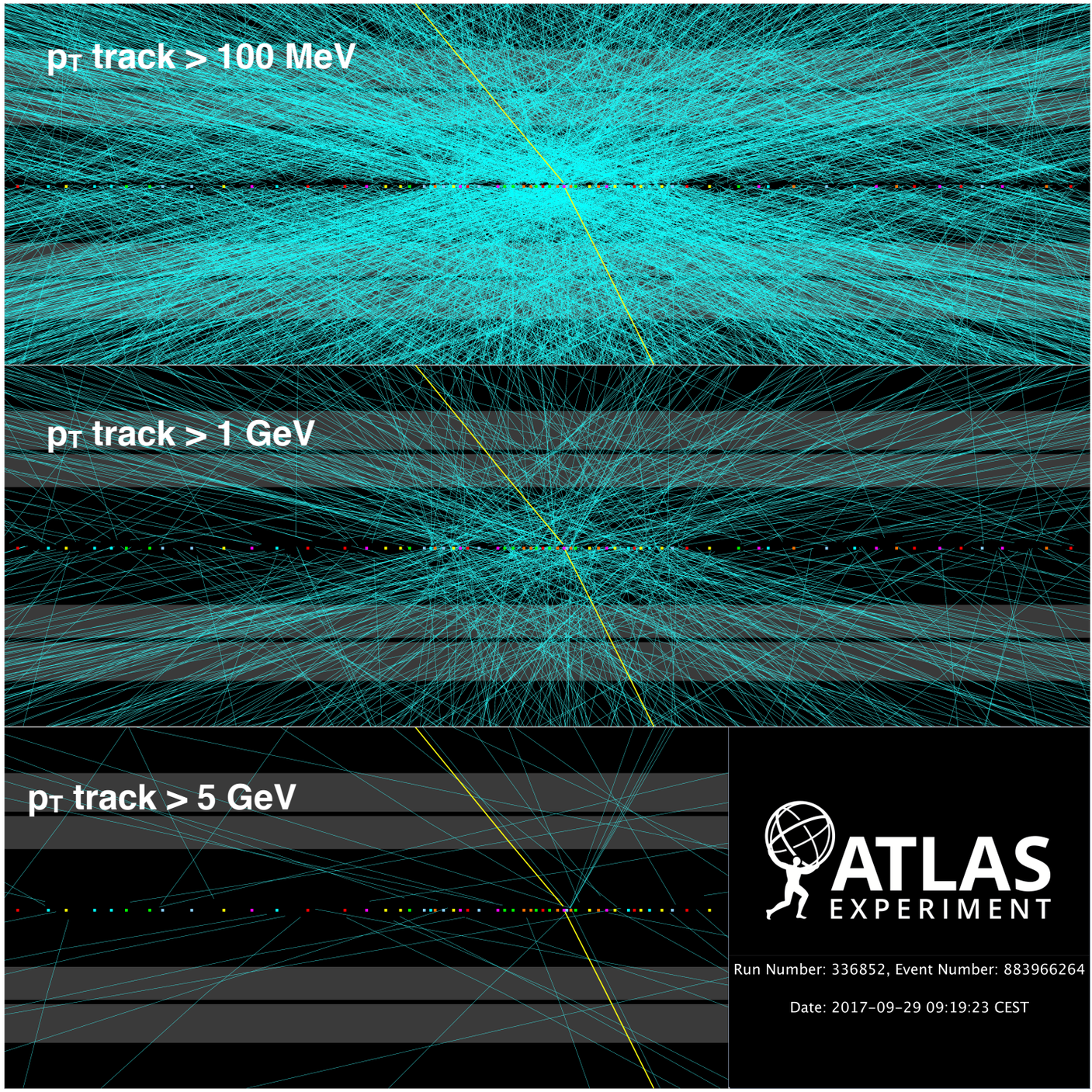
Challenges of HL-LHC Data-taking

- **Average number of interactions per bunch crossing for 2018: $< \mu > \sim 36$**

- Z->μμ candidate event with 65 additional reconstructed vertices from minimum bias interactions ($\mu \sim 90$)

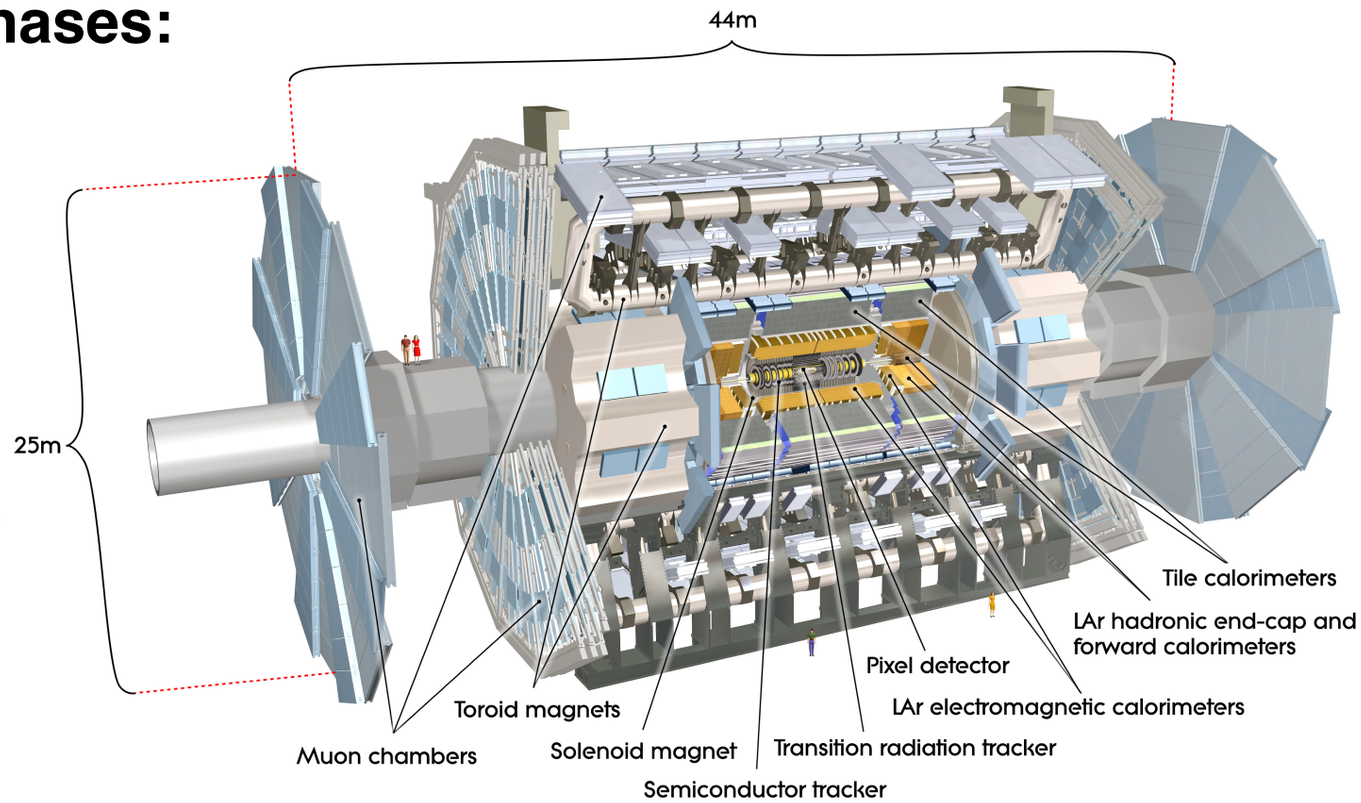
- **HL-LHC: 200 interactions per bunch crossing**
  - *Challenges to online and offline detector performance*





ATLAS in the HL-LHC

- **Upgrades to ATLAS detector in two phases:**



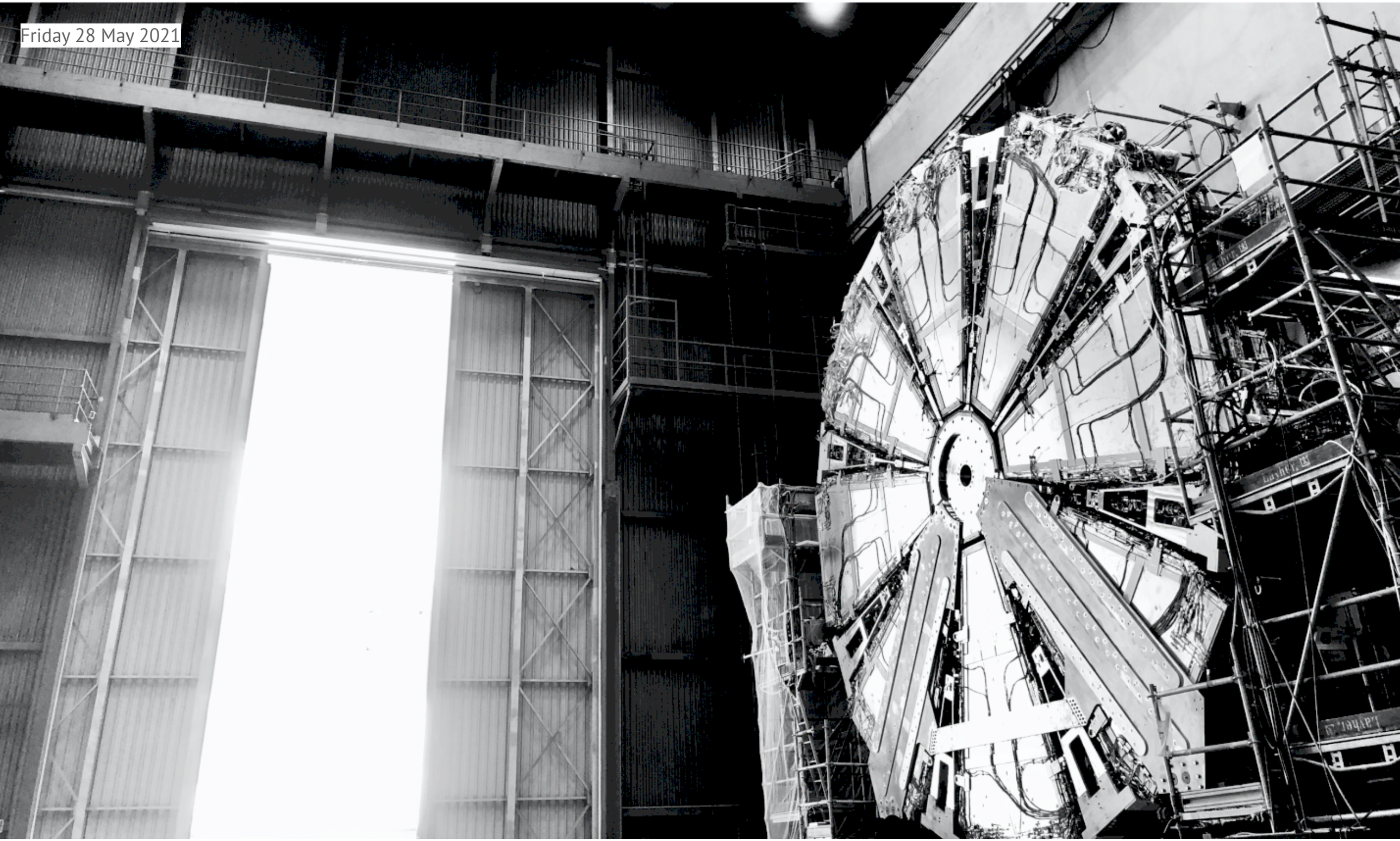
- **Phase-I (current LS2):**
  - **New Small Wheel:** new sTGC and MM chambers
  - **L1Calo:** finer granularity in hardware

- **Phase-II (LS3):**
  - **New hardware triggers** (L0)
  - **Upgraded DAQ** for higher rates
  - **Data streaming at 40 MHz for calorimeter and muon systems** to off-detector readout and trigger electronics

  - **Inner Tracker (ITk):** New all-silicon inner detector with coverage up to $|\eta|<4$
  - **High-Granularity Timing Detector (HGTD):** New silicon detector in end-cap region with excellent time resolution
  - **New muon chambers** in inner barrel region

New Small Wheel pre-Installation

Friday 28 May 2021

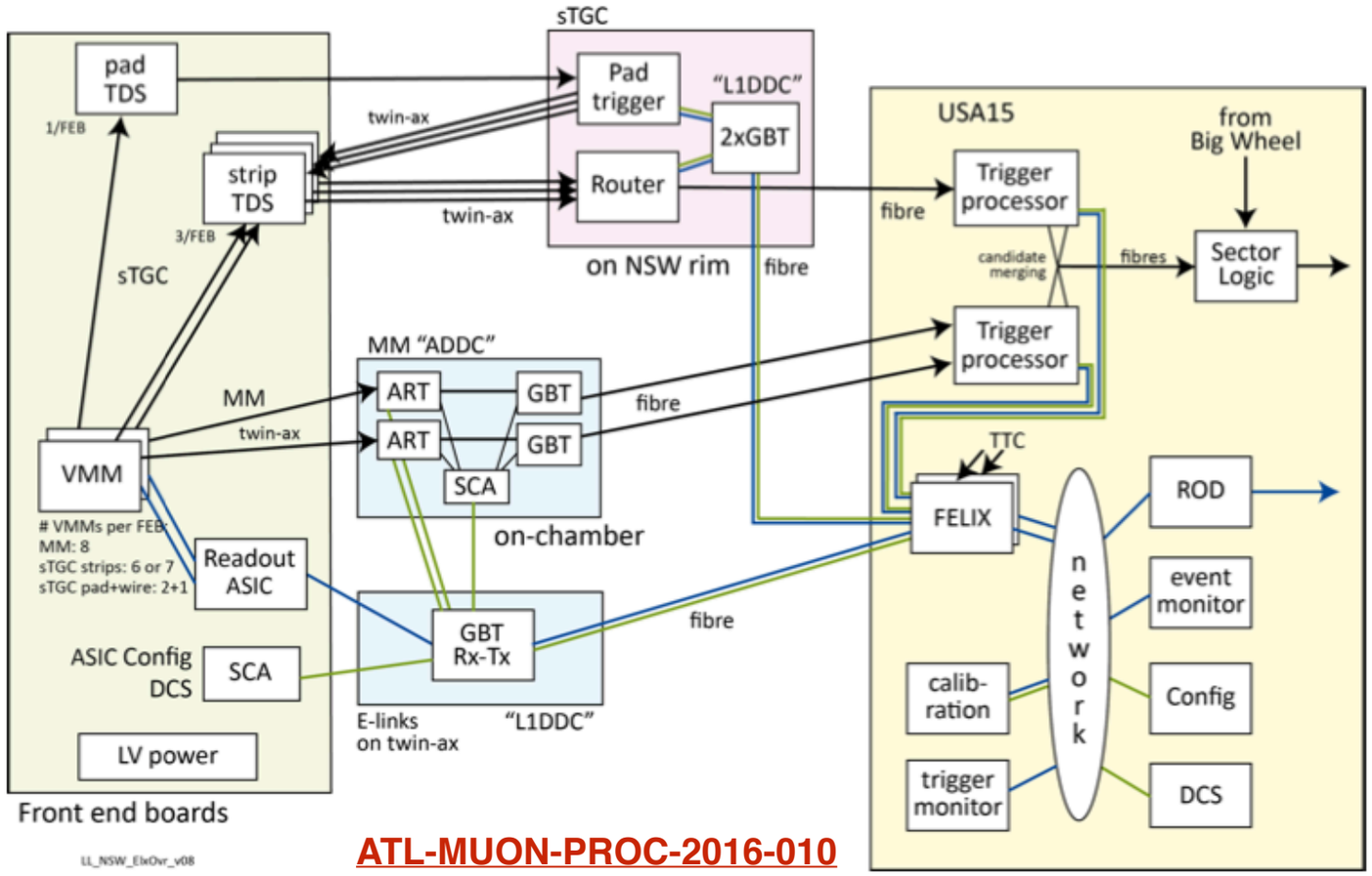


https://cds.cern.ch/record/2771285

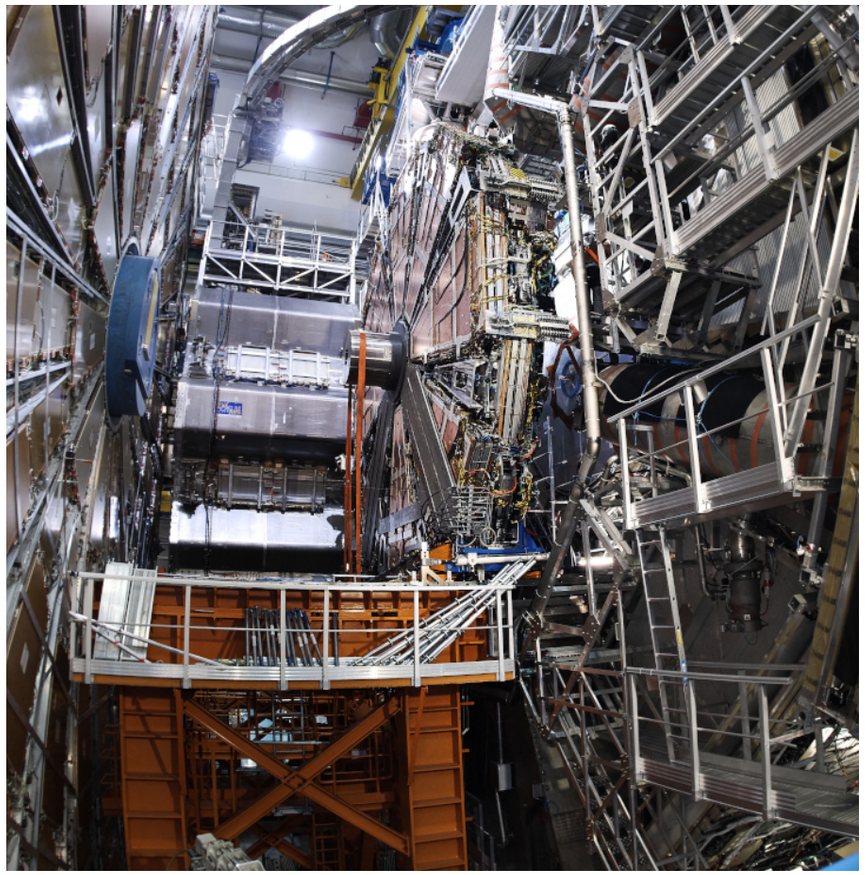
New Small Wheel

CERN-LHCC-2013-006

- **NSW electronics trigger and dataflow**
- Trigger Rate upgrades up to 1 MHz in HL-LHC - *fully compliant with rates*



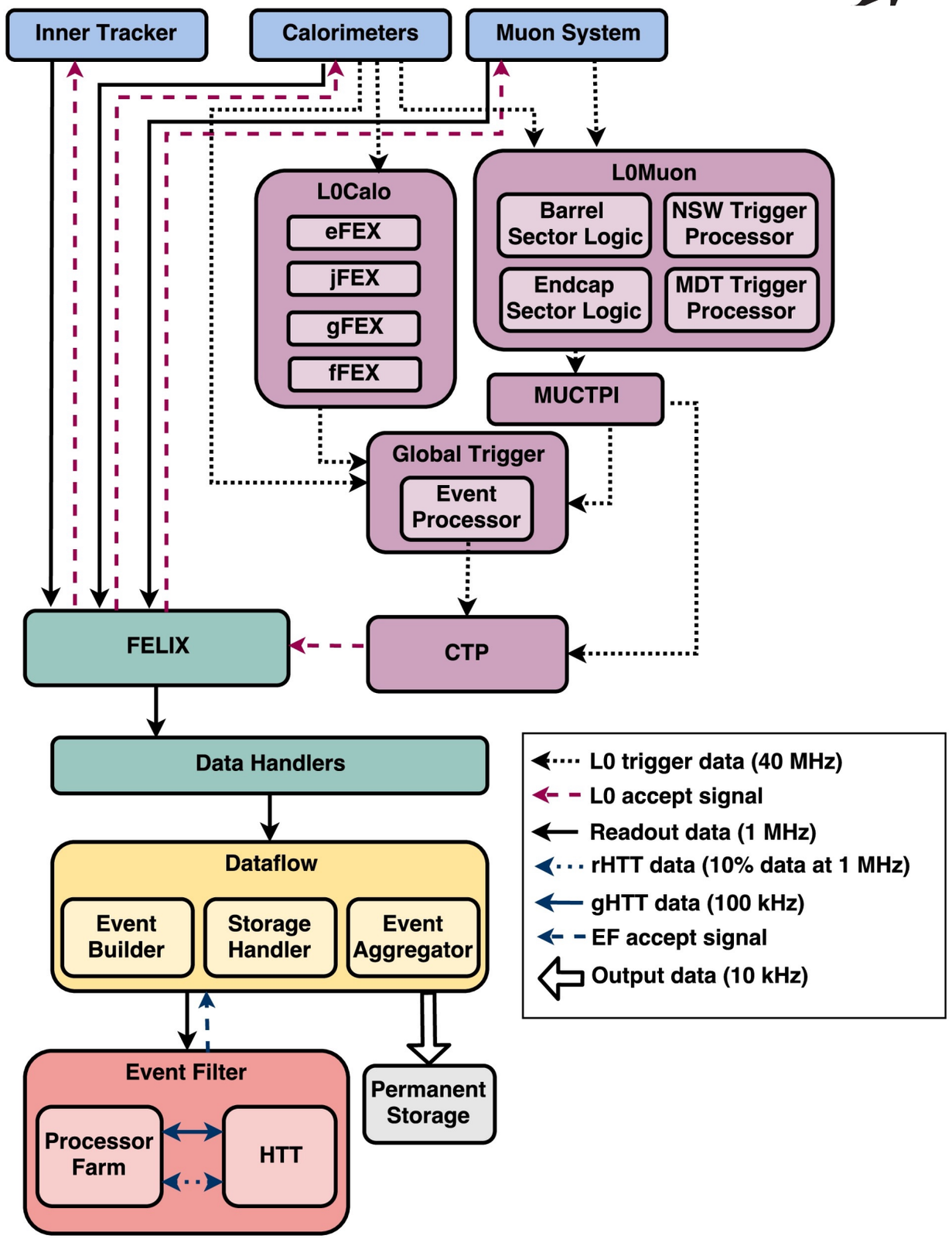
ATL-MUON-PROC-2016-010



- **New MicroMegas (MM) and sTGC chambers installed during LS2**
  - Using Front-End Link eXchange (FELIX): FE <—> backend components, FPGA-based
  - FEAST DC-DC rad-hard up to TID of 200 MRad and 5×10^{14} n/cm^2 NIEL
  - GBTx 130 nm CMOS chips for continuous read-out through FELIX
- **SCA-GBTx-FELIX communication chain (inbound configuration to ASIC)**

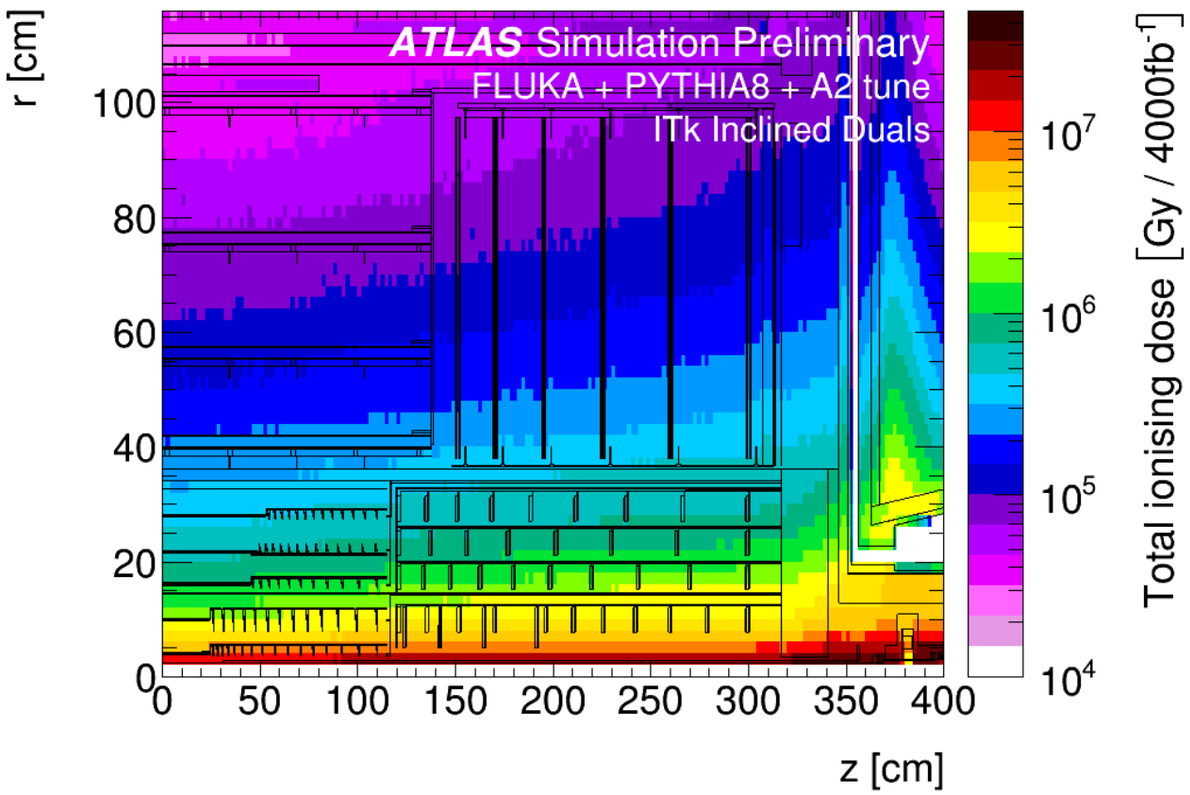
Phase-II Trigger architecture

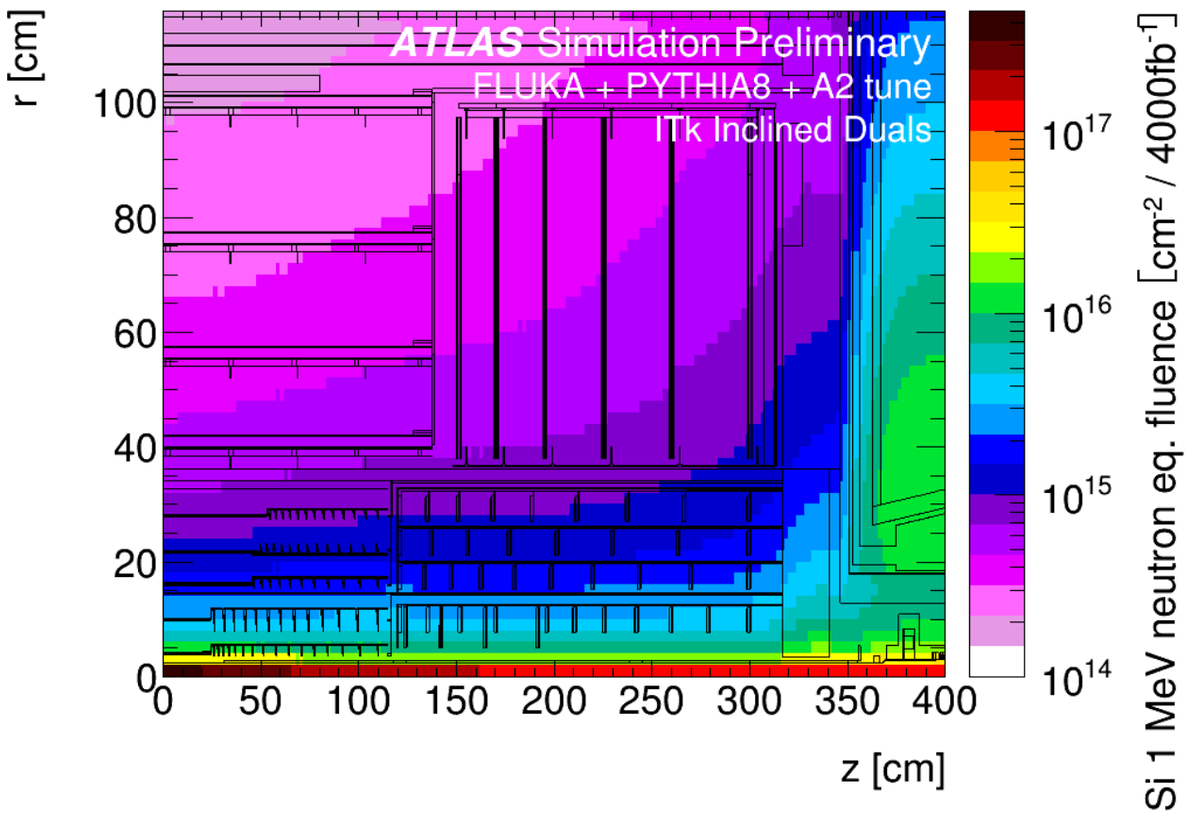
- **ATLAS Phase-II Trigger system will be L0-only**
  - Hardware based Trigger at 40 MHz
  - Feature extractors for calorimeter and muon systems combined at Global Trigger with improved acceptance and momentum resolution
- **Full FELIX read-out after LS3**
- **Event Filter Trigger**
  - Provide high-level Trigger functionality using algorithms close to offline reconstruction and tracking methods
  - Recommendation to commit to a commodity-based solution



Radiation Maps at 4000 fb^{-1}

Radiation Simulation





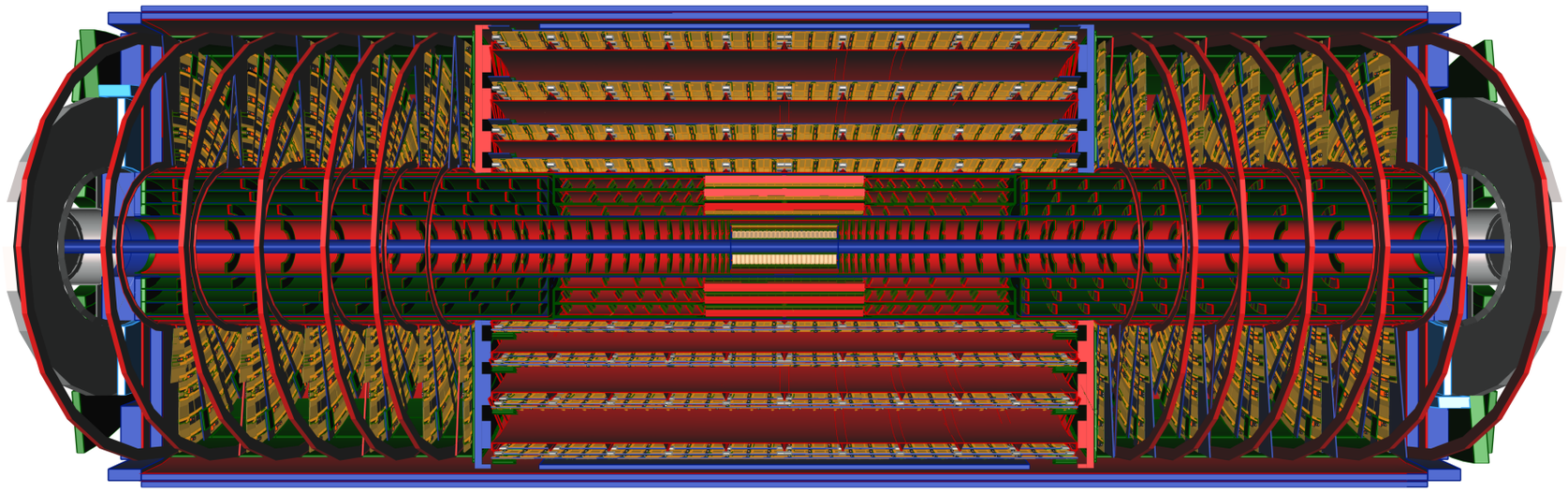
- **TID > 10 MGy and 10^{16} 1 MeV n/cm^2 fluence in ITk inner system**
  - Up to 1 MGy TID and 10^{15} 1 MeV n/cm^2 fluence in the outer layers
  - Use radiation tolerant ASIC designs and optimized services *(100x Run-2 values)*
- **TID ~ 100 Gy and 10^{14} 1 MeVn/cm^2 in the outer layers of the detector**
  - Allow use of flexible FPGA designs and single-point-failure-free engineering

- **Require qualification against TID (surface effects, transistor damage) and SEE (single event upsets, latch-up events)**

ITk: Phase-II Inner Tracker

ATL-PHYS-PUB-2021-024

- **All silicon tracker to replace the current ATLAS inner detector**
- **4 strip and 5 pixel barrel layers + 2x6 strip disks and pixel ring layers**

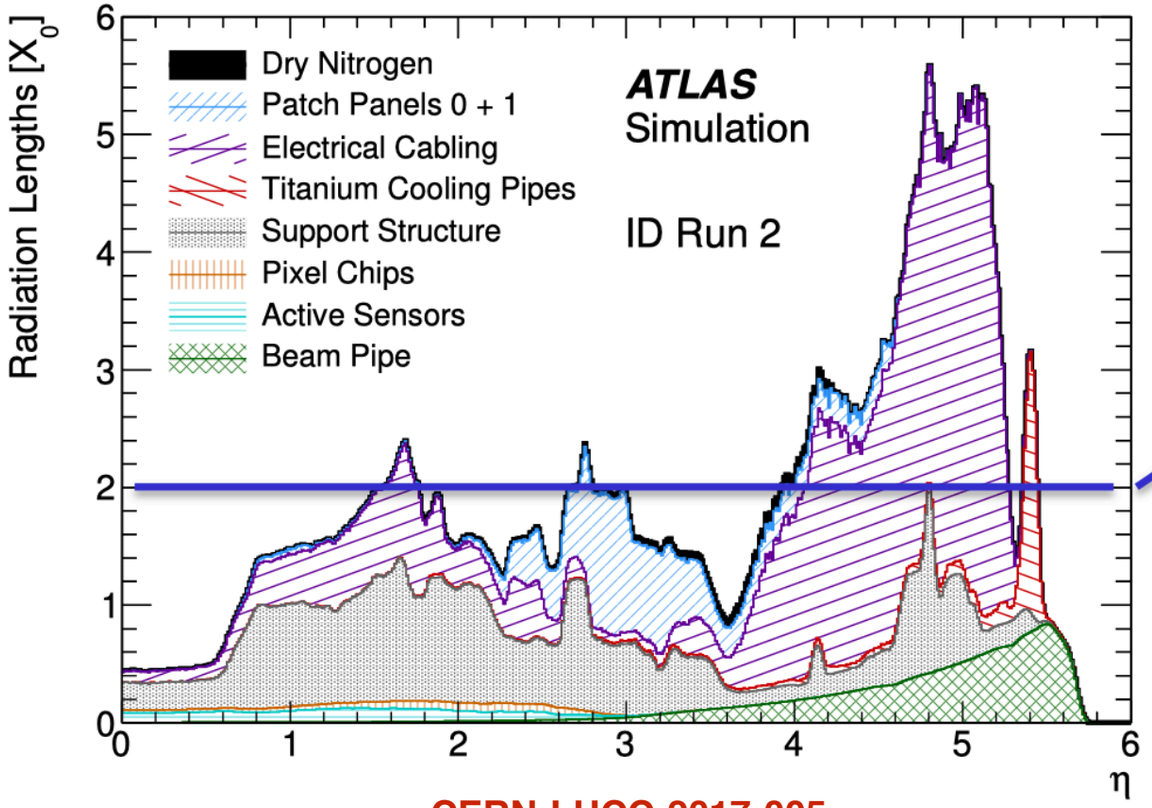


- **In order to improve the present tracking performance in the HL-LHC environment:**
  - Tracking coverage up to |η|<4
  - About 10 times more track density
  - Needs better tracking granularity: occupancy < 10 %
  - Cope with increased readout rates
  - Up to 1 MHz L0 Trigger rate

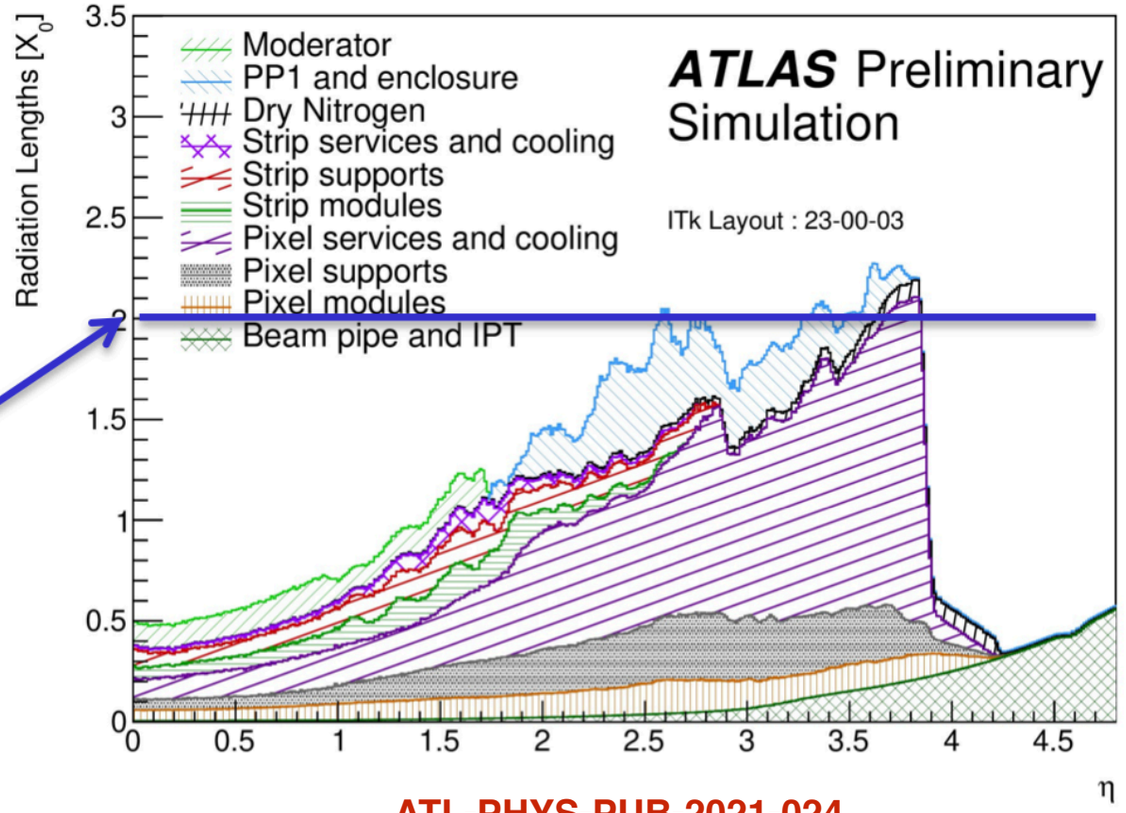
Material Budget

- **Reduction of material budget as much as possible**
  - Evaporative CO_2 cooling system with titanium pipes
  - Light carbon structures (mechanical stability) and rad-hard monitoring
  - Usage of optical links and point of load regulators in Strips
  - Serial powering, 10 Gbps read-out links in Pixels

- **More than factor 2 in forward region vs current ID in Run 2**



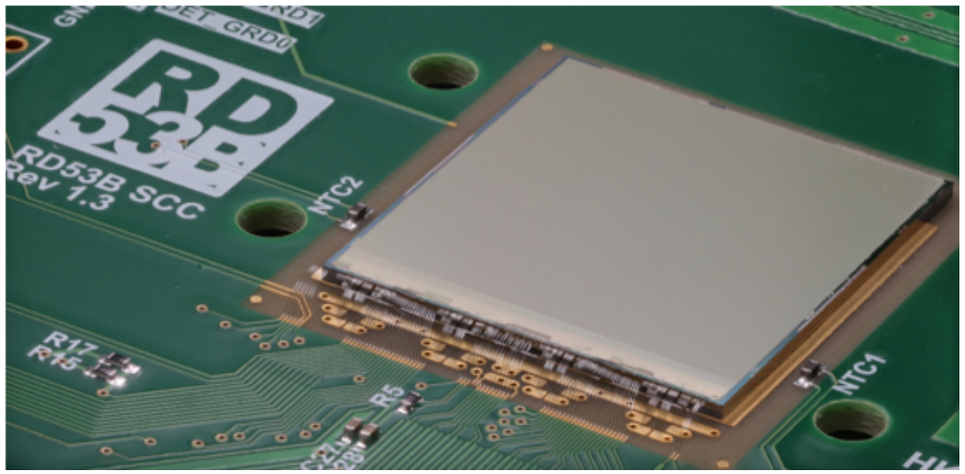
CERN-LHCC-2017-005



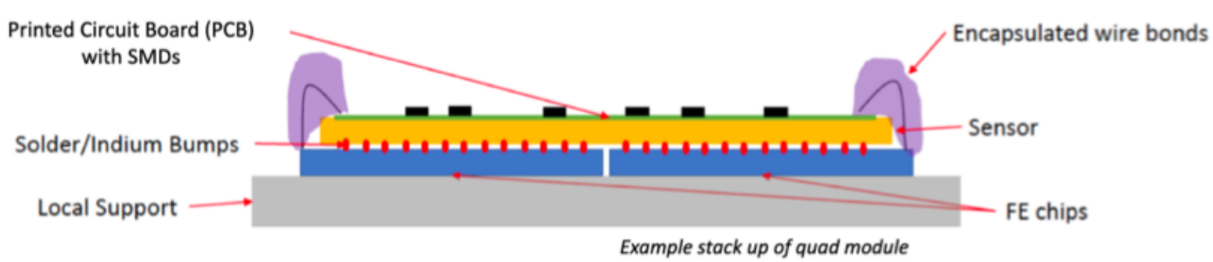
ATL-PHYS-PUB-2021-024

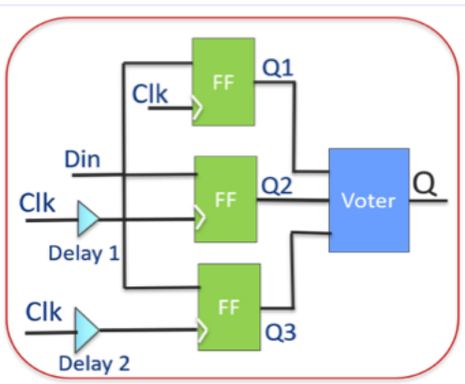
ITK Pixel (RD53)

- **ITk Pixel detector sensors:**
  - 3D-sensors in innermost layer
  - Planar sensors in other layers
- Pixel size 100x25 μm² (innermost barrel), 50x50 μm² (all other layers)
- Data output 4x1.28 Gbps / module



- **RD53: joint effort between ATLAS and CMS**
- RD53A large prototype in 65 nm (half-size)
- Full size chip **ITkPixV1**
  - Produced in 65 nm technology
  - Radiation hard > 5 MGy (10^{16} neq/cm²)
  - Single Event Effects (SEE) hardened





- Pixel configuration registers with Triple Modular Redundancy (TMR)
- Global configuration and state machines in the chip periphery with self-correction
- SEU tests to test register cross-section

- **Submission of ITKPixV2 planned for March 2022**

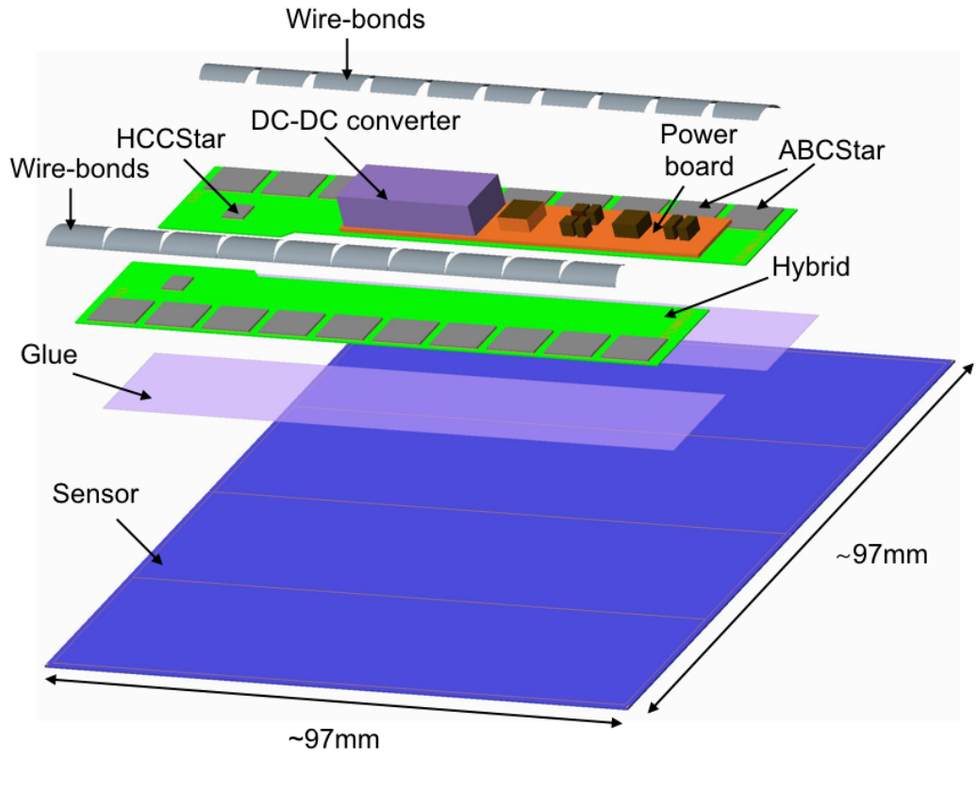
ITk Strips and SEE mitigation

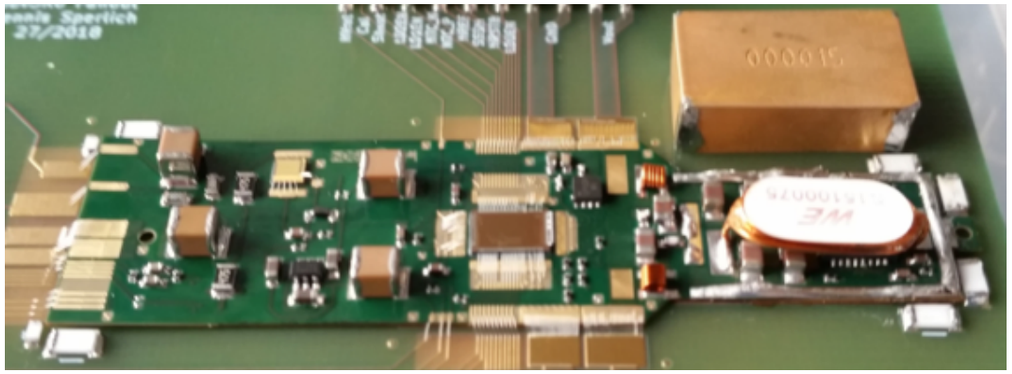
- **8 sensor types (2 barrel, 6 endcap)**
- Strips size: 2 - 5 cm

- **Parallel powering scheme**
  - 14 modules per LV channel
  - Up to 4 modules per HV channel
  - On-module power control and monitoring

- **ABCstar (Front End Chip)**
  - Binary readout
- **HCCstar (FE Interface Chip)**
  - Connects 10x ABC to stave
- **AMACstar (Power Control and Monitoring)**
  - LV power LinPoL12V linear regulator
  - LV power for module BPoL12V DC-DC
  - HV switch using commercial chip

- **All chips made in 130 nm technology**

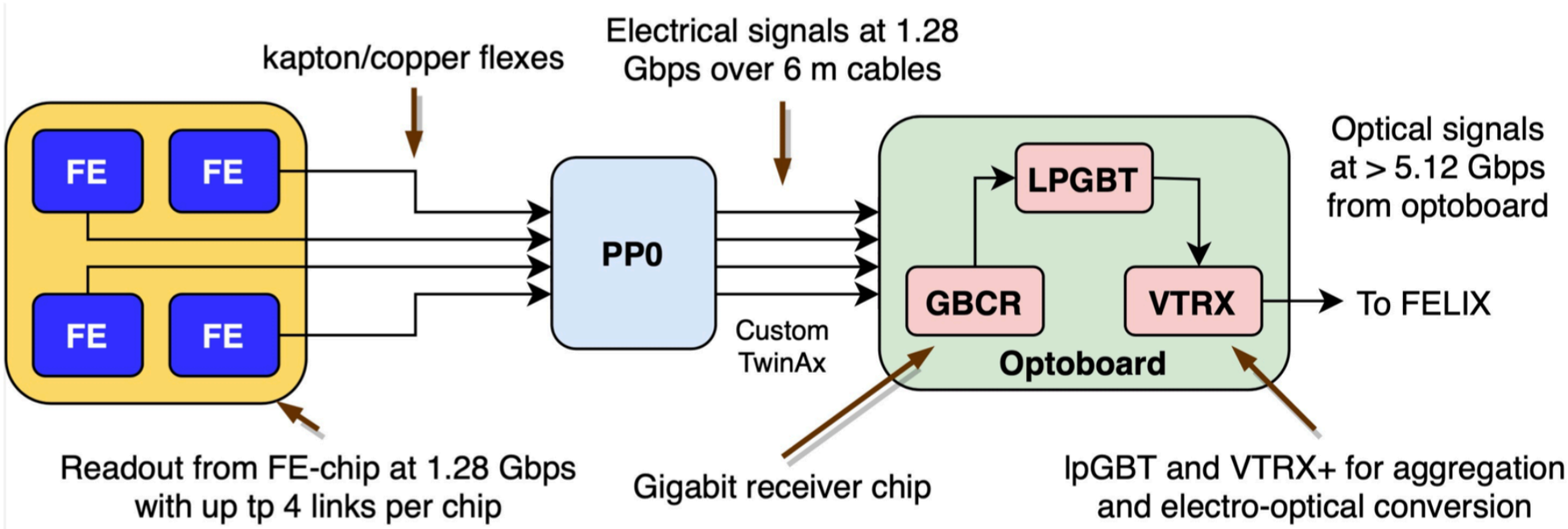




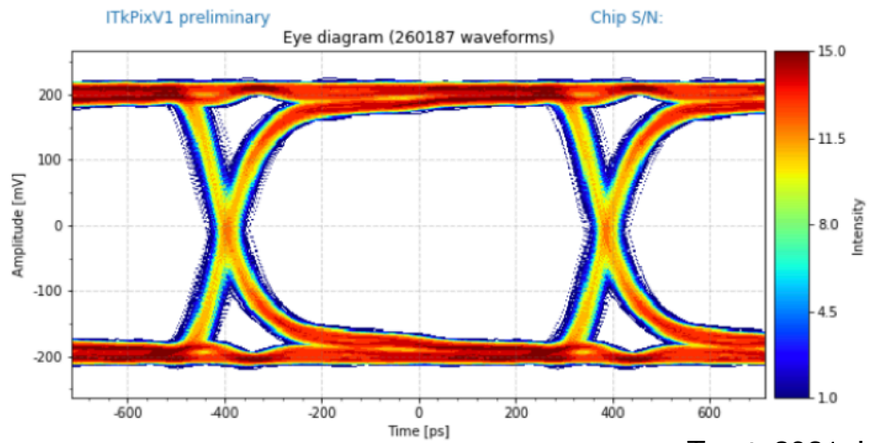
- **SEE measurements have been performed on the current prototype chips**
- Some design faults found and being fixed
- Full triplication of register map and safe control logic

Data transmission

- **Electrical —> Optical signal transmission**
  - Optical transceivers are very sensitive to SEE
  - Placed outside ITk volume
- CERN wide **low power Gigabit Transceiver (lpGBT)** for optical transmission
- Custom Gigabit Receiver Chip (GBCR) recovers the signal for lpGBT



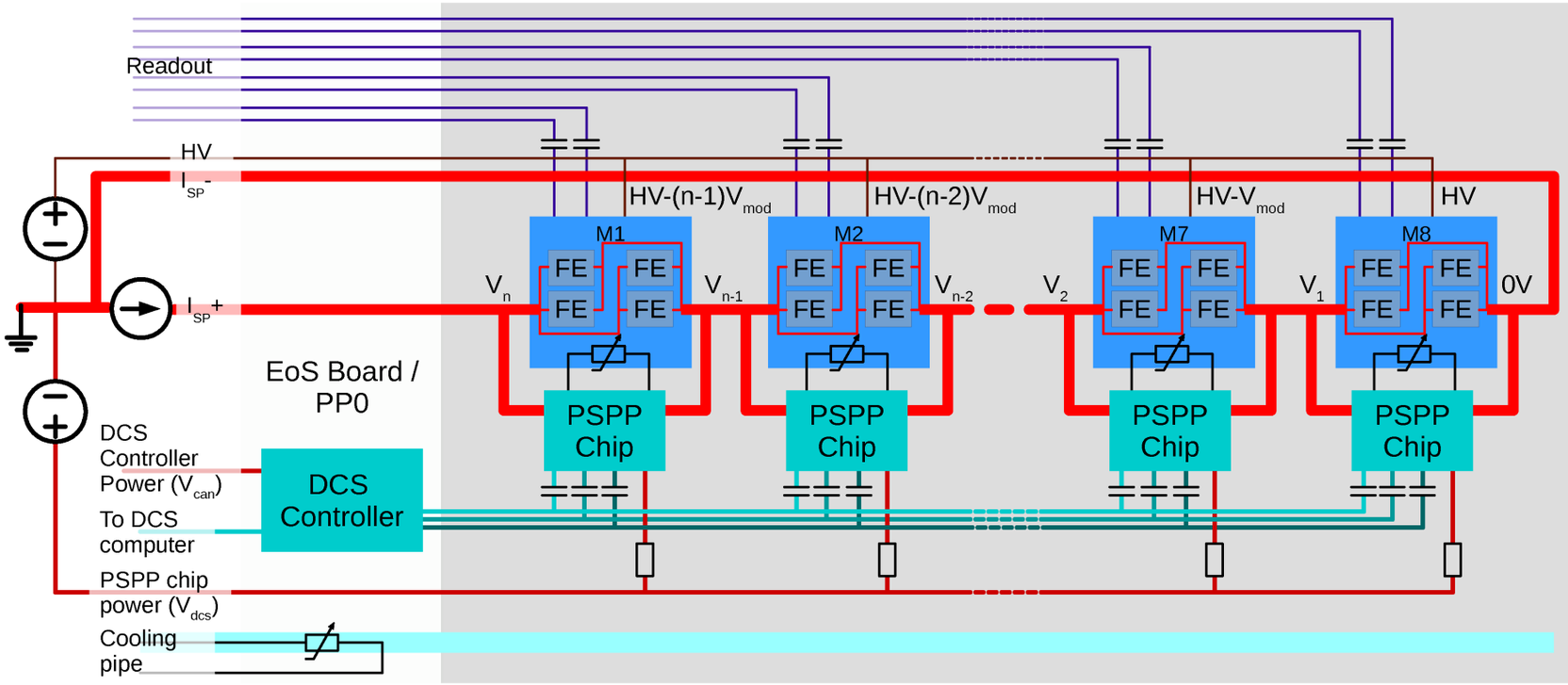
- Data uplinks per FE chip up to 4×1.28 Gbps (up to 16 links on a quad module)
  - Multi-chip data aggregation on a module to reduce number of data links
- **Measurement of peak-to-peak eye opening of 98 ps at the output link**



Trento2021_Loddo

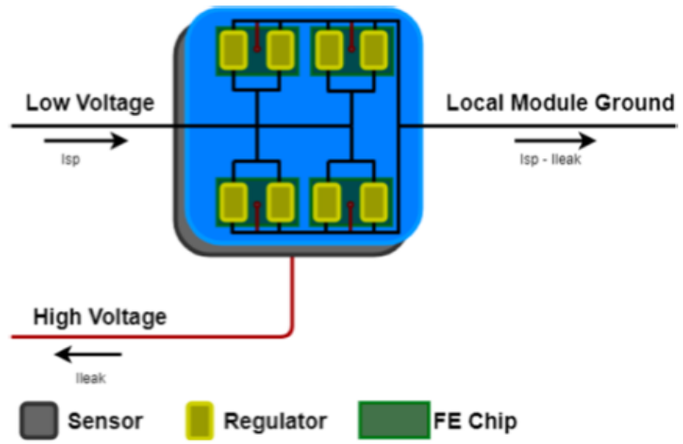
Serial powering

- **Serial powering chain: reduction in cabling and material budget for detector**
  - ITk Pixel modules are connected in series by a constant current source
  - Serial powering chains with 3 to 14 modules are monitored by dedicated chip



CERN-LHCC-2017-005

- **LV inside the module distributed in parallel**



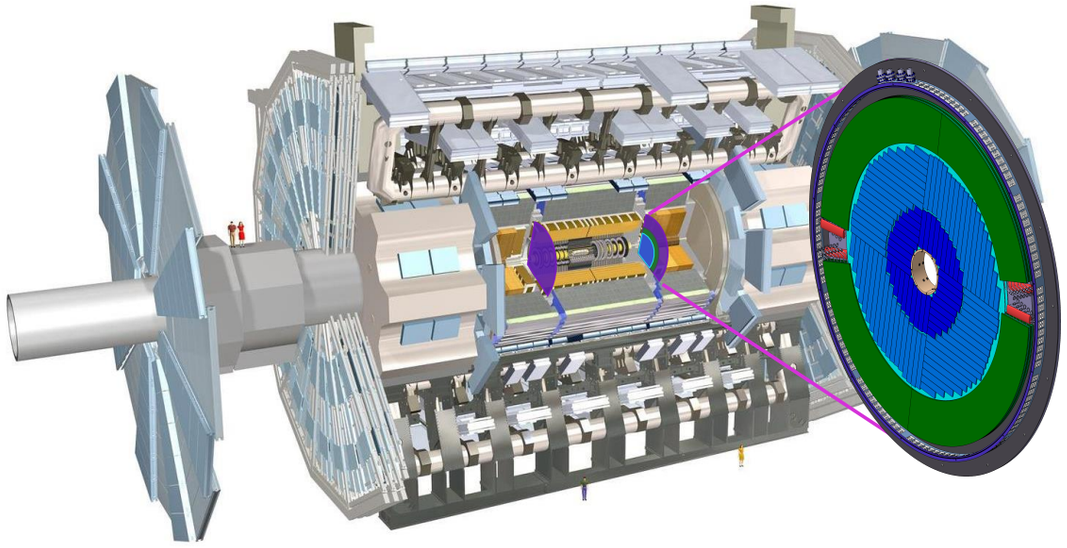
- All module front-ends powered in parallel and regulated by 2 shunt-LDOs (analog, digital)
- Shunt-LDO allow voltage regulation with constant current from the external power source
- Average chain of about 10 modules

High Granularity Timing Detector

- **HGTD:** Active area coverage: **2.4 < |η| < 4.0**

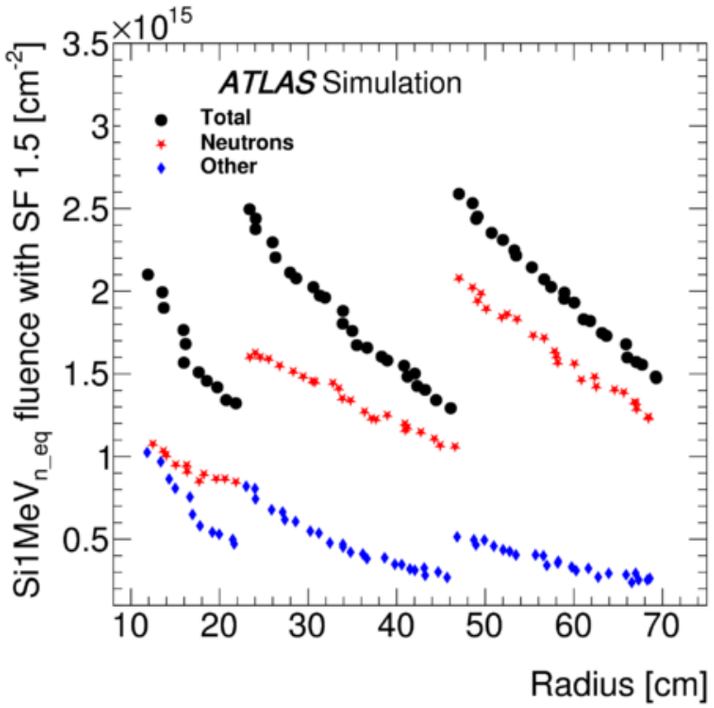
- **Low Gain Avalanche Detectors (LGADs)**
  - **R&D from ATLAS/CMS/RD50**
  - Arrays of 15x15 1.3mm^2 sensors
  - n-p silicon planar detector + multiplication layer
  - Moderate gain ~ 10-50
  - Excellent time resolution < 30 ps pre-irradiation
  - Fast rise time ~ 0.5 ns

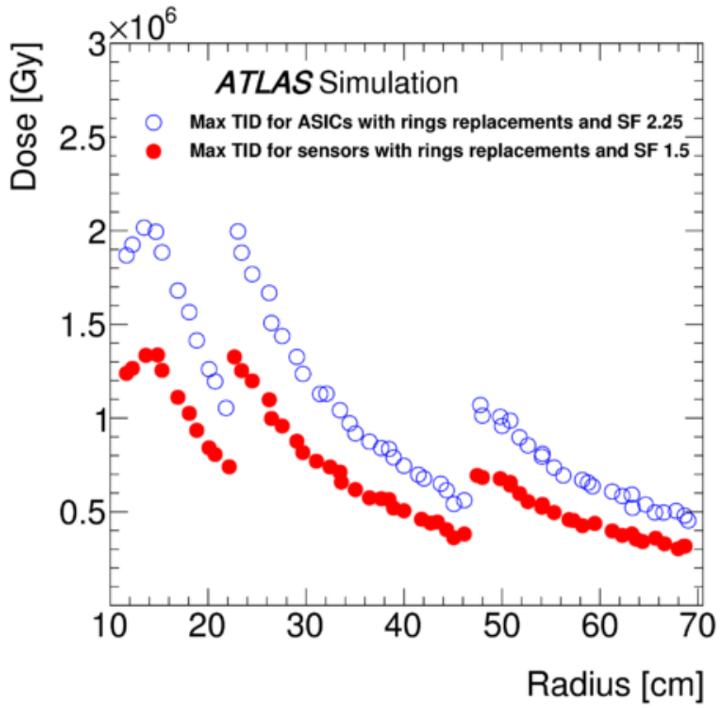
CERN-LHCC-2020-007



- **2 sensors + 2 ALTIROCs (ASICs) per module**

- **Radiation damage is a main concern:**
  - Rad-hard up to 1.5 MGy TID and 2.5 x 10^{15} n/cm^2 NIEL
  - **Replacement of sensor+ASIC**





HGTD: Electronics and read-out

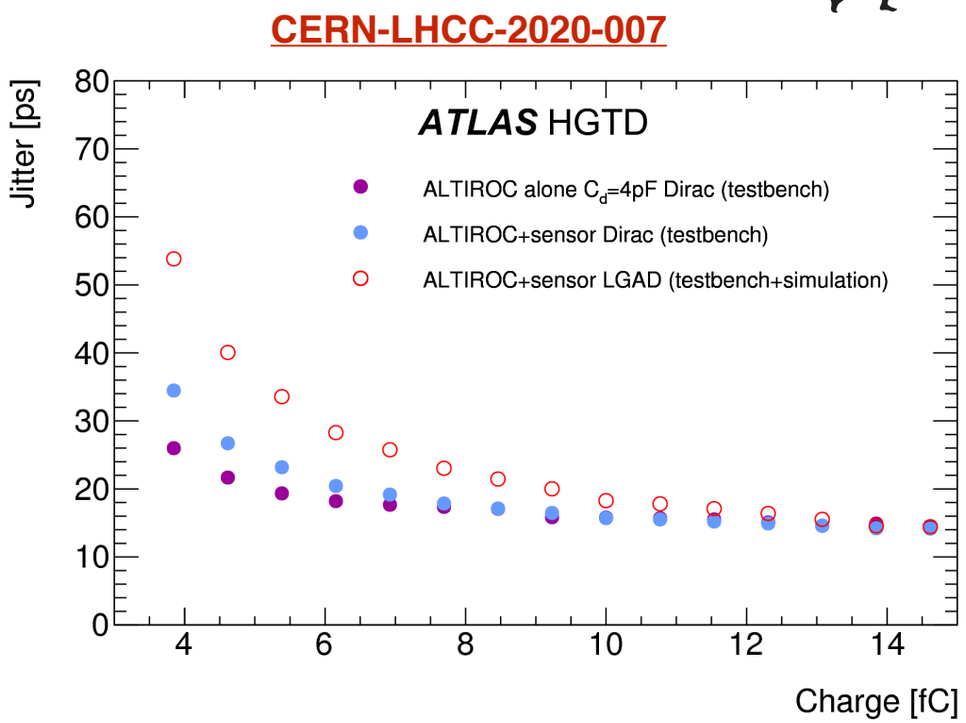
- **ATLAS LGAD Timing Integrated ReadOut Chip (ALTIROC)**
- Submitted in TSMC 130 nm
- Designed for < 5 μA sensor leakage current per sensor pad
- Provide TOA (time-of-arrival) and TOT (time-over-threshold)

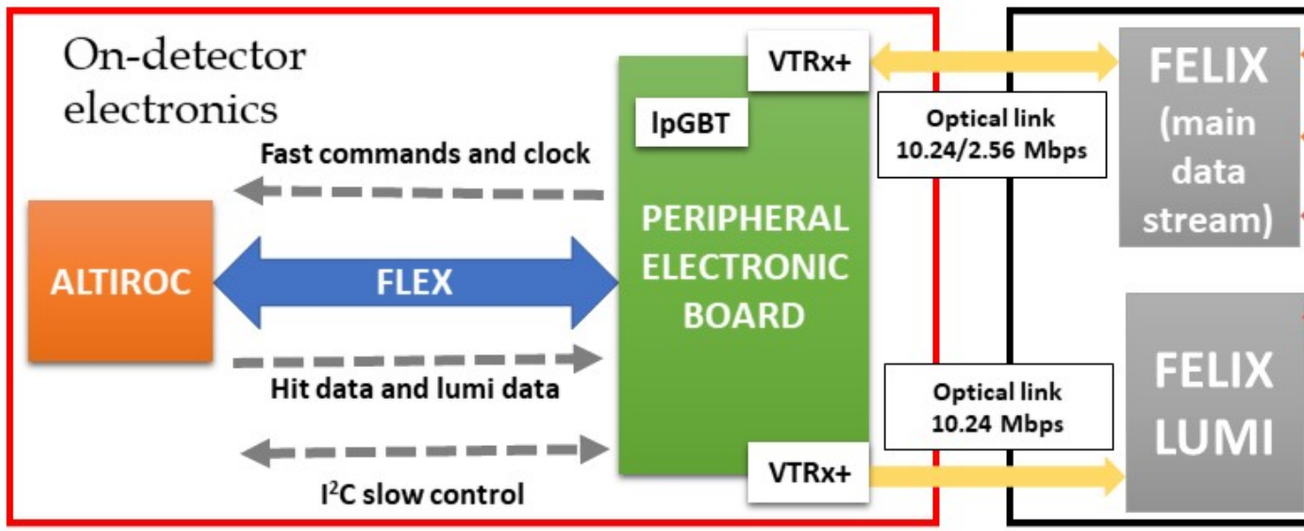
- **Target time resolution < 50 ps at end-of-lifetime**

- **Main data stream and luminosity**
- Radiation studies on-going
  - *May need mitigation strategies*

- **Electric signals to PEB via FLEX**
  - Tight spacing on PEB

- **Bunch by bunch luminosity measurement capability (40 MHz)**
  - Occupancy <—> # of interactions





LAr Calorimeter

Maheyer Shroff's Poster

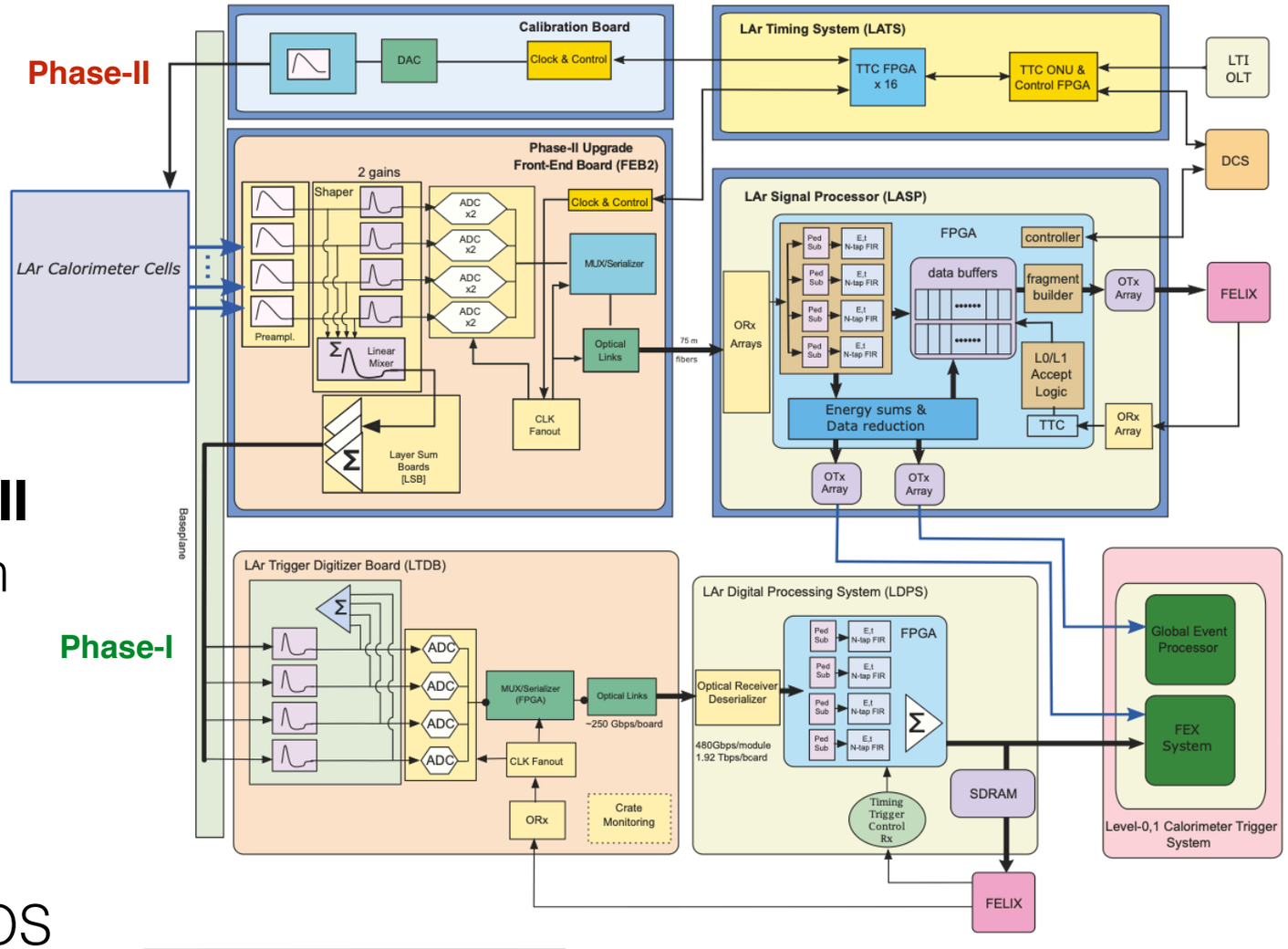
CERN-LHCC-2017-018

- **Main and trigger readout paths:**

- **Trigger** readout is currently being upgraded as part of **Phase-I**
  - *Better E resolution/longitudinal info*

- **Main** readout will be updated for **Phase-II**
  - Calibration ASIC in HV-CMOS 180 nm
  - Replace front-end boards (FEB2) in CMOS 130 nm
    - *Amplification and shaping of calorimeter signals*
  - Full custom 14-bit ADC in 65 nm CMOS
    - Provides digital signals at 40 MHz

- **All analog signals will be digitized and sent off-detector at 40 MHz**



ATL-LARG-PROC-2020-008

- *Tests of phase-II boards on-going*
  - *e.g. LASP*

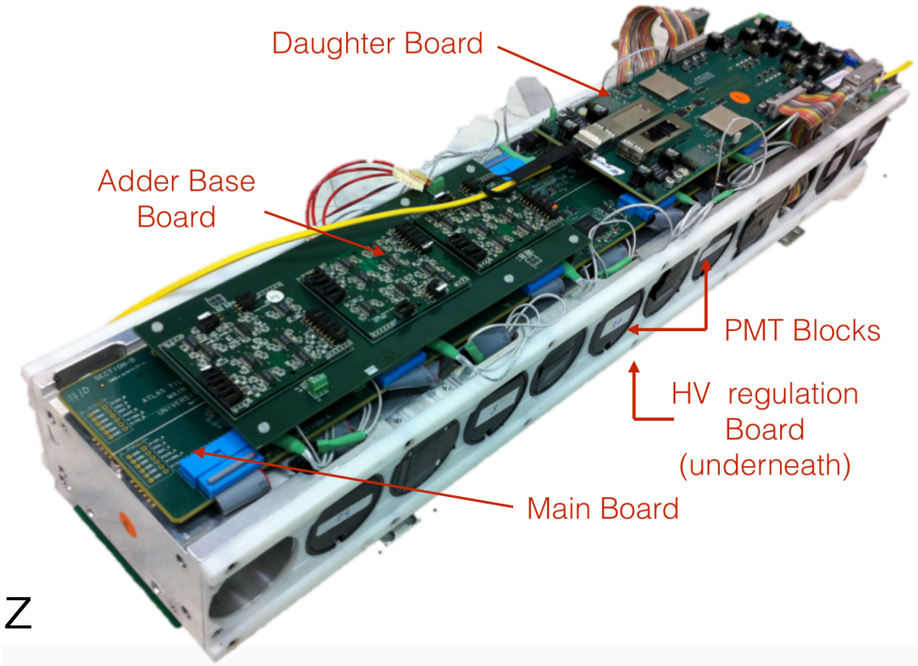
Tile Calorimeter

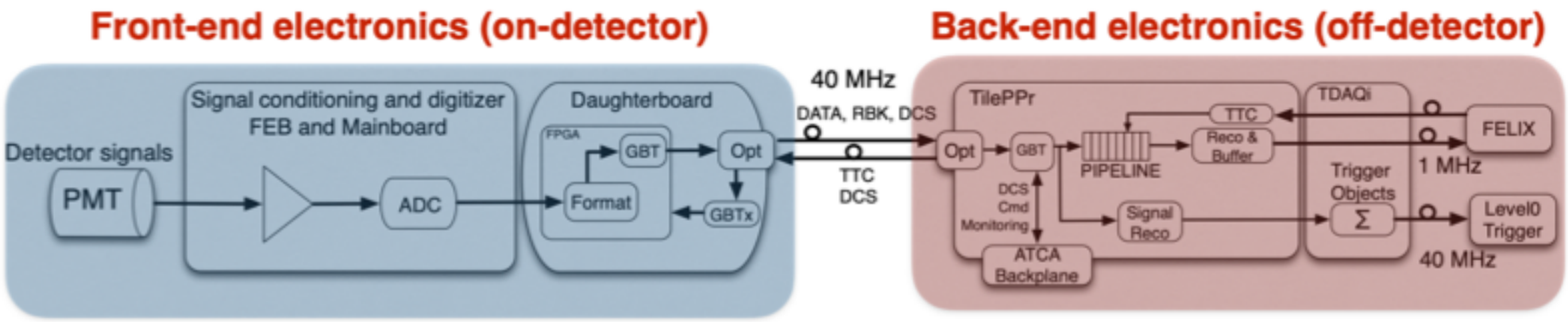
Louis Vaslin's Talk

CERN-LHCC-2017-019

- **Full electronics replacement, both on and off detector**

- **Modular front-end mini-drawers** (4 mini- vs. 1 super)
  - 12 Front-End Boards (FEBs) named FENICS (Front-End ElectroNICS) to shape and condition the PMT signals.
- Need for withstanding higher ambient radiation
- **Some PMT replacement**
  - Light —> electric signals
- **Main board** for continuous digital conversion -> 40 MHz
- **Daughterboard** for LHC timing, configuration, readout



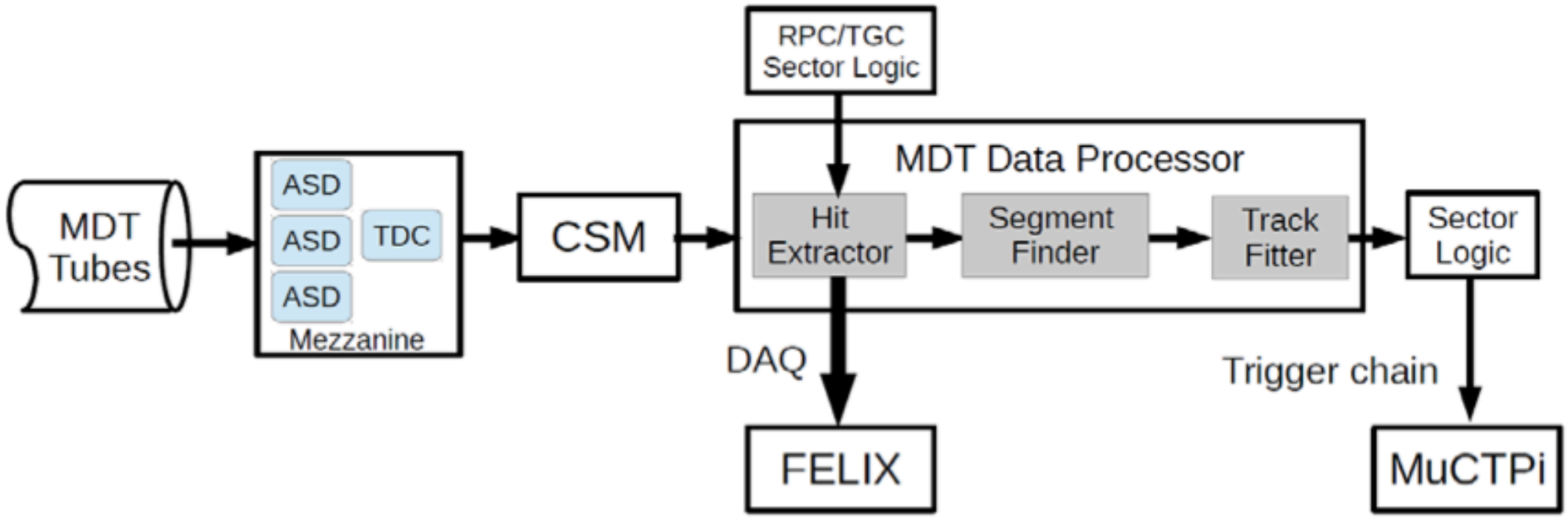


- **Complete redundancy from the cell to the off-detector electronics**
  - Higher radiation levels, improved reliability and robustness of electronics

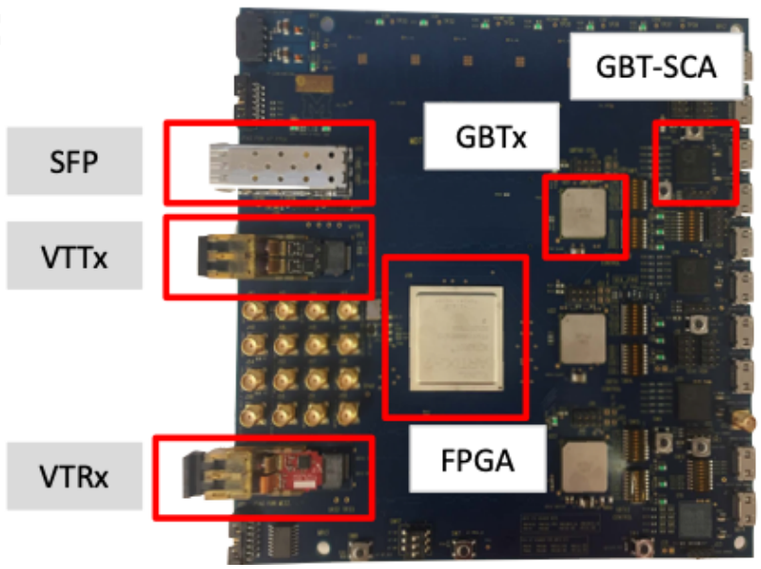
Muon Drift Tube (MDT)

CERN-LHCC-2017-017

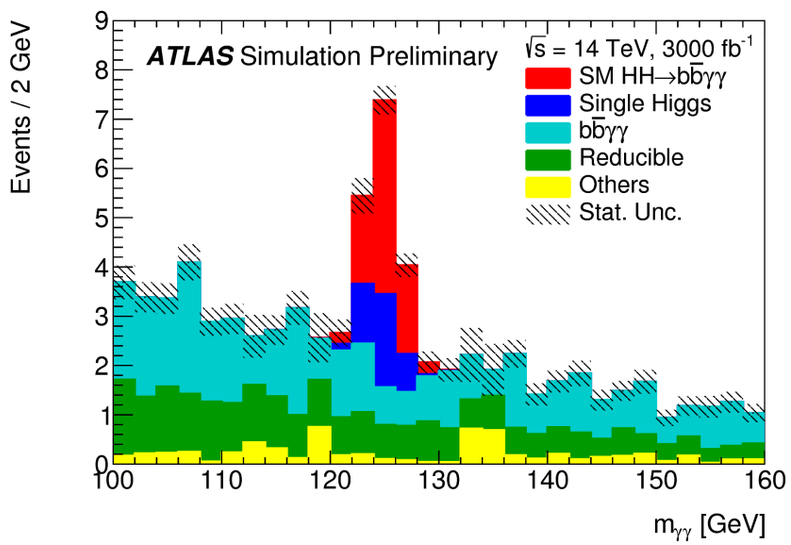
- Improvements to muon transverse momentum resolution at L0
- **Higher rates at HL-LHC: MDT readout electronics upgrade**



- **New front-end electronics testing and prototyping on-going:**
  - New ASD (Amplifier-Shaper-Discriminator) and TDC ASICs on Mezzanine card
    - 130 nm technology
  - New CSM (Chamber Service Module): GBT chipset based
    - lpGBT, GBT-SCA, VTRx



Conclusions and Outlook



- **Challenging HL-LHC environment with <μ> = 200**
  - Physics goals of HL-LHC
- **Trigger + DAQ: L0 only trigger for Phase-II upgrade**
  - FELIX common across all detectors
- **Radiation hardness of electronics vital for ATLAS success up to 4000 fb^{-1}**
  - Implementing robust designs against SEU and SEL, testing of ASICs on-going
  - Specific to all ATLAS front-end ASIC including lpGBT, VTRx, …
  - ITk Pixel and Strip detectors need special care due to proximity of interaction point
- **Global silicon shortage affecting production schedules of all electronics**