ATLAS LAr Calorimeter Commissioning for LHC Run-3

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On behalf on the ATLAS Liquid Argon Calorimeter Group

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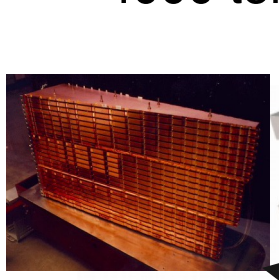
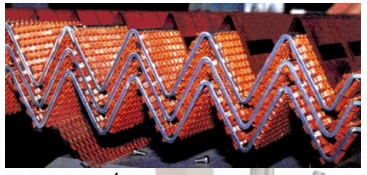
ATLAS Liquid Argon Calorimeter

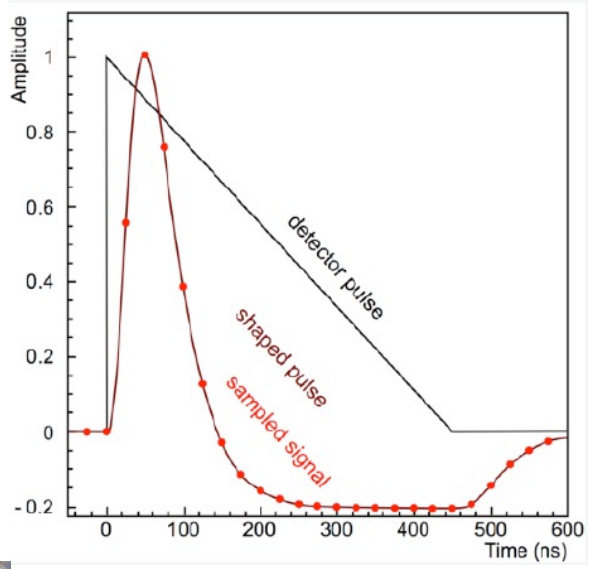
Liquid Argon (LAr) sampling calorimeter

- Energy, time and position of e±, γ, jets
- ~180k cells
- Lead, copper and tungsten absorbers
- 4000 tons

- Sampling calorimeter using cryogenically cooled liquid argon as active medium
- EMB/EMEC calorimeters with accordion-like geometry
- ~5.4k Trigger Towers: group of cells of size $\Delta\eta \times \Delta\Phi = 0.1 \times 0.1$







- Triangular ionization pulse amplified & shaped @ 40 MHz
- FIR filter: compute energy (E-tau and collision timing t-tau) for each bunch crossing (p-p collision)

$$E_T = \sum a_i A_i$$

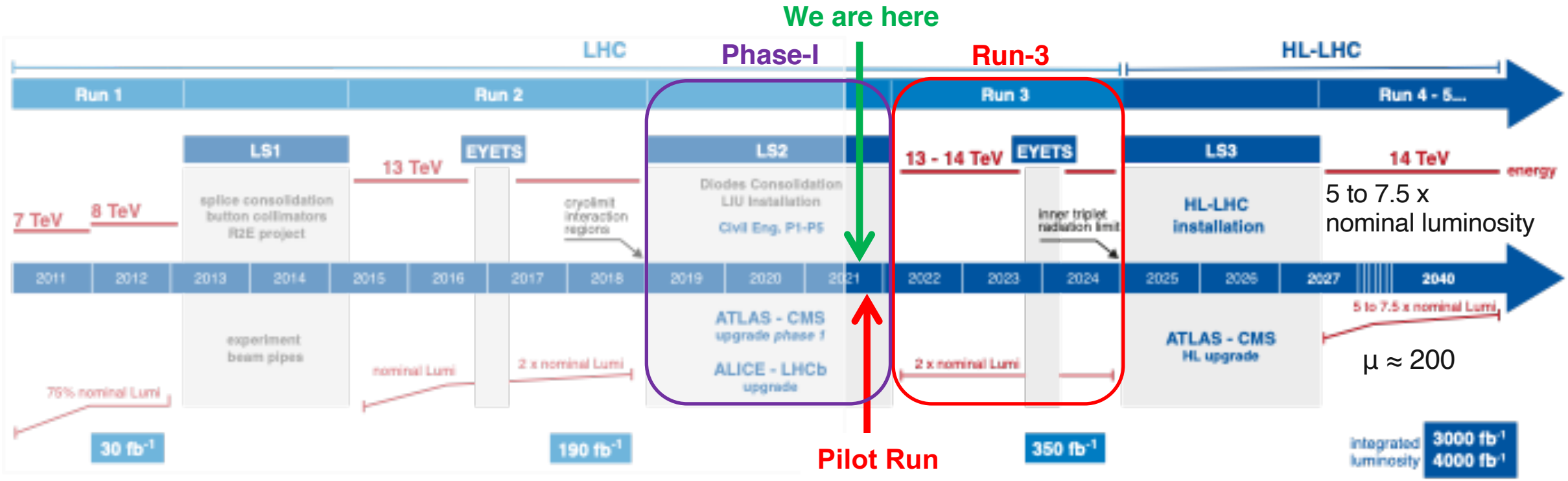
$$\tau_T = \sum b_i A_i$$

a_i, b_i: Coefficients
A_i: Digitized samples

$$\eta = -\ln \tan\left(\frac{\theta}{2}\right)$$

More details in: CERN-LHCC-96-041

LHC / HL-LHC schedule



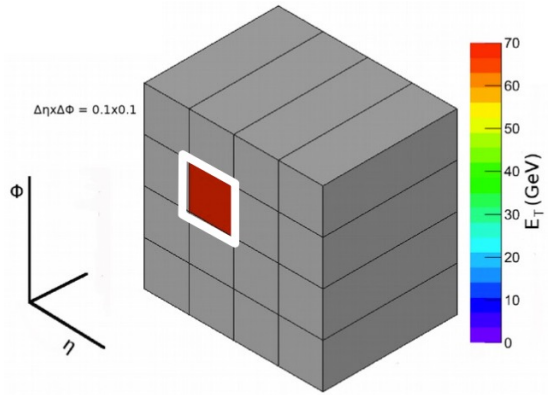
- **Phase-I:** long shut-down (LS2) from 2019 to 2022
  Installation & commissioning of new trigger electronics
- **Pilot Run** in October 2021
- **Run-3** starting early 2022 until 2024
- L1 trigger bandwidth stays at 100 kHz (~20 kHz for $e^{\pm}$)
- Luminosity and pile-out almost doubled

	Run-2	Run-3	Increase
Lumi [10^{34} cm^{-1} s^{-1}]	1.9	3	~x1.5
μ (avg. pile-up)	36	80	~x2
L1 trigger rate [kHz]	100	100	1

LAr Phase-I Upgrade Motivation

- **Why? Old (or "legacy") trigger electronics not designed for higher luminosity & pile-up**
- **Improvement:** Trigger Tower → Super Cells
- ~10 times finer granularity for trigger → Enhanced rejection algorithms → Higher quality data
  Avoid trigger rate going above maximum throughput (120 kHz)

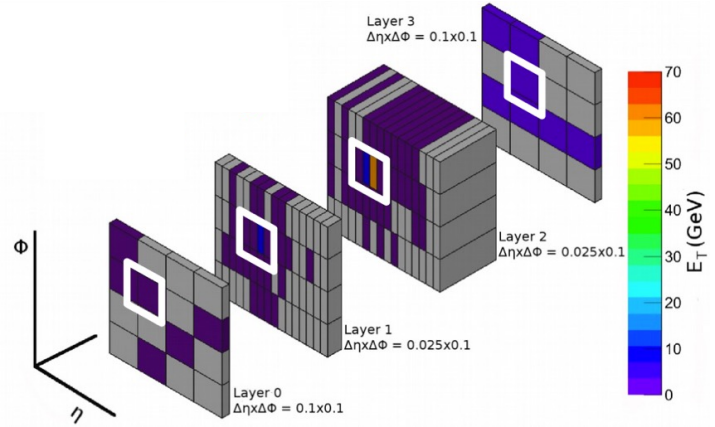
Trigger Towers (TT)



Phase-I Upgrade

Granularity x10

Super Cells (SC)



Simulation of electron with 70 GeV of transverse energy

- No longitudinal segmentation
- Fixed size in Δη × Δφ = 0.1 × 0.1
- Up to 60 cells from 4 layers
- Only **~5.4k TT** from 180k cells
- Analog trigger

- Lateral & longitudinal segmentation
- Increased granularity in Front and Middle to Δη × Δφ = 0.025 × 0.1
- Up to 8 cells from 1 layer
- **~34k SC** from 180k cells
- Digital trigger

Trigger

~5.4k TT for analog trigger

~34k SC for digital trigger

~180k cells for main readout

More details in: CERN-LHCC-2013-017

LAr Electronics Readout

Front End Board (FEB)

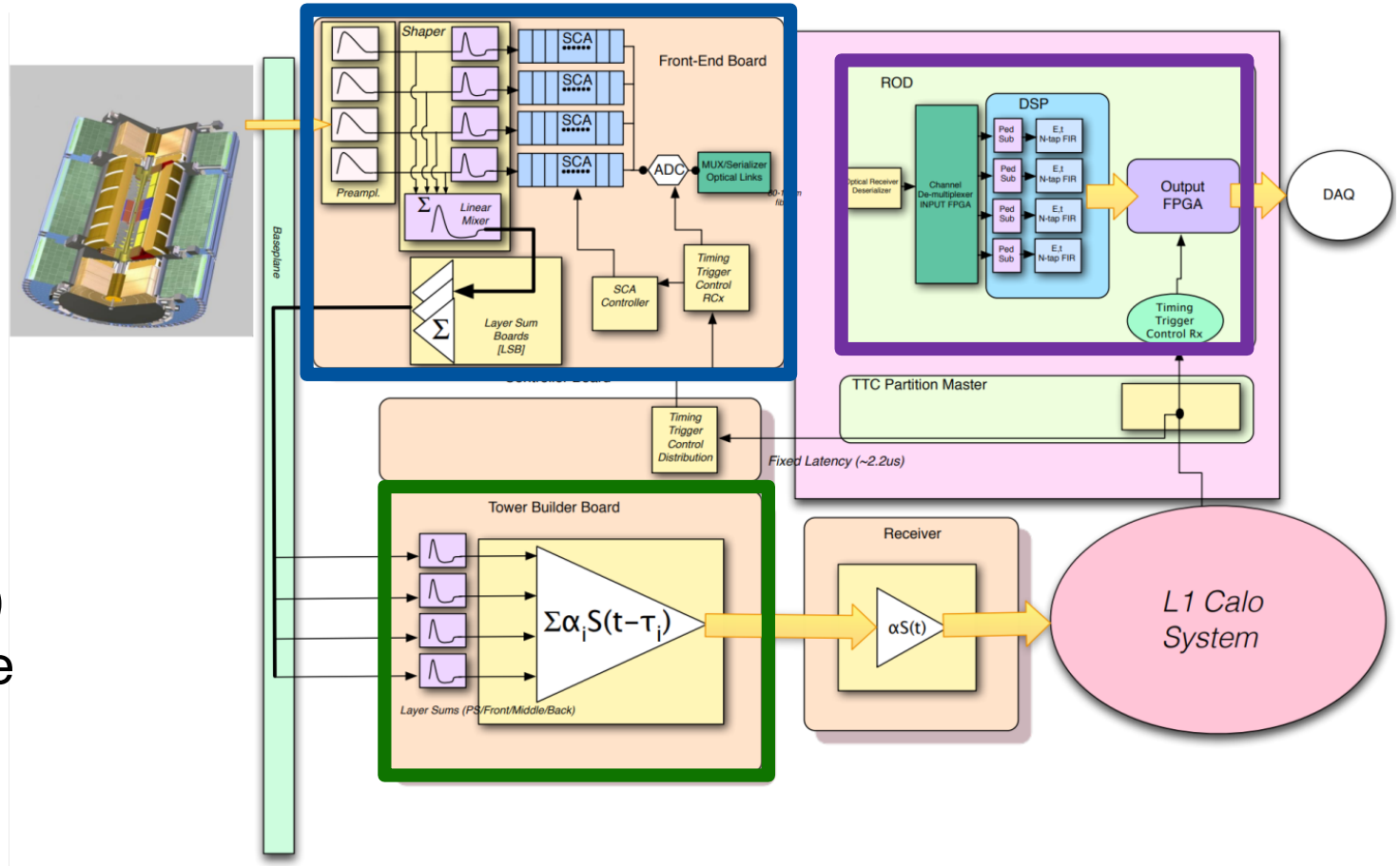
- Amplify, shape, buffer, sample & digitize ionization signals, and transmit them to back-end
- ~128 channels per calorimeter layer (4 layers)
- Analog sums for the trigger prepared by Linear Mixer & Layer Sum Boards (LSB)

Tower Builder Board (TBB)

- Receives analog sums from LSB
- Forms legacy Trigger Tower (TT)
- TT signals are sent to L1A trigger via analog cables

Readout Driver (ROD)

- Receives ADC samples from FEB
- Computes energy (E_C) and time (t_C) for each cell signal at L1 trigger rate



Phase-1 Electronics Readout

Main readout

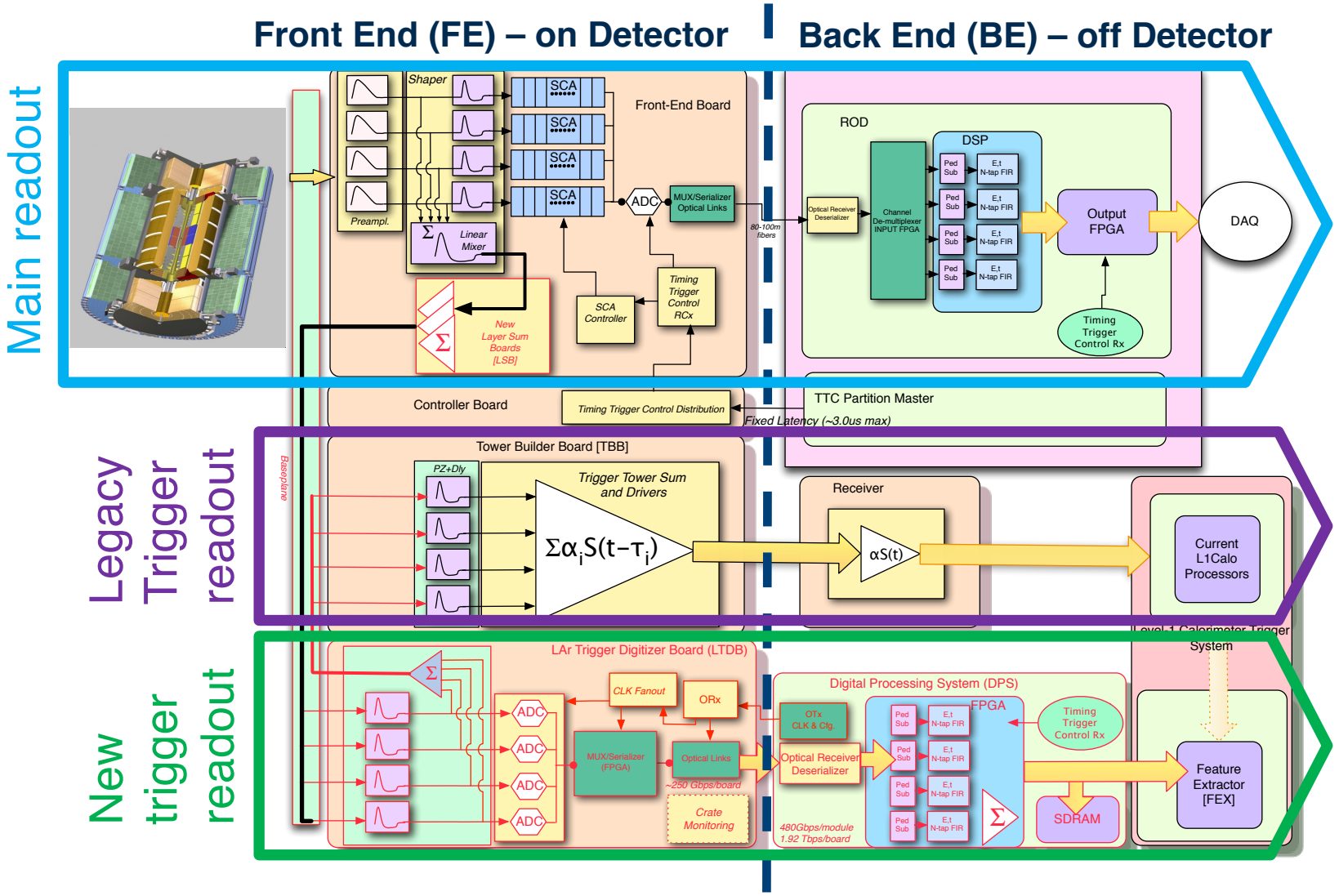
- ~180k channels
- 100 kHz

Legacy trigger readout

- ~5.4k Trigger Towers
- Analog trigger
- Still operational during Run-3

New trigger readout

- ~34k Super Cells
- Higher-granularity (x10 signals)
- 40 MHz
- Will remain operational for HL-LHC



New electronic boards marked in red

New Trigger Readout Electronics

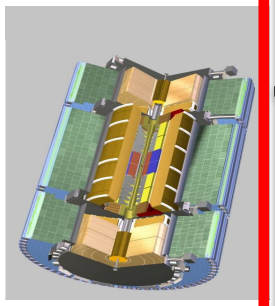
New electronic boards:

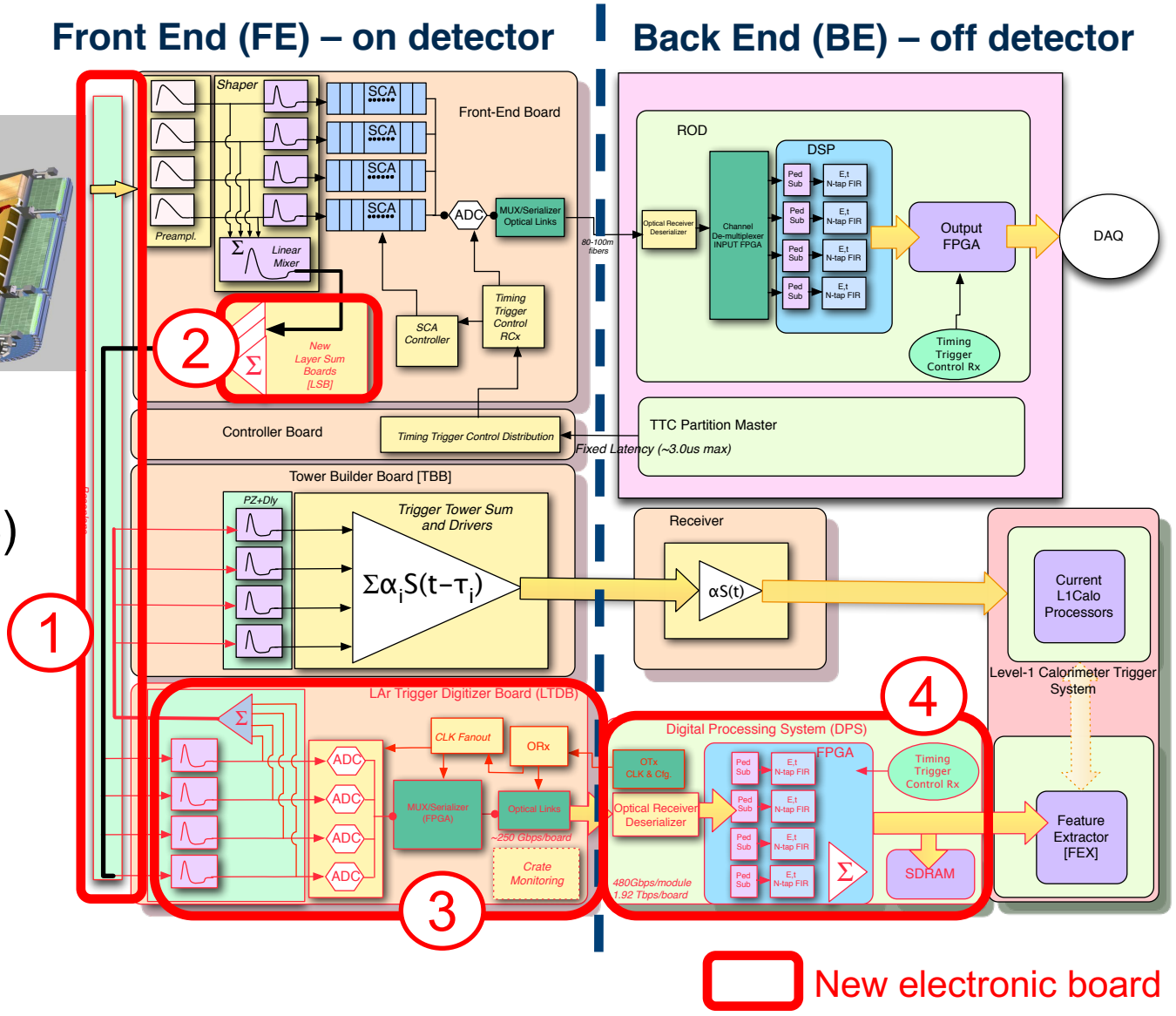
(1) Baseplane

(2) Layer Sum Board (LSB)

(3) LAr Trigger Digitizer board (LTDB)

(4) LAr Digital Processing System (LDPS)





Front-End: Baseplane Replacement

New baseplanes are needed to meet demands of the upgraded system:

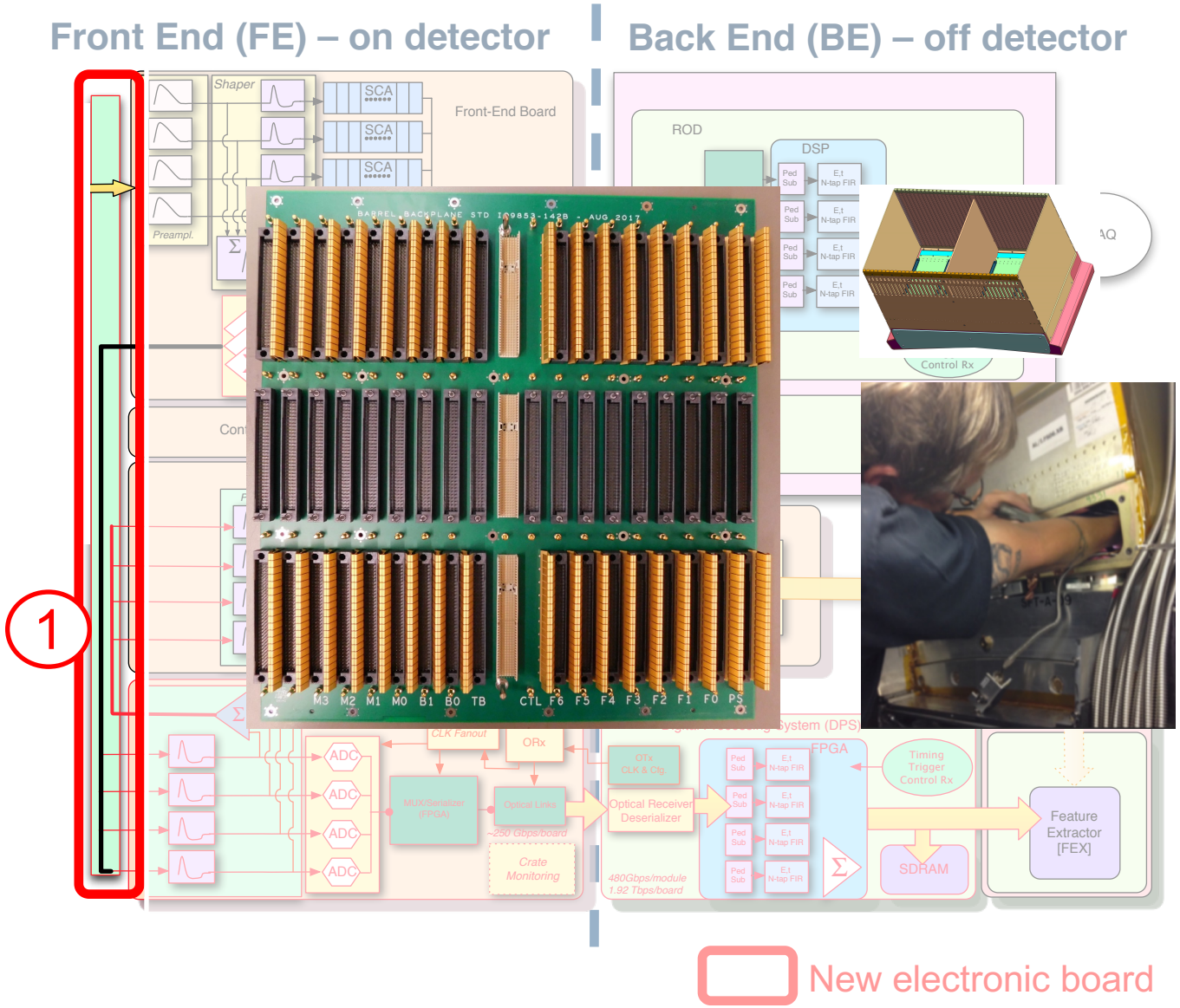
- Channels x10
- Additional slot for the new LTDB
- Operate digital and legacy system concurrently
- Routing SC sums (LSB → LTDB)
- Routing legacy sums (LTDB → TBB)

Replacement is complicated work in a restricted space:

- Requires removal of all boards first

Installation status:

✓ **All baseplanes (114) are complete & installed on detector**



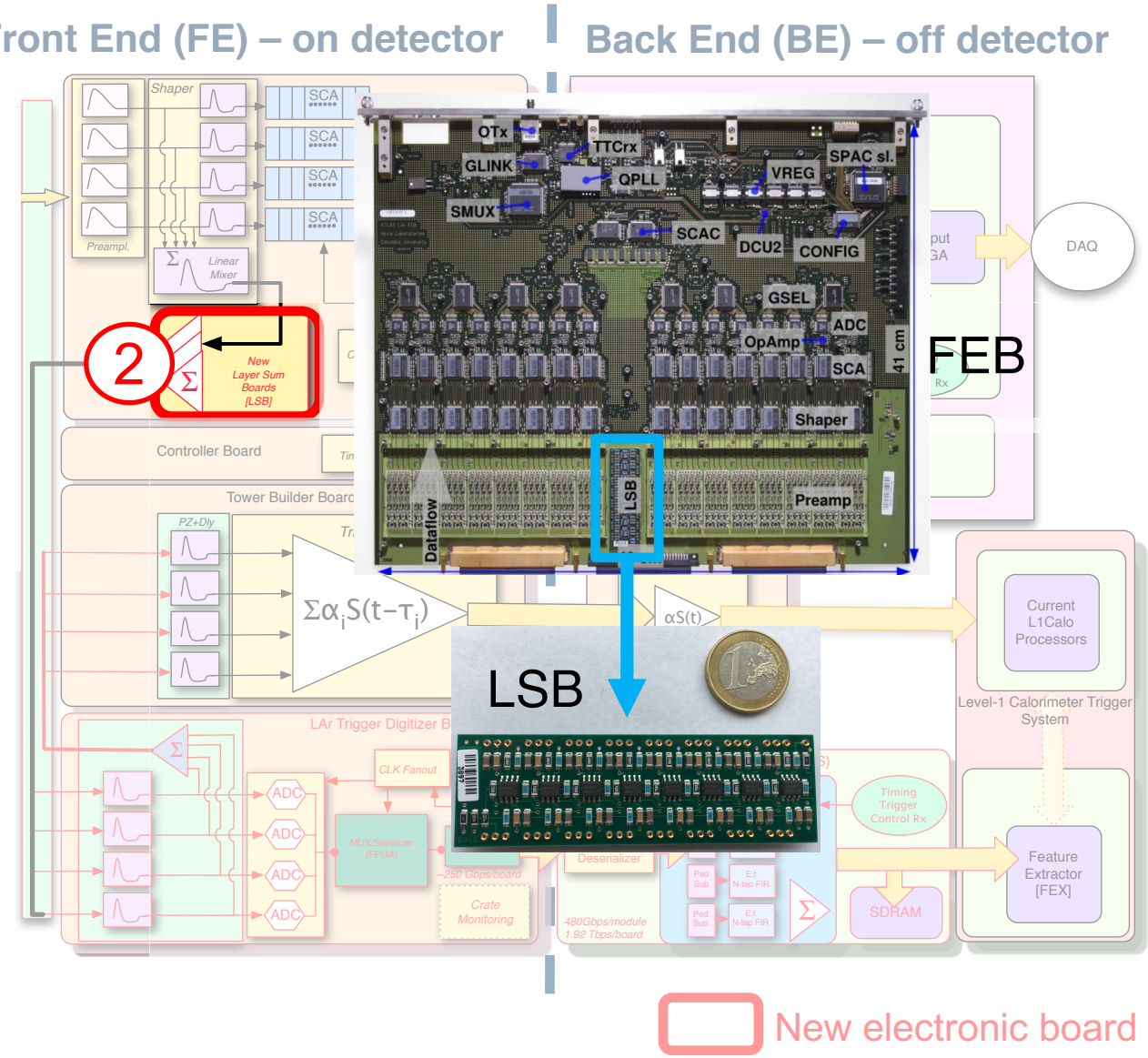
Front-End: LSB Replacement

NEW: Layer Sum Board (LSB):

- Mezzanine card on the FEB
- Sums signals of the calorimeter cells in each layer
- SCs require finer sum than old TTs
  - ⇒ Must exchange LSBs on FEBs
  - ⇒ FEBs must be **taken out** of the cavern to be **refurbished**
  - ⇒ 1524 readout FEBs

Installation status:

- ✓ **All LSB replaced**
- ✓ **All cooling plates, hoses and Low Voltage Power Supplies (LVPS) replaced**



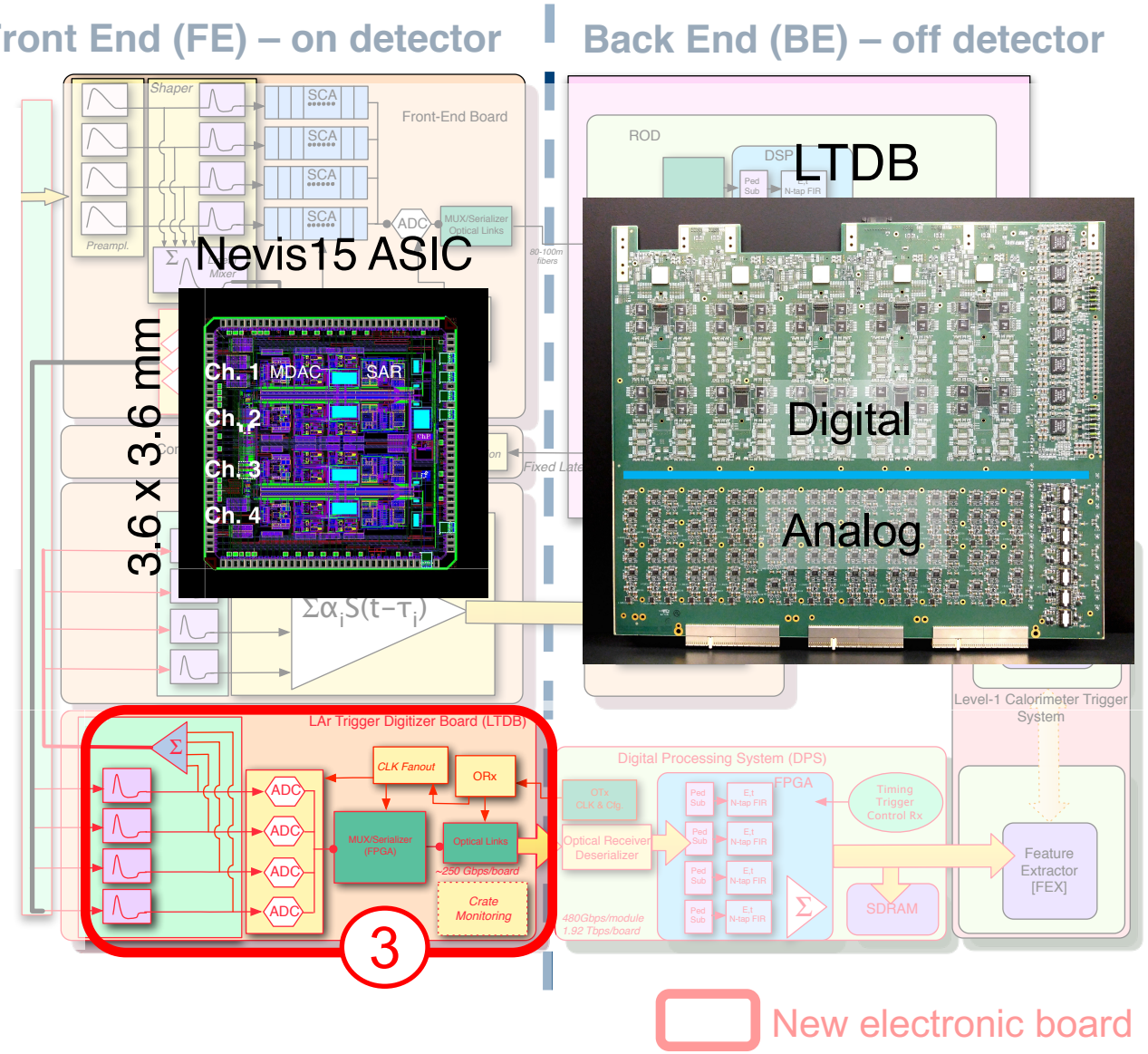
Front-End: LTDB Installation

NEW: LAr Trigger Digitizer Board (LTDB):

- Custom radiation-hard ASICs and high-performance ADC (40 MHz)
- Processes and digitizes up to 320 SCs, sends them to digital processing system (DPS), and reroutes layer sums to legacy trigger path
- 124 LTDBs, 7 “flavors” depending on the location: 1 for barrel, 6 for end-cap
- 40 fibers, 8 SC per fiber @ 5.12 Gbps

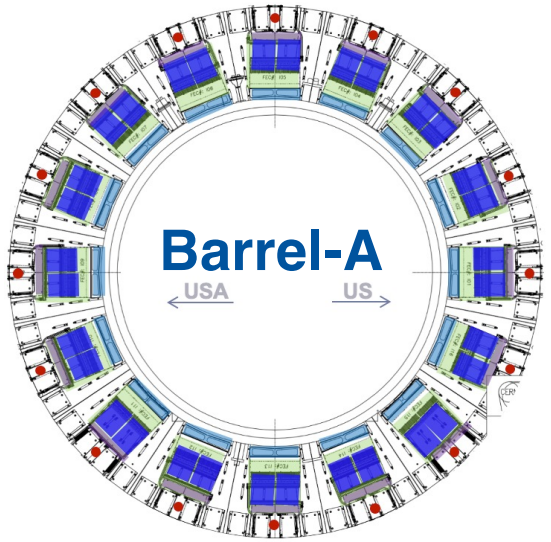
Installation status:

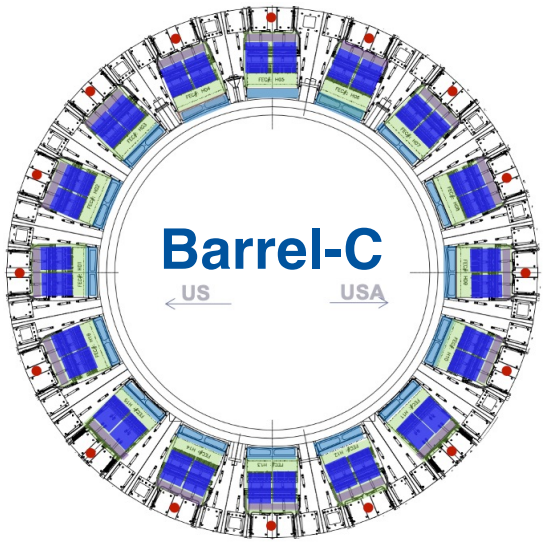
- ✓ **All LTDBs are installed and connected**
- ✓ **Power Distribution Boards (PDB) replaced in order to increase clearance to ease insertion of LTDBs in FE crates**

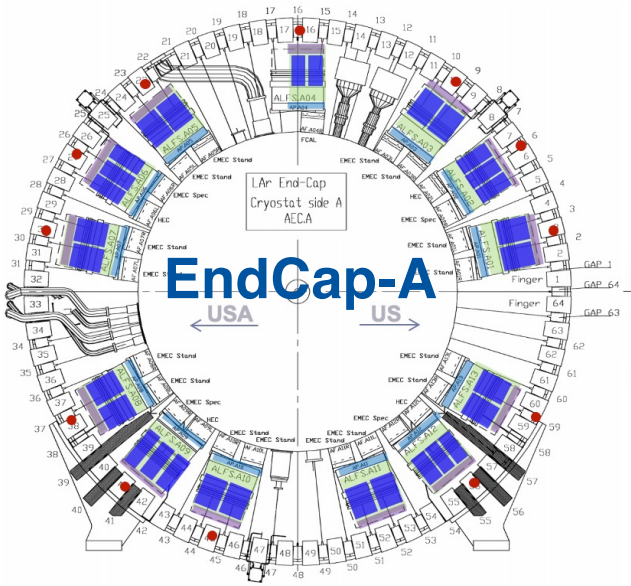


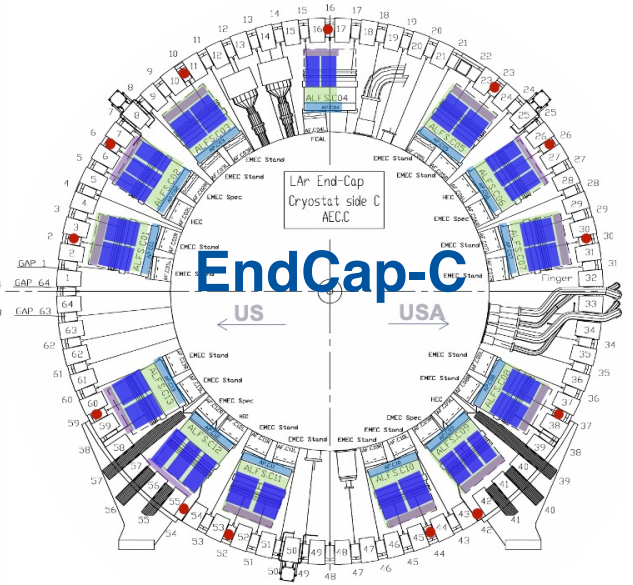
Front-End: Installation Status

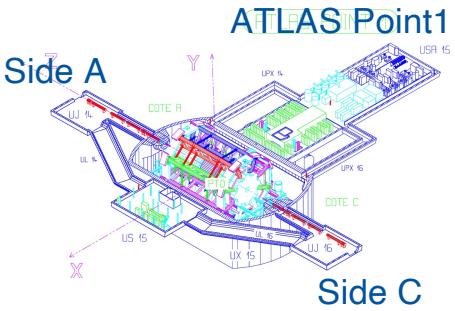
- ✓ All crates baseplanes and FEB boards refurbished and reinserted
- ✓ All LTDBs are installed and connected











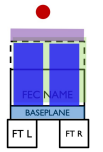
Baseplane exchanged

Re-cabled for commissioning

FEB boards reinserted

LTDB installed, commissioning

Cooling refurbished



Fully Done

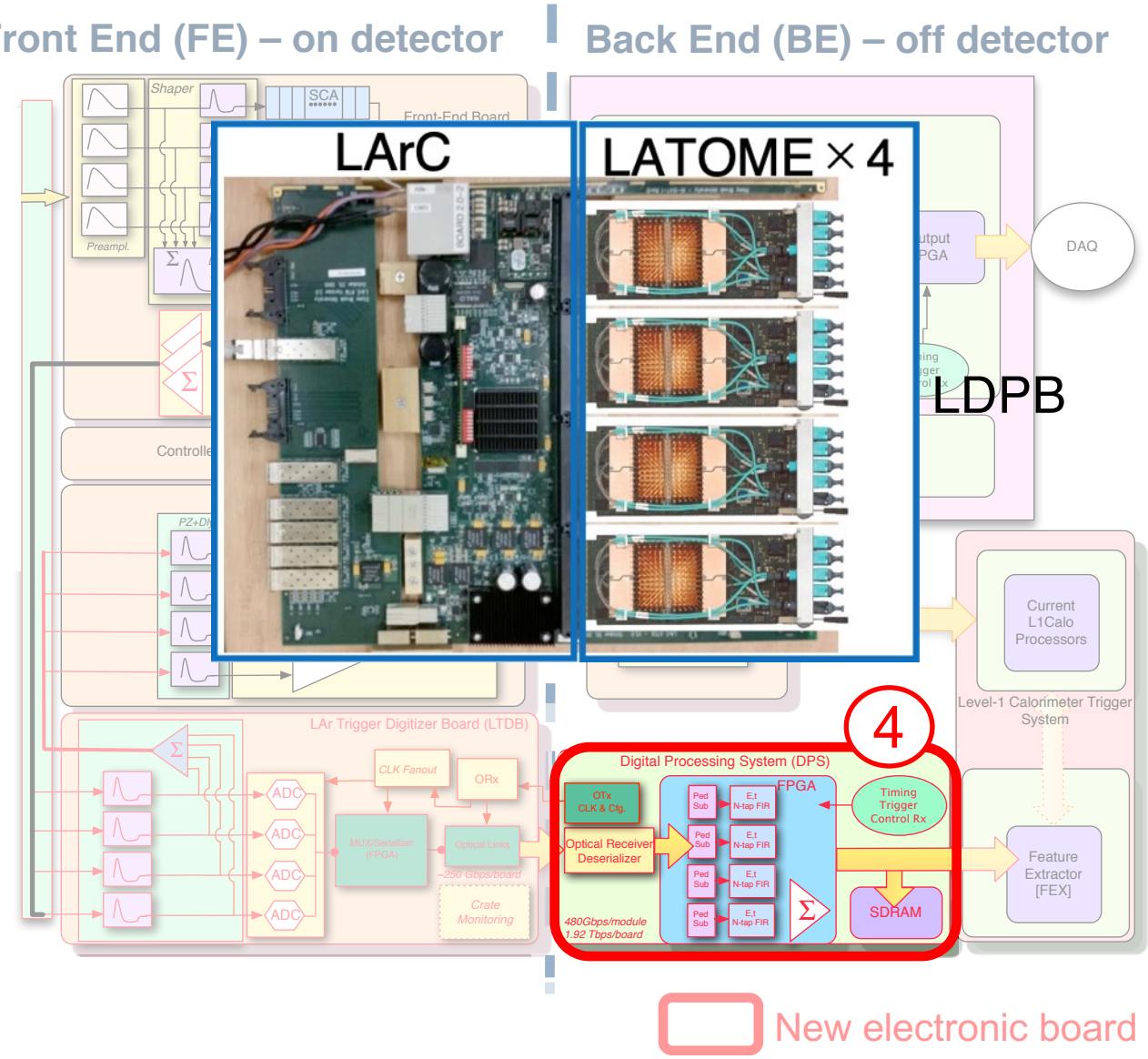
Back-End: LDPB Installation

NEW: LAr Digital Processing Blade (LDPB):

- System receives ADC values from LTDB (~25 Tbps, 40 MHz) and transmits energy values to L1Calo Trigger (~41 Tbps, 40 MHz)
- Composed of 30 blades, each hosting 4 LAr Trigger prOcessing Mezzanines (LATOMEs) over one LAr Carrier (LArC)
- Operated by commercial FPGAs:
  - ⇒ LATOME → Intel® Arria® GX 10
  - ⇒ LArC → Xilinx Virtex-7
- **Main goals:** reconstruct super cell E_T, identify bunch crossing ID and correct baseline
  - ⇒ Strict latency requirements (< 375 ns) and pulse phase algorithms (5-6 bunch crossing)

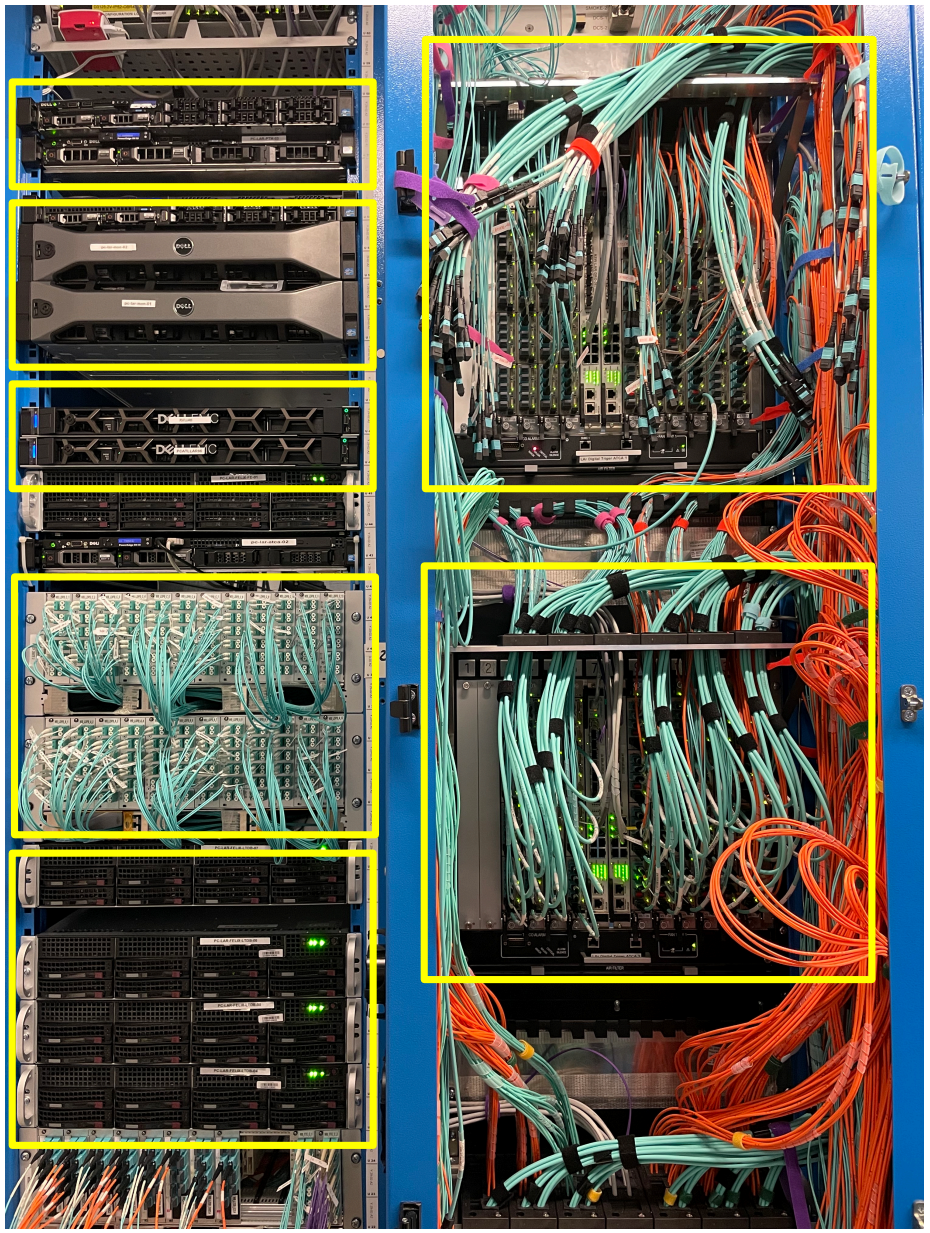
Installation status:

- ✓ **All LDPBs installed in ATCA crates**
- ✓ **All LATOMEs connected to LTDBs**



Back-End: Installation Status

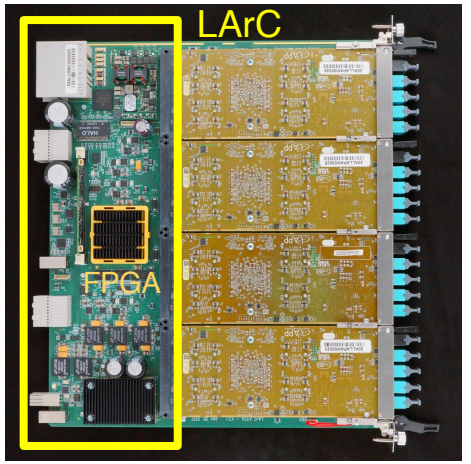
- ✓ All LDPB installed in 3 ATCA crates
  - ⇒ 10 LArC per crate
  - ⇒ LArC are grouped by readout regions
- ✓ All fibers from LTDB to LATOME connected
- ✓ All network/TTC/TDAQ readout connections done
- ✓ Monitoring and control system in place (included in ATLAS control)

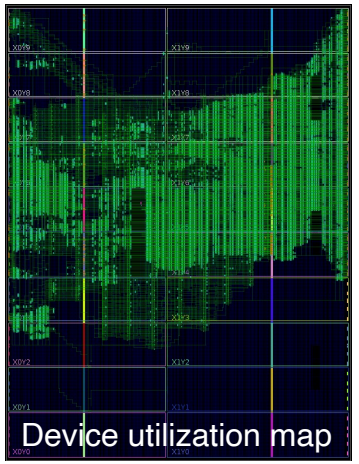


Back-End: LArC FW Status

LAr Carrier (LArC):

- Custom board operated by Xilinx Virtex-7 FPGA
- Main functionality:
  - ⇒ ATLAS global monitoring readout (MGT)
    LTDB → LATOME → **LArC** → FELIX (TDAQ)
  - ⇒ Local monitoring readout (10 GbE)
    LTDB → LATOME → **LArC** → Local PC
  - ⇒ Provide Trigger, Timing and Control signals to LATOMEs (LVDS)
  - ⇒ Low level control and monitoring (1 GbE, IPbus)



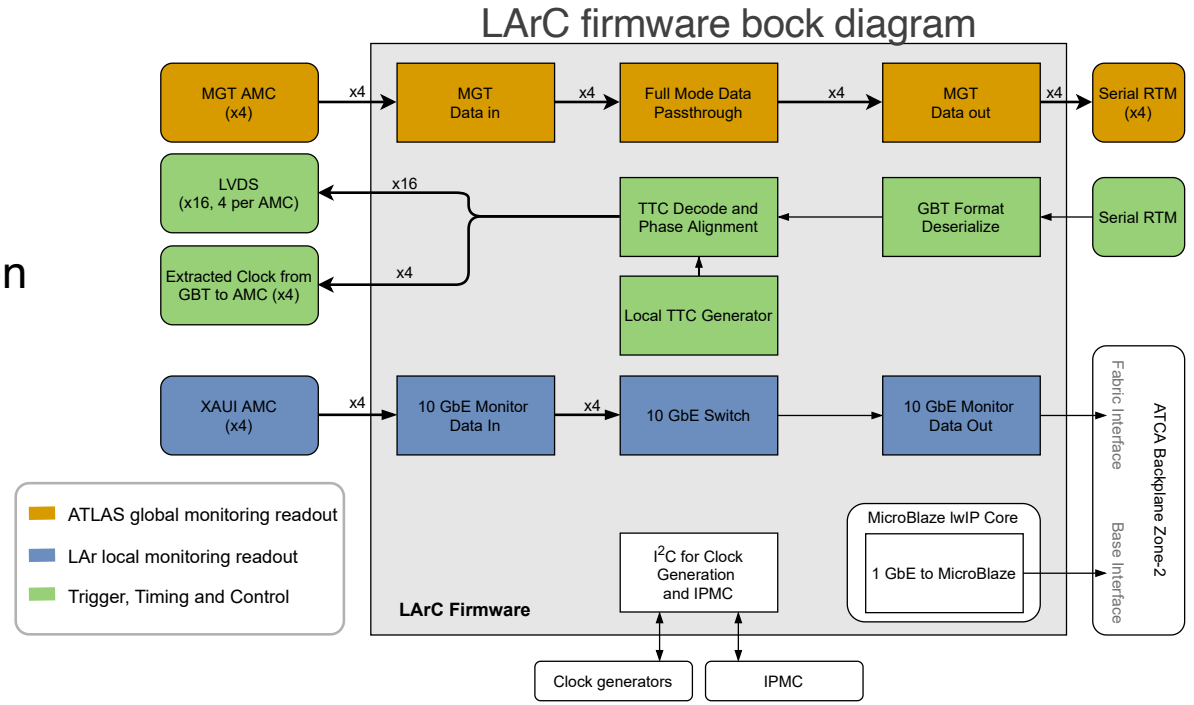


FW releases verification & validation

- Several tests available to validate FW requirements
  - ⇒ First, verification (simulation)
  - ⇒ Second, validation (in target)
- Effort ongoing to automatize FW validation & regression using GitLab Continuous Integration (CI)

Firmware status:

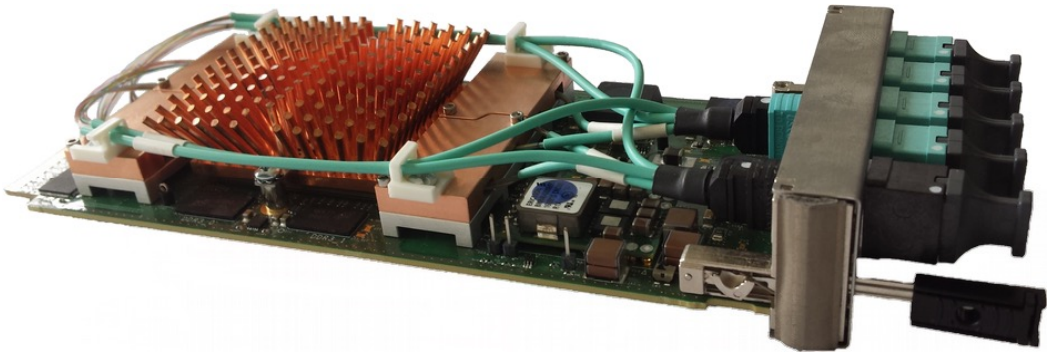
- ✓ **All relevant functionalities are in place**
- ✓ **Logic comfortably fits in the device**
- ✓ **Latest FW version is stable and ready for operation with first beam**



Back-End: LATOME FW Status

LAr Trigger prOcessing MEzzanine (LATOME):

- Custom board operated by Intel® Arria® GX 10 FPGA
- Main functions:
  - ⇒ Receive up to 48 high speed input links from LTDB at 40 MHz
  - ⇒ Reconstruct super cell E_T and identify bunch crossing ID
  - ⇒ Transmit results to Level-1 trigger system (FEX) at 40 MHz
  - ⇒ Process, buffer & transmit data to TDAQ and local PC upon L1A



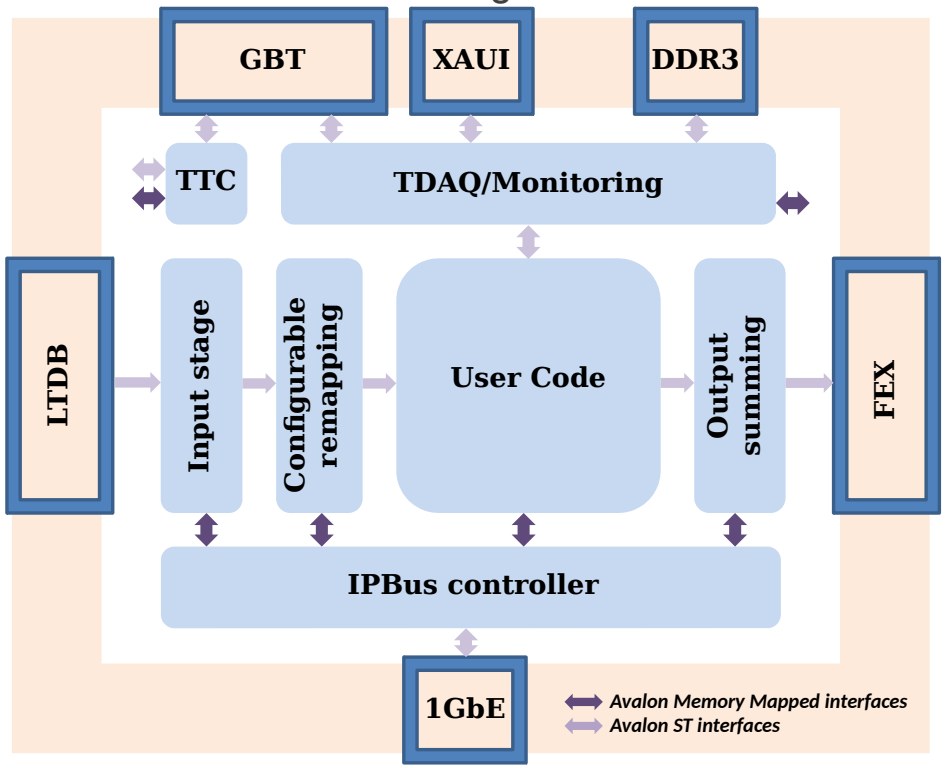
FW releases verification & validation

- FW validation & regression using GitLab CI
- Several automatic tests available, effort ongoing to implement more tests to validate all the requirements

Firmware status:

- ✓ **Logic utilization is high → challenging to close timing**
- ✓ **Ongoing effort to re-design failing paths to meet timing (problems are already located and being solved)**
- ✓ **Trimmed version based on requirements used for commissioning**
- ✓ **Reduced version available that can be used for operation with first beam**

LATOME firmware bock diagram

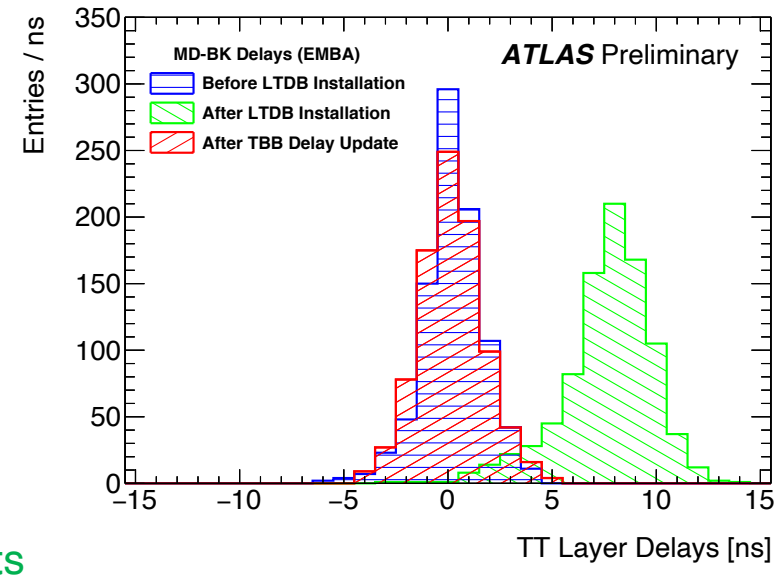


Validation and Commissioning (1)

Legacy trigger readout

- Additional path for TBB, checked gain and timing at L1
  - ⇒ Corrections applied, consistent results as before LTDB installation
- No problems found so far

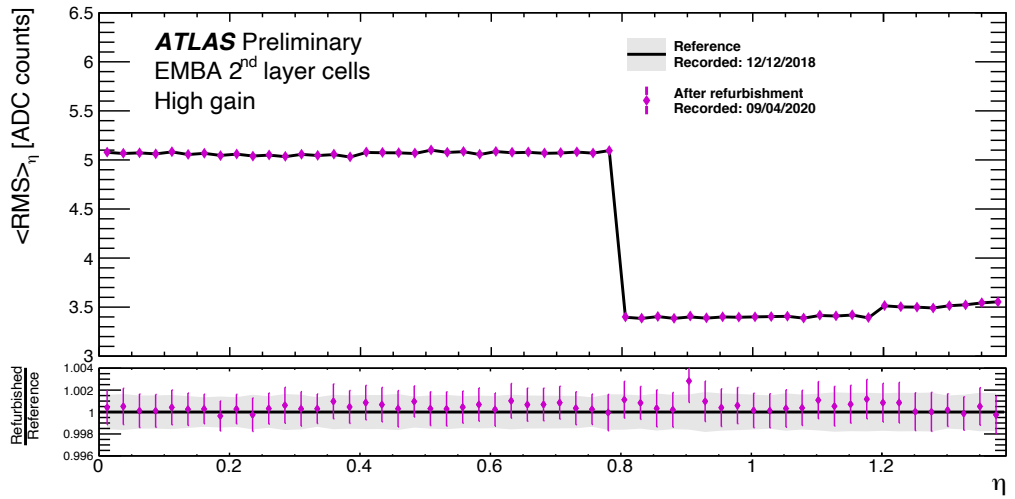
TBB timing correction middle vs back layers



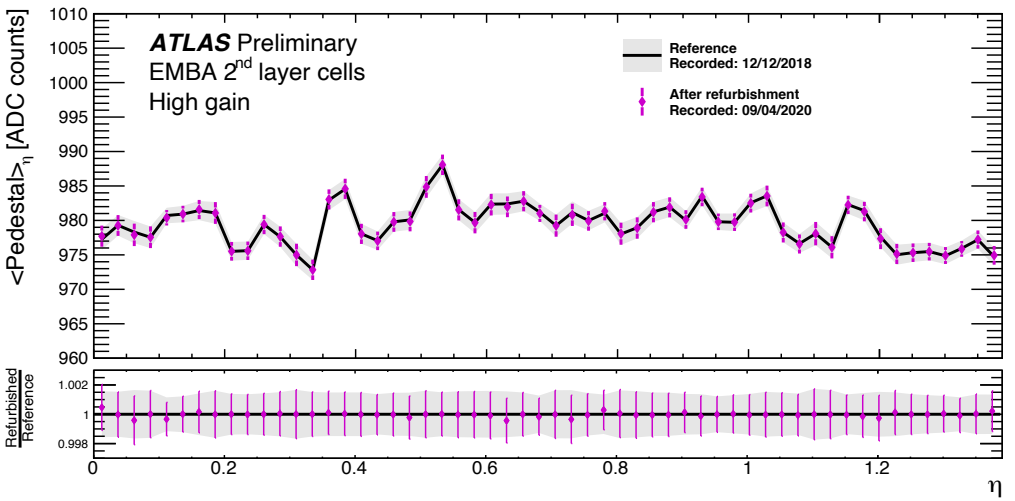
Main readout

- FEBs refurbished with LSB → should have similar calibration coefficients and same noise level as before
  - ⇒ No change in electronic noise level after refurbishment of the FEBs
  - ⇒ Calibration runs compared to pre-LS2 calibration set show same results

Noise level



Pedestal value

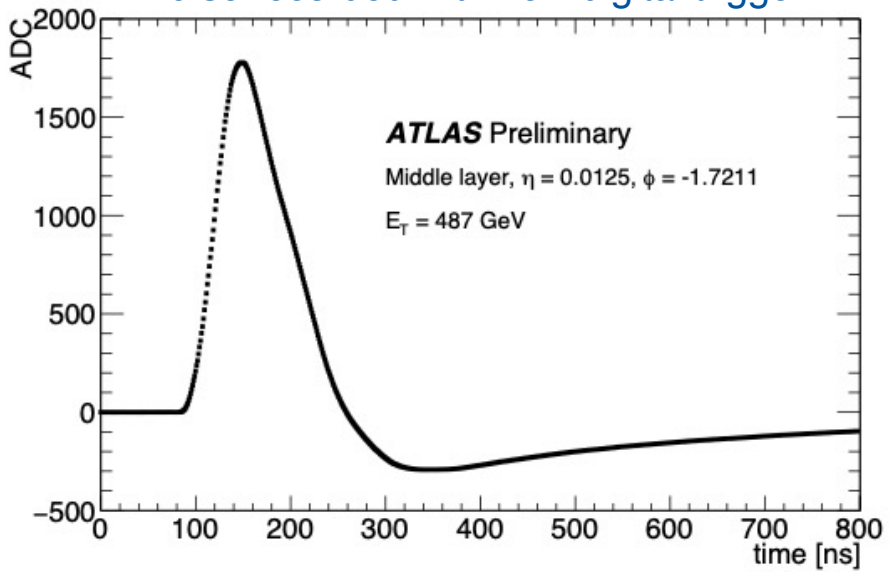


Validation and Commissioning (2)

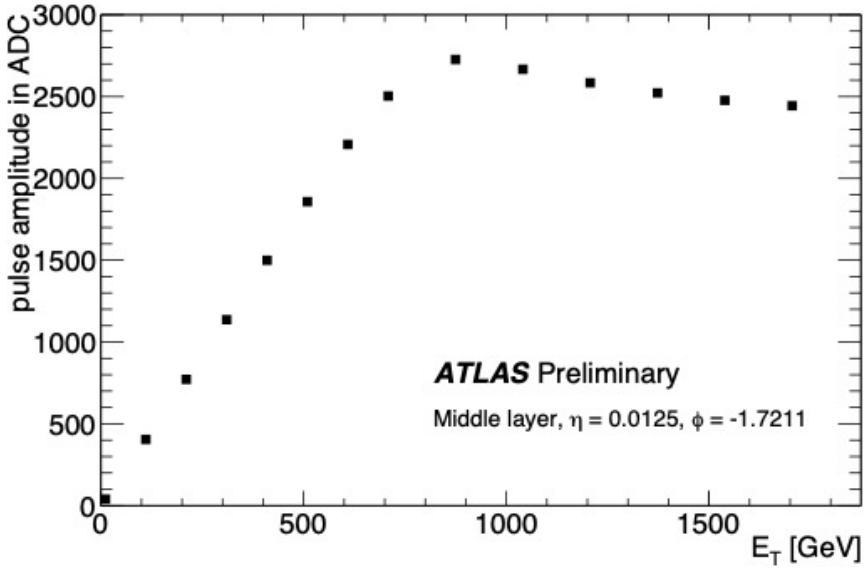
Digital trigger readout

- SC mapping verified using channel pulsing scans
- Pedestal & pulsed runs to monitor stability, energy & timing of SCs should be similar to legacy TTs
  - ⇒ Linearity valid up to ~700 GeV for all SCs, much higher than previous TTs (250 GeV)

Pulse recorded with new digital trigger



Amplitude pulse vs injected calibration signal



Energy computed with LATOME (digital processing)

- Online and offline algorithms should give similar results
  - ⇒ Differences below 1%
  - ⇒ Automatic processing in place

$$E_T = \sum_{i=1}^{4} a^{(5-i)}(data_i - Pedestal)$$

a: calibration constant

Conclusion

LAr digital trigger installation finalized on time despite the pandemic

- Front-end installation done
  - ⇒ All baseplanes, LSB, FEBs refurbished
  - ⇒ All LTDBs installed
- Back-end fully installed, including control & monitoring system
  - ⇒ All the fibers routing to the back-end installed
  - ⇒ Firmware ready for Pilot Run, effort ongoing to develop more automatic tests to validate all the requirements

Validation & commissioning progressing very well

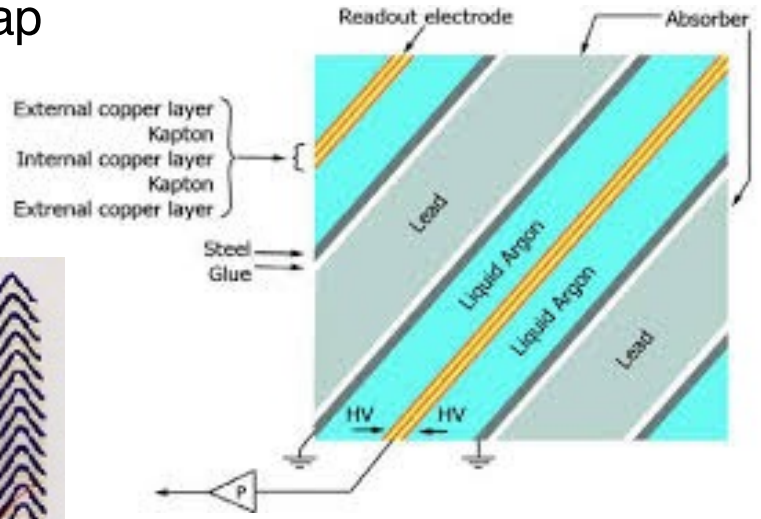
- The main readout path already validated
  - ⇒ No issues found so far (no major deviations from end of Run-2)
- Already applied corrections to synchronize legacy and new systems
- Continuously improving stability, efficiency & robustness
- Expect to keep providing excellent performance during Run-3

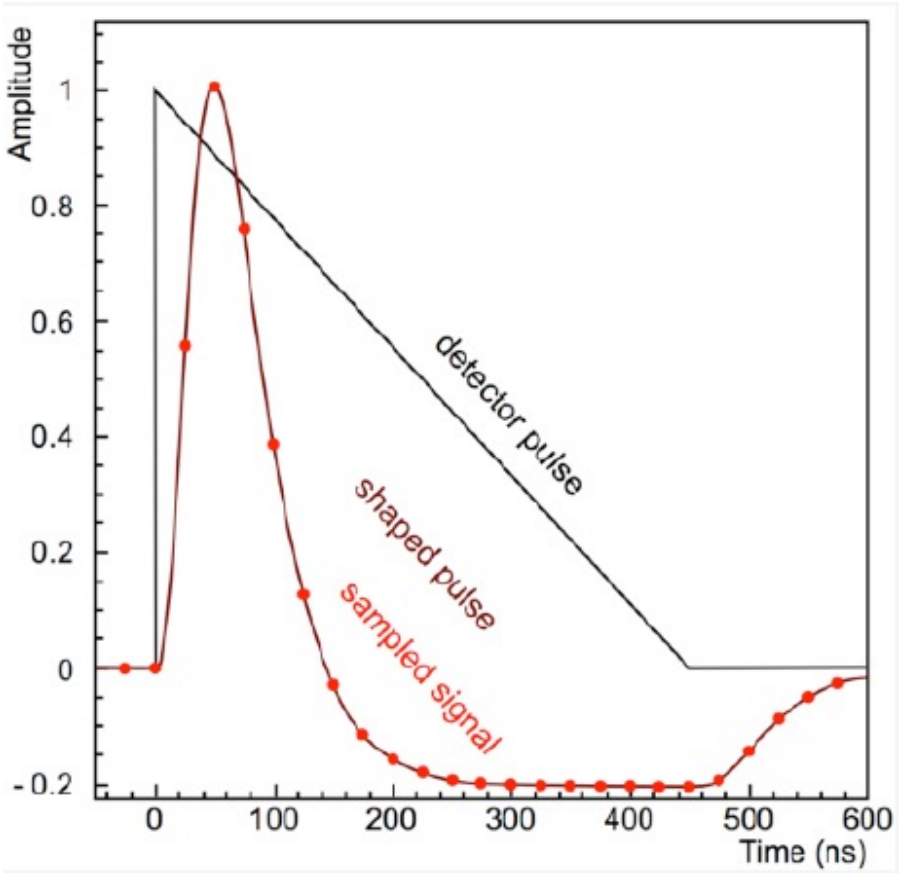
On track to have a fully operational readout and digital trigger for the Pilot Run in October and for Run-3, thanks to a devoted and overachieving group of scientists!

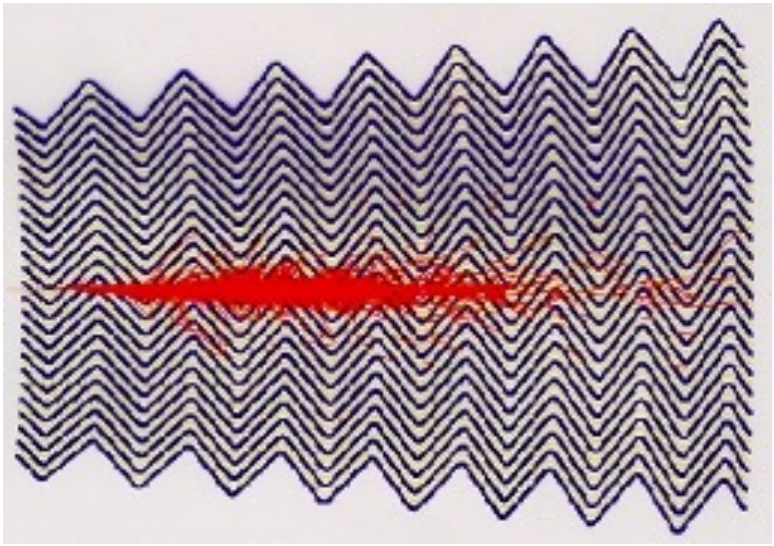
BACKUP

LAr Calorimeter Principle of Operation

- Ionization electrons drift to electrodes due to HV applied to 2.1 mm LAr gap
- Incoming particle creates EM shower & ionizes LAr
- Electric current is produced and read out by electrodes

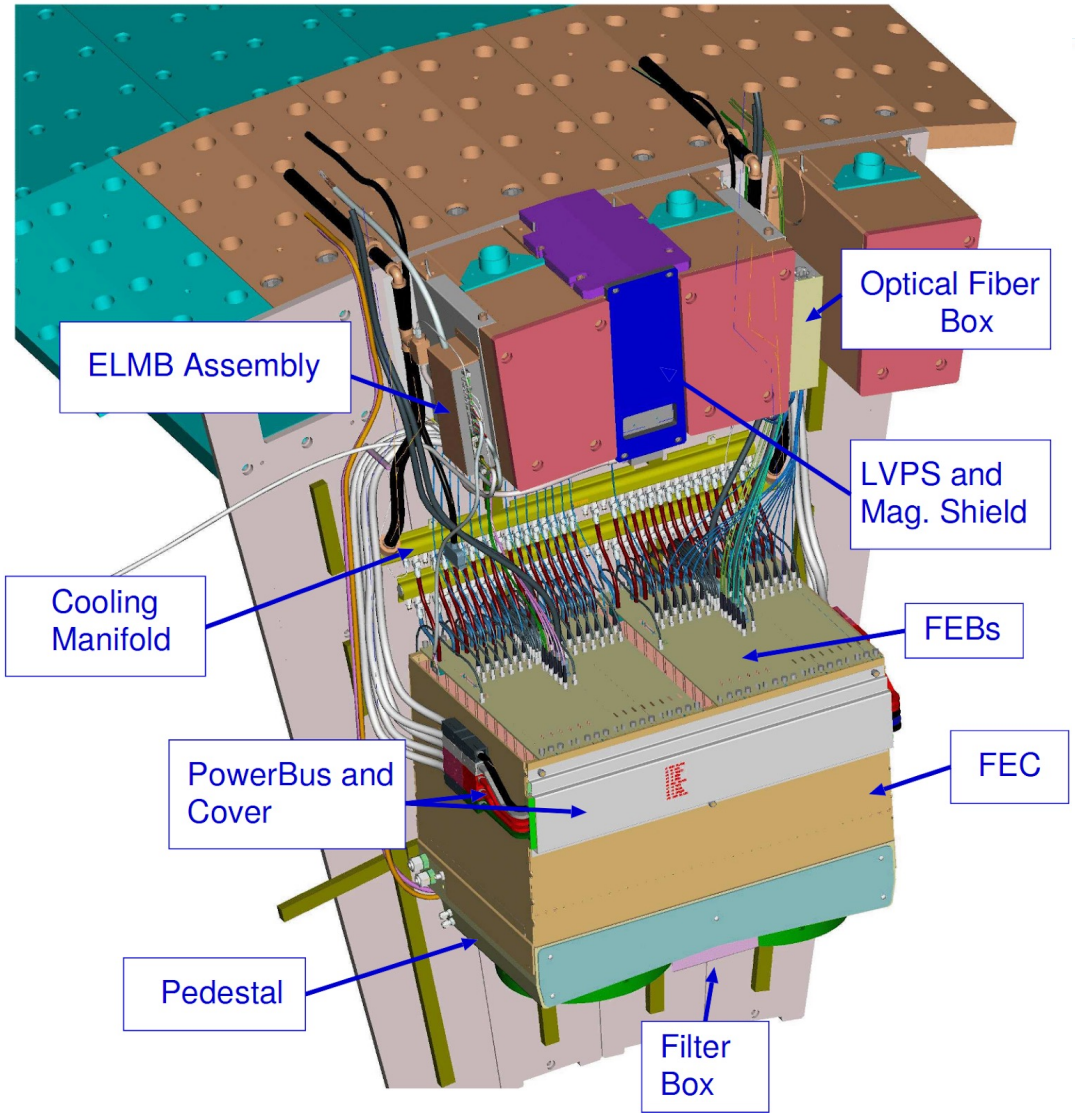




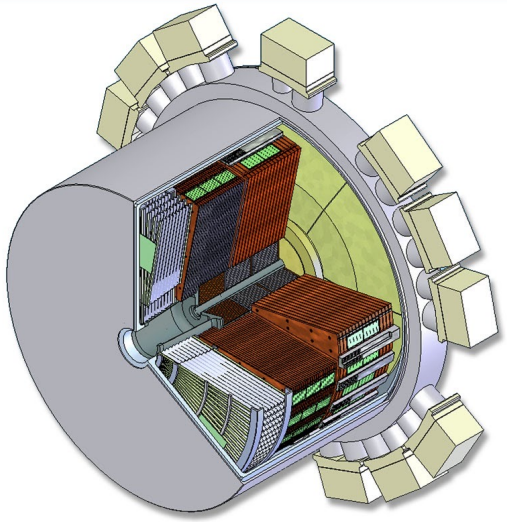


- Signal amplified & shaped (CR-RC^2)
- Sampled signal stored in analogue memory awaiting trigger decision @ 40 MHz & digitization
- ET deposited in given cell computed & sent to DAQ

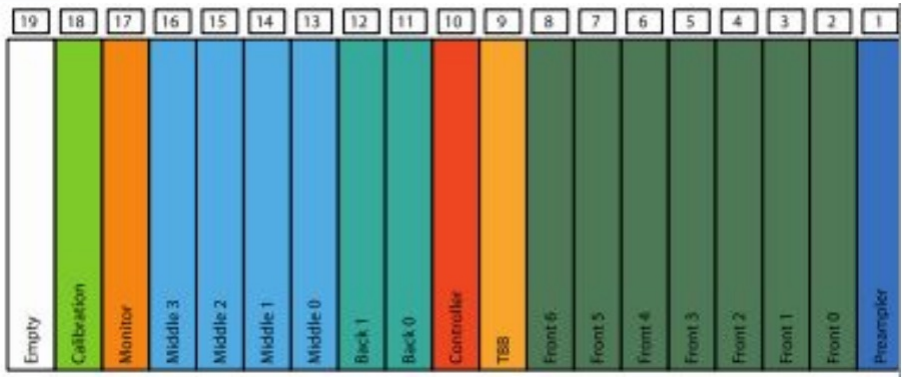
Front-End Crate



EndCap cryostat



Baseplane slot assigment example



58 crates = 116 Half Front-End Crates (HFEC)

- Each HFEC has a baseplane connected by a feedthrough
- One HFEC contains a full set of boards
  - ⇒ FEBs, Calibration boards, TBBs, Controller boards

1524 FEB

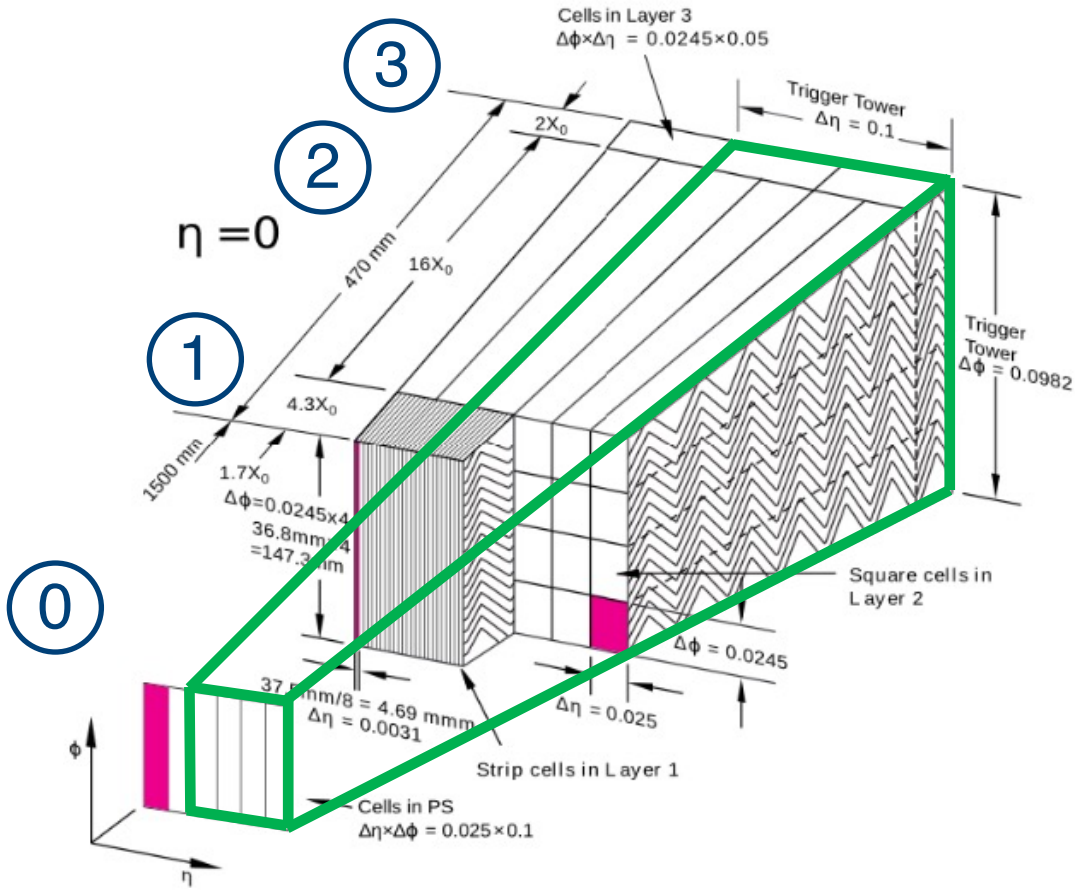
- Each covering a dedicated calorimeter layer
  - ⇒ Back, middle, Presampler, front
- 128 channels each

LAr Calorimeter Geometry

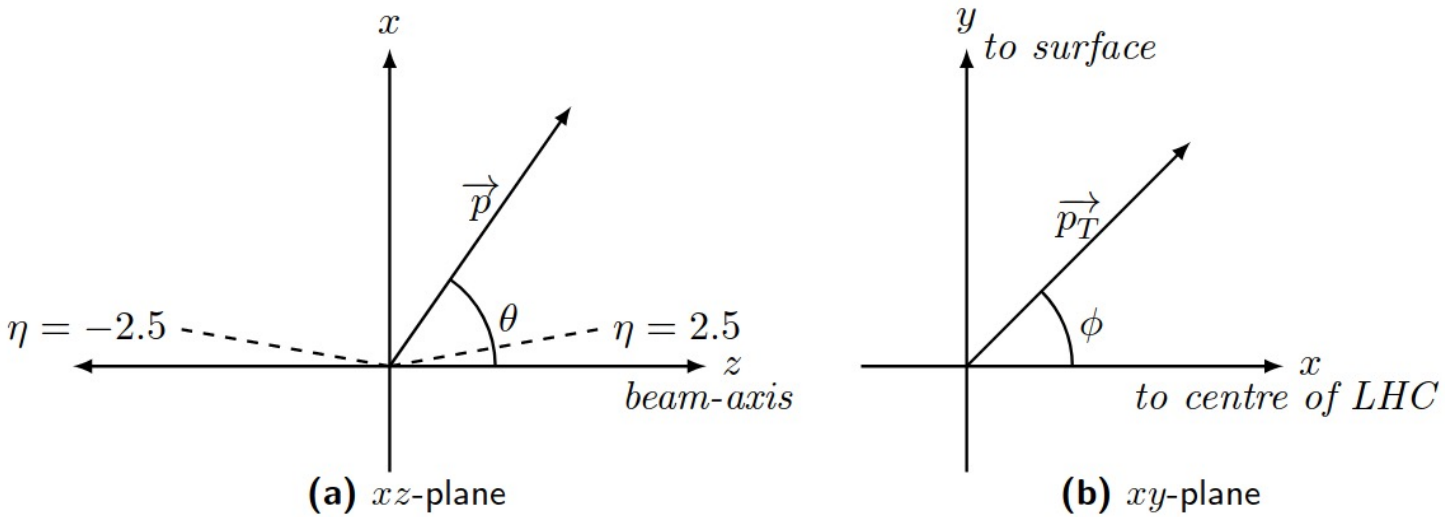
- Total of ~22 x (avg. distance for EM particle to lose all but 1/e energy)
- Four layers with different spatial resolutions
- Presampler **(0)** measure energy loss before calorimeter, $\Delta\eta = 0.025$
- Front **(1)** distinguish π^0 from γ, 4.3 X_0, $\Delta\eta = 0.0031$
- Middle **(2)** contain bulk of EM shower, 16 X_0 , $\Delta\eta = 0.025$
- Back **(3)** capture tail of shower (+ leakage), 2 X_0 , $\Delta\eta = 0.05$
- ~5.4k **Trigger Towers (TT)** $\Delta\eta$ x $\Delta\phi$ = 0.1 x 2π/64 (~0.1)

Example:
EM barrel

LAr calorimeters cells

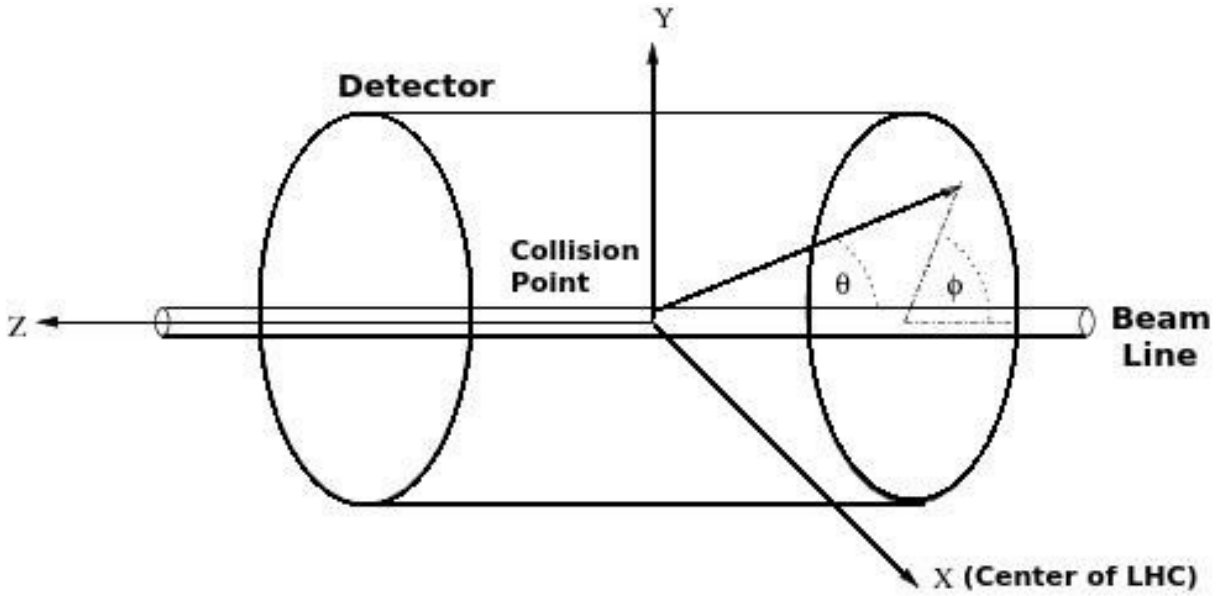


The LHC Coordinate System



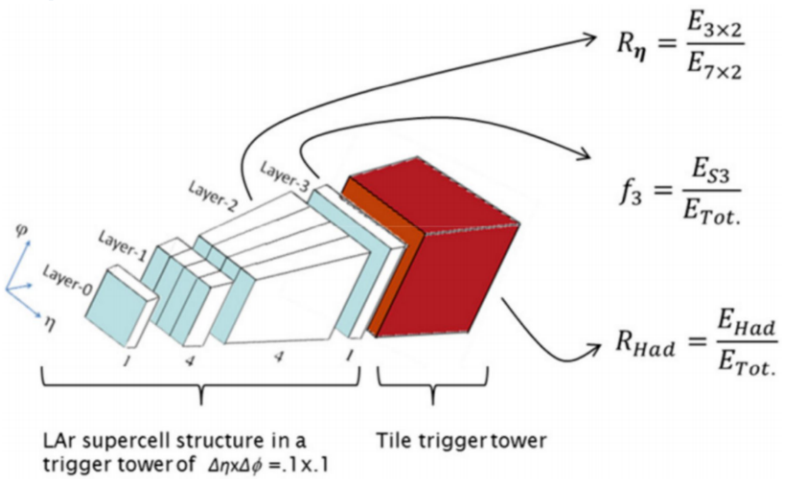
$$\eta = -\ln \tan\left(\frac{\theta}{2}\right)$$

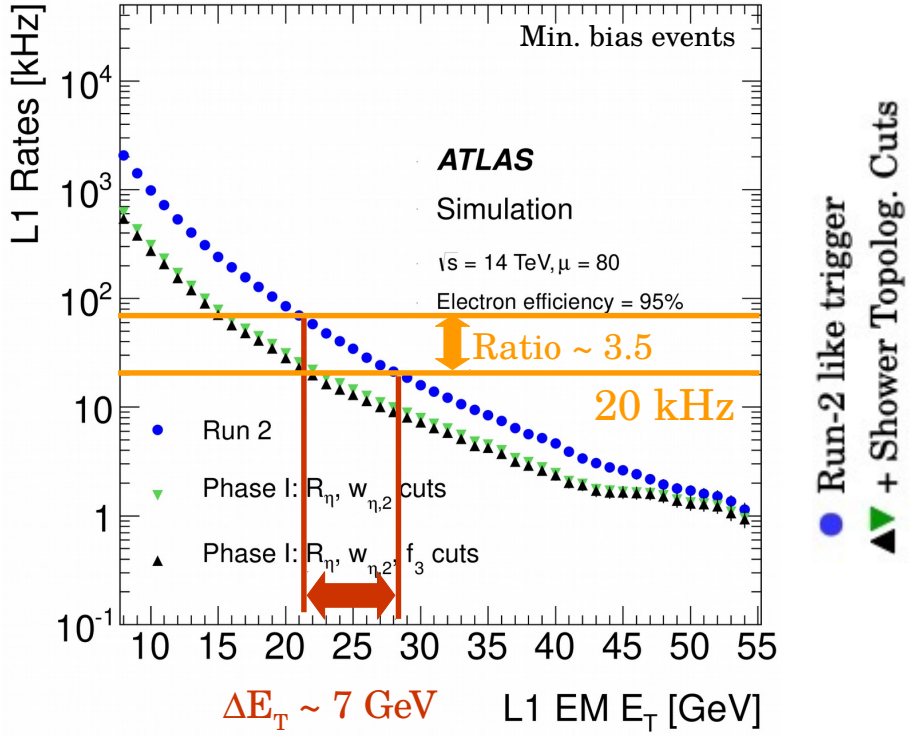
$$\Delta R = \sqrt{(\Delta\phi)^2 + (\Delta\eta)^2}$$

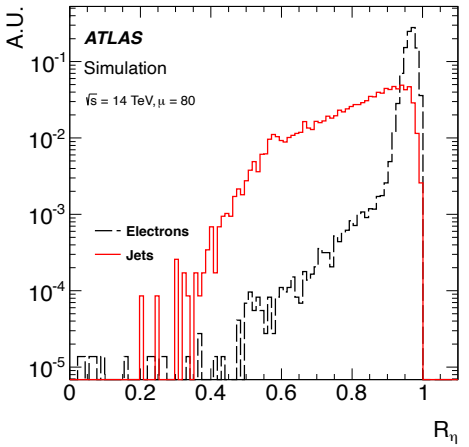


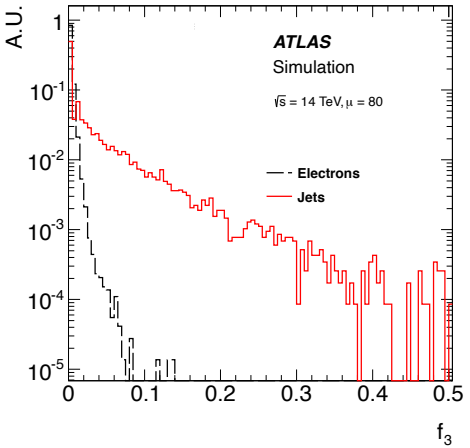
Phase-I Trigger Readout Motivation

- **Shower shape information can be used to discriminate between jets and electrons at L1**
  - ⇒ Improved jet background rejection for electron ID
- **Example of performance for electron**
  - ⇒ Keeping same bandwidth (20 kHz), use E_T threshold 7 GeV lower
- **Enhanced L1 EM resolution**
  - ⇒ Significantly sharpen the trigger turn-on curves
  - ⇒ Reduction offline E_T threshold and increase acceptance

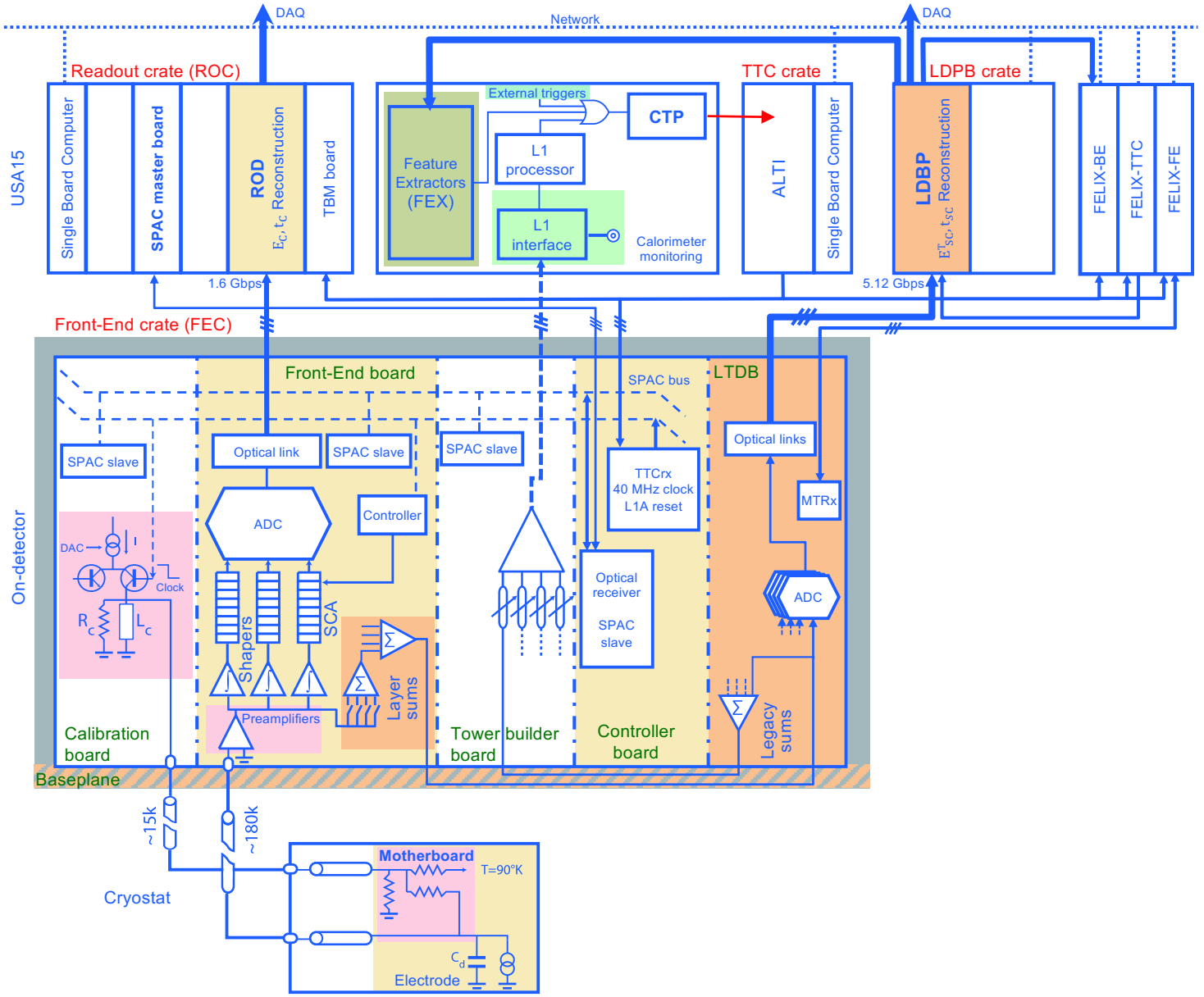






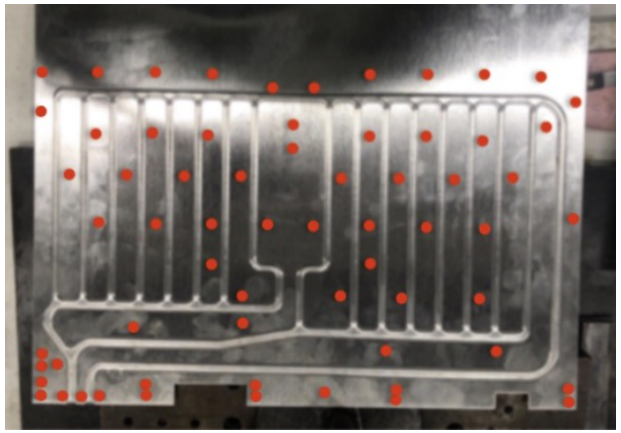


LAr Calorimeter Electronic Layout



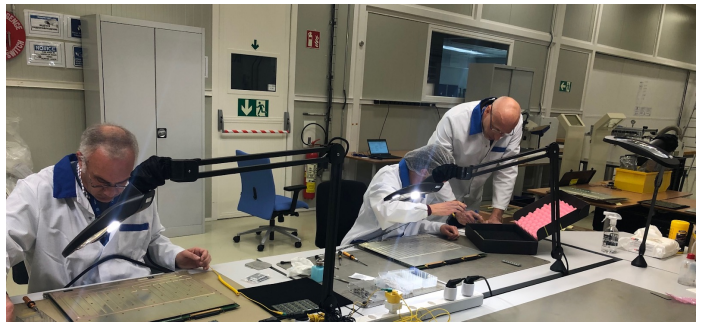
FEB & LSB Refurbishment

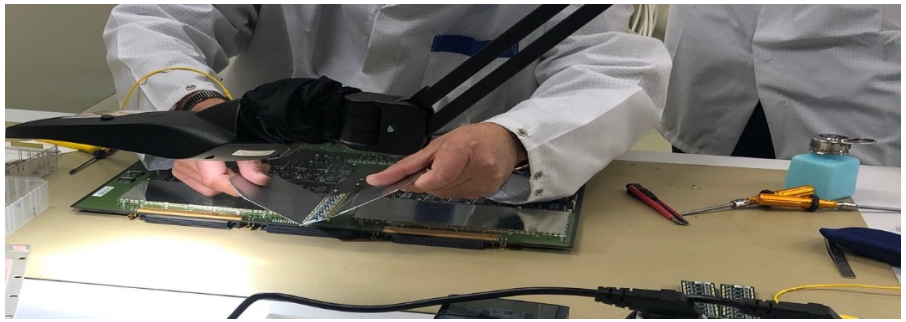
- **LSB exchange is a long and arduous process**
  - ⇒ Removal of all FEB, which are transported to the surface by crane
    - ❖ Including calibration, trigger tower builder, and controller boards: ~1700 boards
  - ⇒ Cooling plate removal, ~50 small screws involved
  - ⇒ Exchange of LSB
  - ⇒ Leak test
  - ⇒ Re-installation of brand-new cooling plates

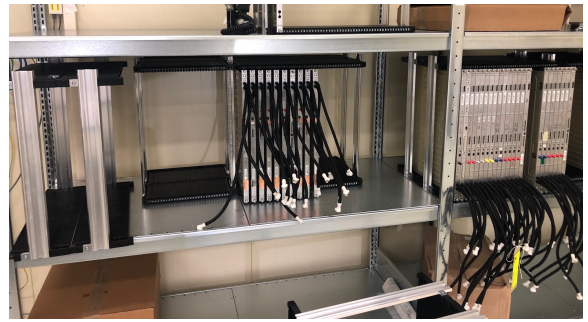


- **Mild radioactivity of boards enforced the refurbishment to take place on site lab at P1 (ATLAS)**

✓ **FEB & LSB already refurbished and 90% of the installation completed**

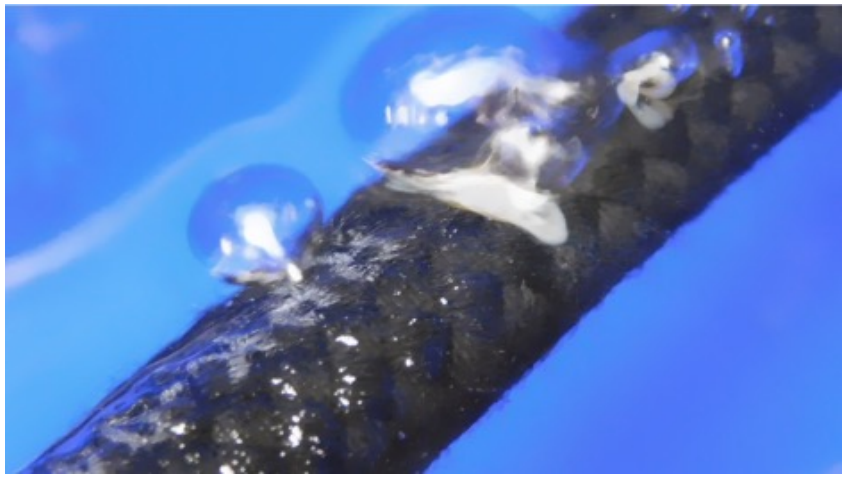






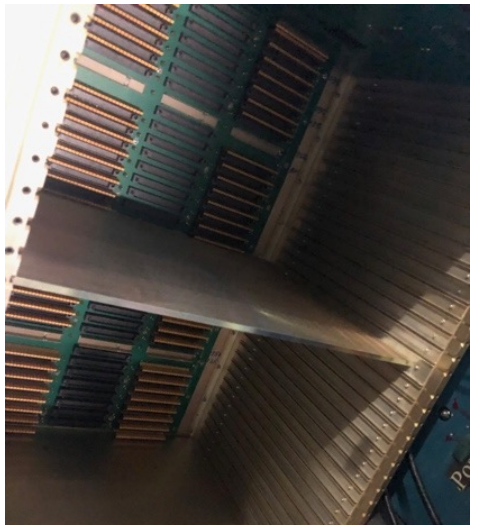
FEB Cooling Hoses Replacement

- **Cooling hoses for all FEBs had to be replaced**
  - ⇒ Ageing rubber losing flexibility & grip on connector
  - ⇒ Some already replaced and refurbished FEBs were re-extracted to undergo replacement
- **Same hoses are used in FEC LVPS and also need replacement**
  - ⇒ Some leaks found in the past
- **Cooling hose replacement has been included in the installation process, without disrupting the schedule**

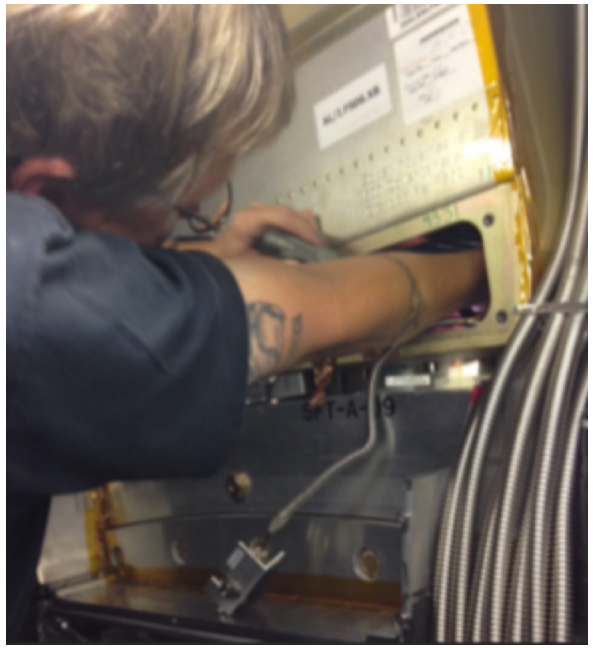


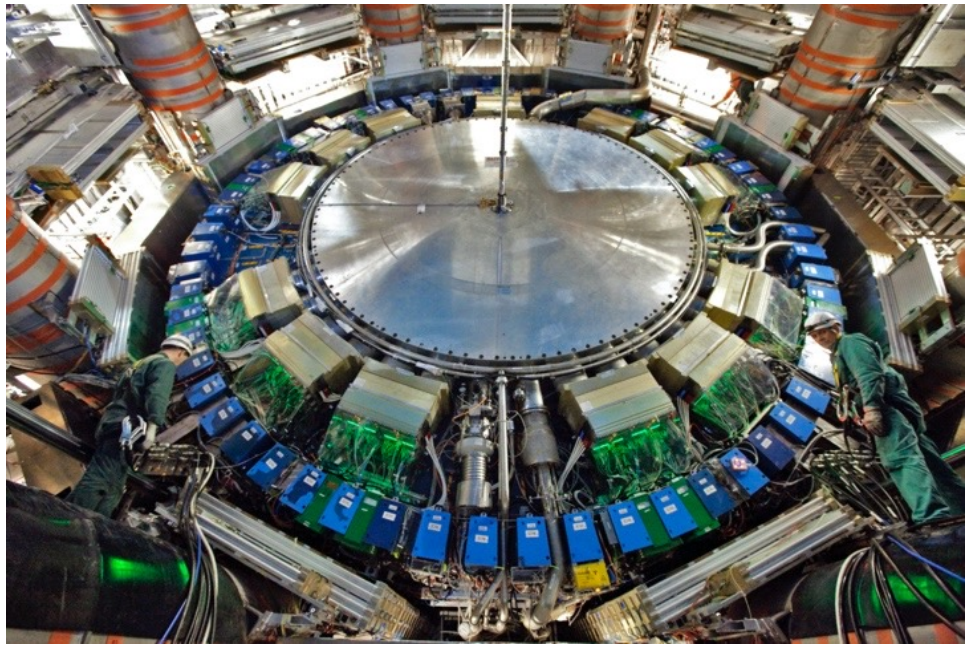
Baseplane Replacement

- **Baseplane replacement is an arduous work in a restricted space**
  - ⇒ Requires removal of all boards first, which are sent to the surface by crane

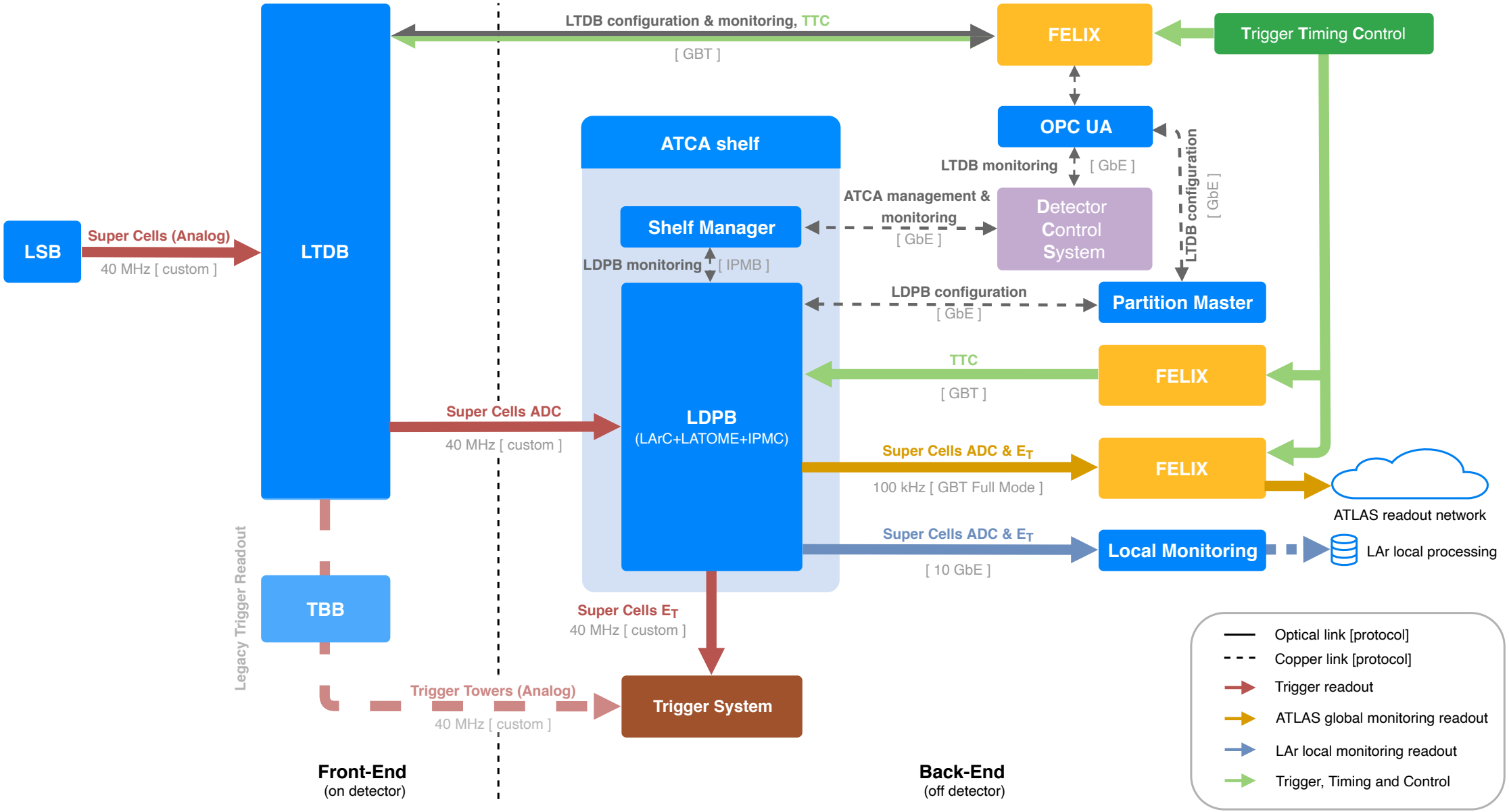


Endcap C

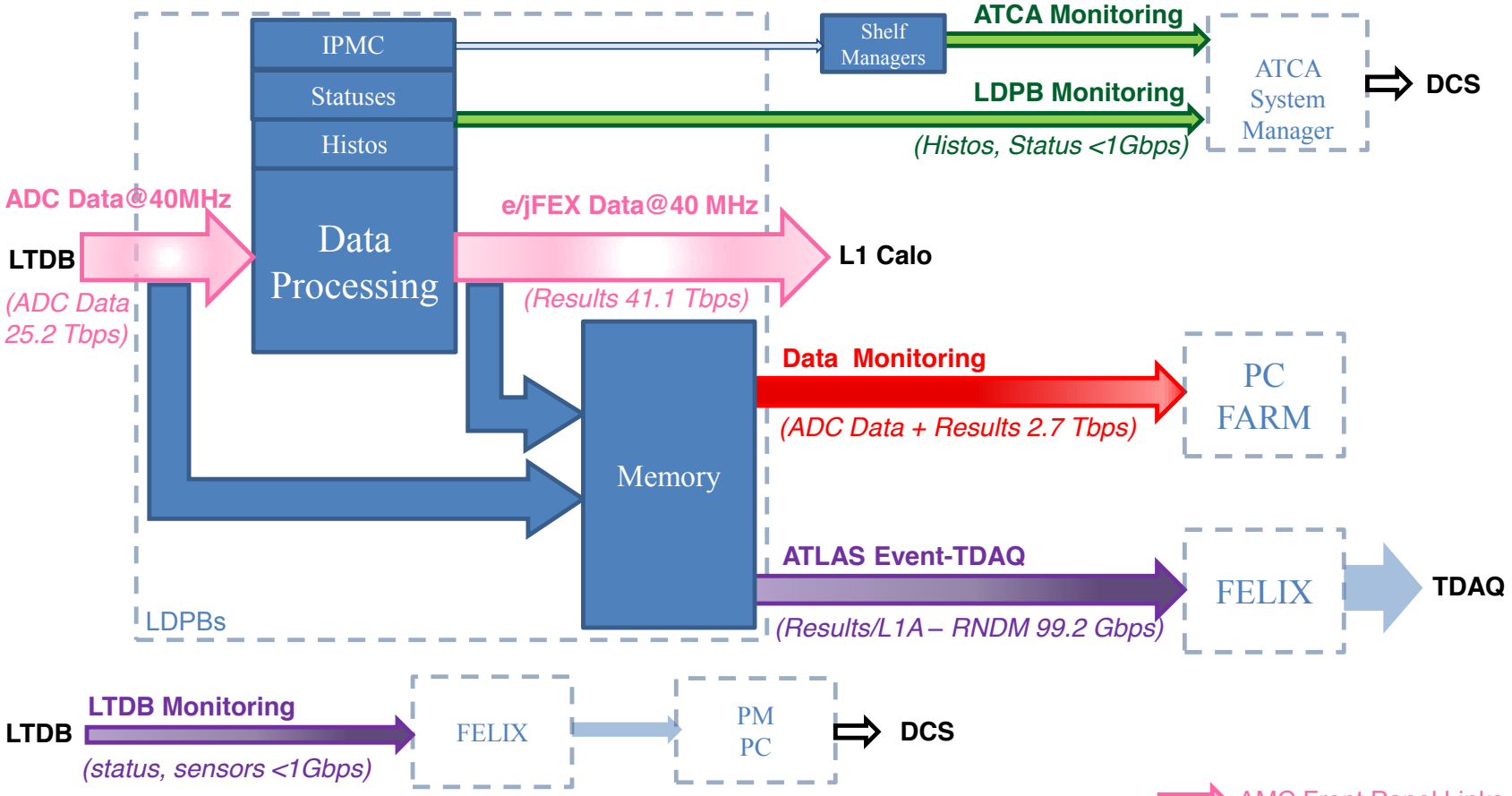




LAr Trigger Readout System



LAr Data Path

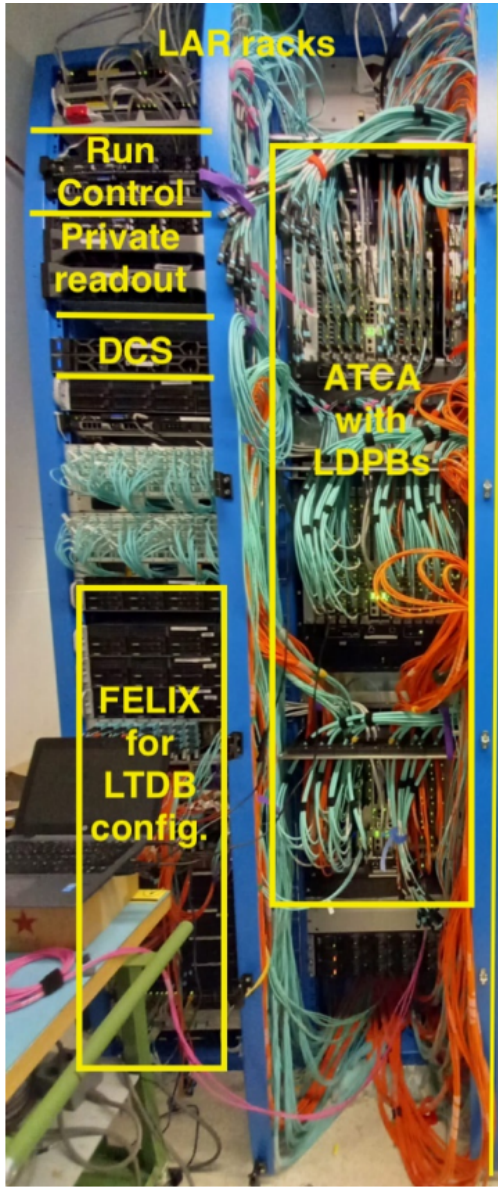


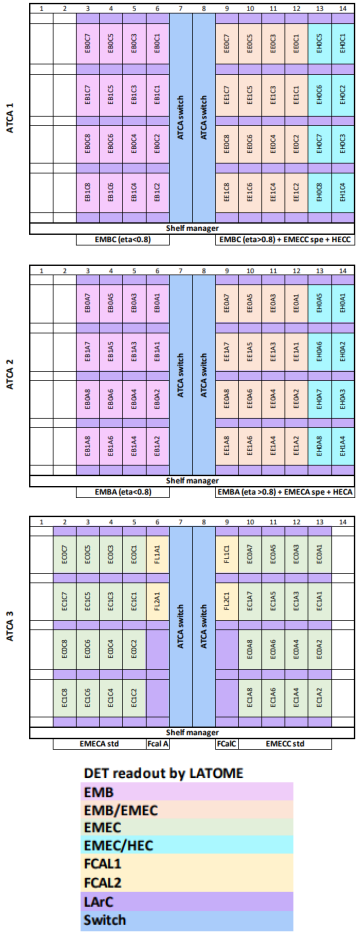
LTDB: 124 Modules LDPB: 31 Blades

Data Flow Rates	ADC Data @40MHz	e/jFEX Data @40MHz	LDPB Monitoring	Data Monitoring	ATLAS Event-TDAQ	LTDB Monitoring	DCS
LTDB	204 Gbps	-	-	-	-	<<1 Gbps	<<1 Gbps
LDPB	814 Gbps	1.3 Tbps	<<1 Gbps	82 Gbps	3.2 Gbps	-	<<1 Gbps
GLOBAL	25.2 Tbps	41.1 Tbps	<1 Gbps	2.7 Tbps	99.2 Gbps	<1Gbps	<<1 Gbps

AMC Front Panel Links
GbE Network
10/40 GbE Network
GBT links
DCS
TDAQ Network

LAr Back-End Trigger Readout





LDPB in USA15 (counting room next to ATLAS cavern)