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Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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A new era of hadron collisions will start around 2027 with the High-Luminosity LHC, that will allow to collect ten times more data that what has been collected since 10 years at LHC. This is at the price of higher instantaneous luminosity and higher number of collisions per bunch crossing.
In order to withstand the high expected radiation doses, the ATLAS Liquid Argon Calorimeter readout electronics will be upgraded.
The electronic readout chain is made of 4 main parts.
The new front-end board will allow to amplify, shape and digitise on two gains the ionisation calorimeter signal over a dynamic range of 16 bits and 11 bit precision. Low noise below Minimum Ionising Particle (MIP), i.e below 120 nA for 45 ns peaking time, and maximum non-linearity of two per mil are required. Custom low noise preamplifier and shaper are being developed to meet these requirements using 65 nm and 130 nm CMOS technologies. They should be stable under irradiation until 1.4kGy (TID) and 4.1x10^13 new/cm^2 (NIEL). Two concurrents preamp-shaper ASICs have been developed and the best one in term of noise has been chosen. The test results of the new version of this ASIC will be presented. A new ADC chip prototype has been also submitted in June. Integration tests of the different components (including lpGBT links developed by CERN) on a 32-channels front-end board are ongoing, and results of this integration will be also shown.
The new calibration board will allow the precise calibration of all 128000 channels of the calorimeter over a 16 bits dynamic range. A non-linearity of one per mil and non-uniformity between channels of 0.25% with a pulse rise time smaller than 1ns should be achieved. In addition, the custom calibration ASICs should be stable under irradiation with same levels as preamp-shaper and ADC chips. The HV SOI CMOS XFAB 180nm technology is used for the pulser ASIC, while the TSMC 130 nm technology is now used for the DAC part. During second prototype testing, it was found that the DAC part of the calibration system, inserted previously with the pulser in XFAB 180nm technology, was not rad-hard, already after 0.5 kGy. This is why a third version has been designed overcoming this issue, and all results will be presented.
The data are sent off-detector at 40 MHz where FPGAs connected through high-speed links will perform energy and time reconstruction through the application of corrections and digital filtering. The off-detector electronics receive 345 Tbps from front-end readout, which require 33000 links at 10 Gbps. For the first time, online machine learning technics are used in the FPGAs in order to better filter the data. The first test results of the signal processing board will be shown.
Reduced data are then sent with low latency to the first level trigger, while the full data are buffered until the reception of trigger accept signals. The data-processing, control and timing functions are realized by dedicated boards connected through ATCA crates. Design status of this timing boards will be shown too.

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