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Electronics – Development for the BoneOscopy and FLASHGuard projects

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Abstract. FLASHGuard and BoneOscopy are LIP projects focused on advanced particle detection and high-speed electronics for cancer treatment and monitoring. This work focuses on the study of a SiPM (Silicon Photomultiplier), identifying the main challenges associated with its use and proposing solutions. The SiPM output signal was first simulated using an equivalent electrical model, validated against results reported in the literature, and subsequently adapted to the parameters of the Hamamatsu S14160-3010PS detector available in the laboratory. Experimental measurements showed that the detector signal is too weak to be observed directly on an oscilloscope, requiring the development of an amplification circuit. A multi-stage amplifier (pre-amplifier, amplifier, pre-buffer, and buffer) was therefore designed and simulated, with particular attention to impedance matching, essential for signals in the radio-frequency range (100–200 MHz). The results, although based on ideal models, validate the proposed architecture and provide a foundation for future work using realistic SPICE models and physical implementation.

1 Introduction

FLASHGuard is a project developed at LIP (Laboratory of Instrumentation and Experimental Particle Physics) that aims to apply advanced particle detection and high-speed electronics to cancer treatment. The project aims to develop a real-time beam monitoring system for FLASH radiotherapy treatments, using photodetectors and high-speed electronics to ensure accurate dose delivery to the tumor. In parallel, the BoneOscopy project focuses on the development of prompt-gamma spectroscopy techniques for the monitoring of metastatic bone cancer during particle therapy, also requiring fast and sensitive detector systems and high-speed electronics. [1]

In this context, the present work focuses on the study and development of readout electronics for a SiPM (Silicon Photomultiplier), with the aim of addressing some of the challenges associated with its use, namely the amplification of the detector’s output signal and the preservation of the relevant high-frequency signal characteristics.

2 Simulation of the SiPM Output Signal

A SiPM is a photodetector that converts photons into electrical signals. Its operation is based on the avalanche multiplication of charge carriers in silicon microcells, enabling the detection of very low light levels. However, the output of a SiPM is characterized by short-duration, low-amplitude electrical pulses. It is therefore useful to simulate its output signal using an equivalent electrical circuit model. Based on [2], the model shown in Figure (9) was used to simulate the output signal of a single active SiPM cell, corresponding to the detection of a single photon. The model is characterized by a current source, together with parallel capacitors and resistors representing the capacitance and resistance of the remaining passive SiPM cells. From the expressions below, it is possible to calculate the gain based on the SiPM bias voltage and breakdown voltage, as well as its output current. However, the

value V_{ob0} represents only the maximum SiPM bias voltage, and therefore $V_{ob0} \geq V_{ob}$.

$$V_{ob0} = V_{bias} - V_{br}$$

$$G = \frac{(C_d + C_q) V_{ob}}{e}$$

$$I_d(t) = \frac{Ge}{\tau_{md} - \tau_{mr}} \left[\exp\left(\frac{-t}{\tau_{md}}\right) - \exp\left(\frac{-t}{\tau_{mr}}\right) \right] u(t) \quad (1)$$

Using LTSpice [5], it was possible to replicate the equivalent SiPM model used in the reference paper [2]. The resulting graph, shown in Figure 1, was compared with the graph presented in the reference paper (Figure 2), validating the simulation of the SiPM equivalent model.

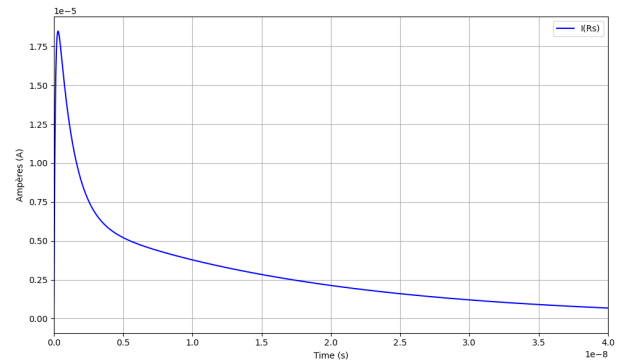


Figure 1. Simulation of the SiPM output signal using the parameters from the reference paper[2]

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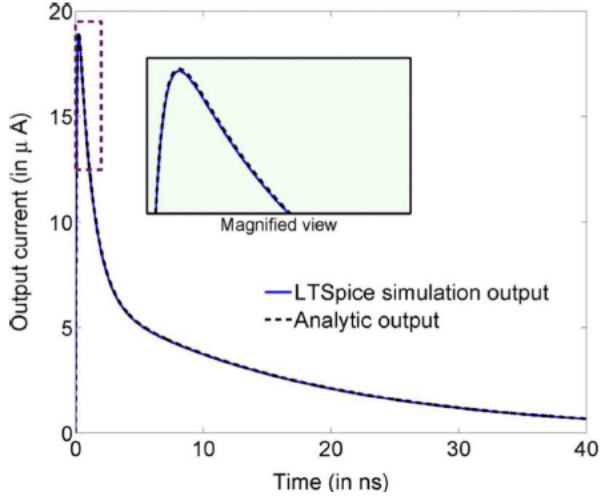


Figure 2. Simulation of the reference paper [2].

Following this, the output signal of the SiPM available in the laboratory, the Hamamatsu S14160-3010PS, was simulated. However, many of the required parameters are not provided in the detector's datasheet [6]. Therefore, a preliminary approximation of the SiPM parameters was made based on the available datasheet information. The parameters used in the simulation are presented in Table 2. The resulting output signal is shown below:

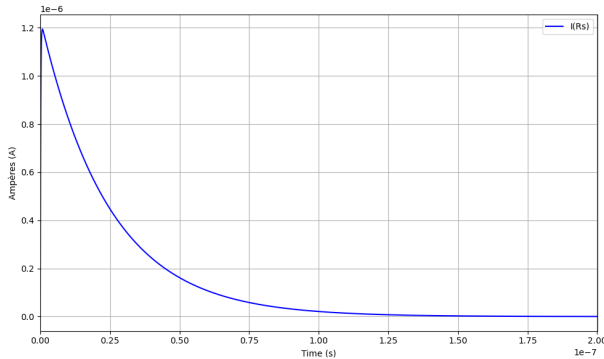


Figure 3. Approximate simulation of the S14160-3010PS.

Although this is a simplified approximation, it was possible to obtain a pulse with a duration similar to that specified in the SiPM datasheet, allowing operation with pulse frequencies in the range of 100–200 MHz. This frequency range places the pulse within the radio-frequency (RF) domain. Even though the simulation it is a simplified approximation is expected that the output signal will not be directly observable on the oscilloscope on the laboratory, due to its low amplitude ($60\mu\text{V}$), as seen in Figure 10.

3 Signal Acquisition Using an Oscilloscope

Following the simplified simulation, an experimental measurement of the pulse amplitude was performed using an oscilloscope. For this purpose, a simple circuit consisting of the detector and two capacitors connected in parallel to ground was implemented. As anticipated, the signal

produced by the detector exhibited a very low amplitude, making it impossible to observe directly (Figure 4). This result confirmed the need to integrate an amplification circuit to enable the signal to be properly measured.

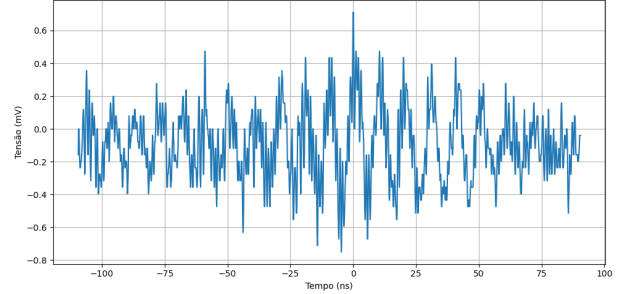


Figure 4. Signal acquisition using an oscilloscope

4 Construction of the Amplification Circuit

4.1 Impedance of Input and Output

When working with a pulse in the range of 100–200 MHz, as verified in this case, due to the high speed of the signal transition, it presents frequency components in the radiofrequency domain. Consequently, it is necessary to pay special attention to the input and output impedances of the circuit, since the oscilloscope used has an input impedance of $50\ \Omega$.

To analyze this effect, two circuits with different input impedances were implemented: one with an impedance of approximately $50\ \Omega$ and another with $6.2\ \text{k}\Omega$, whose results are represented in Figures 11 and 12, respectively. [3]. The $6.2\ \text{k}\Omega$ resistor was selected for the transistor's common-emitter configuration, which requires a higher input impedance for stable operation compared to the common-base configuration, which has a lower input impedance.

As can be observed, the use of a high input impedance causes greater signal reflection. This reflection interferes with the original signal, resulting in an increased fall time compared to the input signal. This behavior highlights the importance of impedance matching in circuits operating with high-speed transition signals.

4.2 Amplification Circuit Architecture

Considering the challenges associated with the signal characteristics, the amplifier architecture shown in Figure 5 was adopted. The complete amplification circuit is shown in Figure 13 and follows the structure described above.

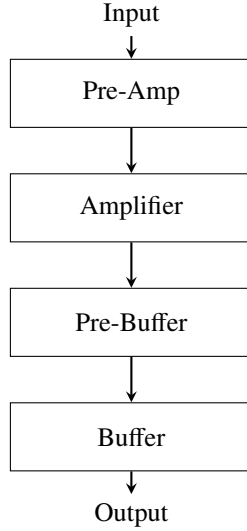


Figure 5. Estrutura do amplificador.

The first stage of the pre-amplifier consists of a common-base NPN transistor. This configuration provides a low input impedance of approximately $50\ \Omega$ and a high voltage gain. However, since the transistor operates in a common-base configuration, it does not provide current gain.

To address this limitation, a second transistor is used in a common-emitter configuration, providing amplification of both the signal current and voltage.

Finally, a current buffer was intended to not only increase the signal current but also provide an output impedance of approximately $50\ \Omega$ for the oscilloscope. However, the buffer introduces some voltage attenuation. To compensate for this loss, two op-amps were added to form a pre-buffer stage, providing additional voltage gain before the signal reaches the buffer.

4.3 Amplifier Characteristics

This amplification circuit has a frequency-dependent gain, as the product of the target frequency and the gain must be taken into account. This product is directly related to the required operating frequency of the transistor, and, as a first approximation, the following relationship can be established [4]:

$$\beta \approx \frac{f_T}{f} \quad (2)$$

Where f_T represents the transistor's transition frequency, i.e., the frequency at which the transistor's current gain is unity. Therefore, to ensure adequate signal amplification, the transistor must have a transition frequency sufficiently higher than the operating frequency.

Based on the graphs presented in Figures 14 and 15, a voltage gain of approximately $21\times$ was obtained for the pre-amplifier, while the amplifier achieved a current gain of approximately $9\times$ and a voltage gain of approximately $21\times$. Therefore, considering the relationship presented above, the transistors should have a transition frequency greater than approximately 2GHz to ensure that the desired gain is achieved at the target operating frequency.

These effects are not directly observable in the NPN transistors used in the simulation, as ideal transistor models were employed. However, some effects related to the practical limitations of the circuit can already be observed in the op-amp stage, as shown in Figure 6. Although the stage achieves a gain of approximately $25\times$, a phase delay and a reduction in gain compared to the theoretically expected value can be observed. Nevertheless, these effects remain limited due to the high operating frequency of approximately 30GHz assumed for the op-amp in the simulation.

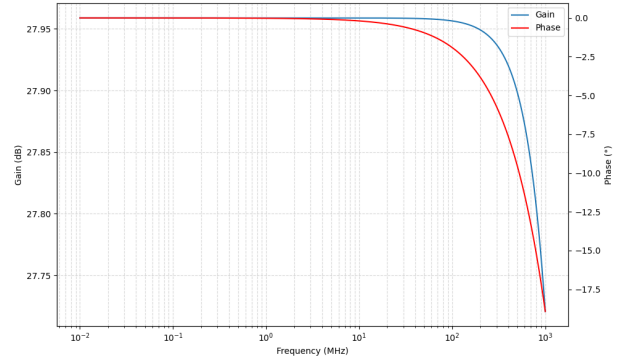


Figure 6. Gain of the operational amplifiers.

Finally, analyzing the buffer, a significantly high current gain can be observed, as shown in Figure 7, corresponding to approximately $90\times$. According to the relationship presented above, this gain requires the transistor to have a transition frequency greater than approximately 18GHz to ensure adequate operation at the target frequency.

In addition to the gain, it is also important to analyze the voltage attenuation introduced by the buffer. As shown in Figure 8, an attenuation of approximately -6dB is observed. This attenuation corresponds to a reduction of the voltage signal amplitude to approximately half its input value, indicating a significant loss between the input and output of the buffer.

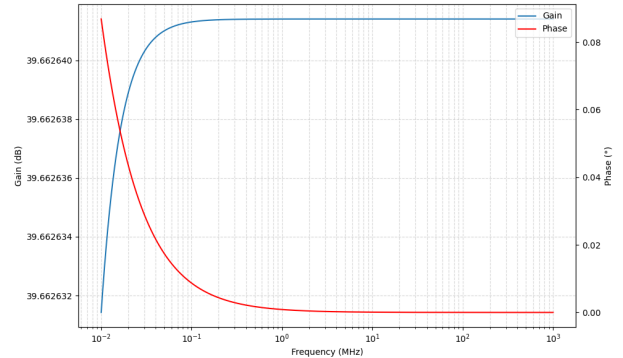


Figure 7. Current gain in the buffer.

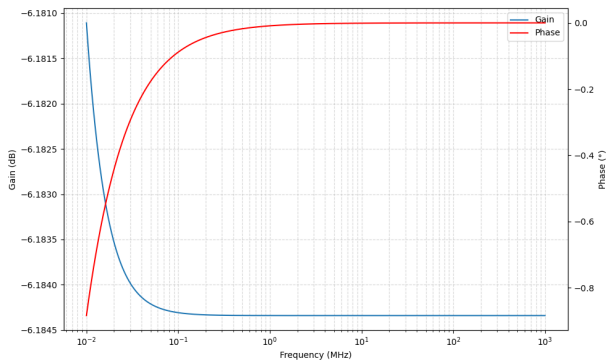


Figure 8. Voltage loss in the buffer.

5 Conclusion and Future Perspectives

In this work, the readout electronics for a SiPM detector were developed and analyzed. Based on an equivalent electrical model adapted to the Hamamatsu S14160-3010PS detector, the generated signals exhibited fast transitions in the 100–200 MHz range. Experimental tests confirmed that the raw output signal is too weak for direct oscilloscope observation, requiring a dedicated multi-stage amplification chain (pre-amplifier, amplifier, pre-buffer, and buffer). Implementing a 50 Ω impedance match at the input and output proved essential to minimize reflections and preserve the high-frequency pulse shape.

The proposed architecture successfully achieved voltage gains of 21 $\times$ and 25 $\times$ at different amplification stages, along with current gains of 9 $\times$ and 90 $\times$. These results require high-speed transistors with transition frequencies of $f_T > 2$, GHz and $f_T > 18$, GHz, respectively, for physical implementation. Although based on ideal transistor models, the simulations validated the overall design while highlighting expected non-idealities, such as the -6 , dB attenuation introduced by the buffer.

As future work, an LTspice [5] analysis should be performed using realistic SPICE models for the transistors and operational amplifiers, in order to account for their frequency limitations and associated parasitic effects. Following this step, the circuit should be physically assembled and preliminarily tested on a laboratory test bench using real components. This experimental validation should allow the practical behavior of the circuit to be assessed, potential deviations to be measured, component values to be adjusted, and the signal response to be optimized before any final integration.

Finally, once the experimental setup has been validated, the circuit can be designed and implemented on a dedicated printed circuit board (PCB).

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environment throughout the internship. I am also grateful for the opportunity to develop a project that encompassed several of my areas of interest and represented a significant challenge throughout this journey.

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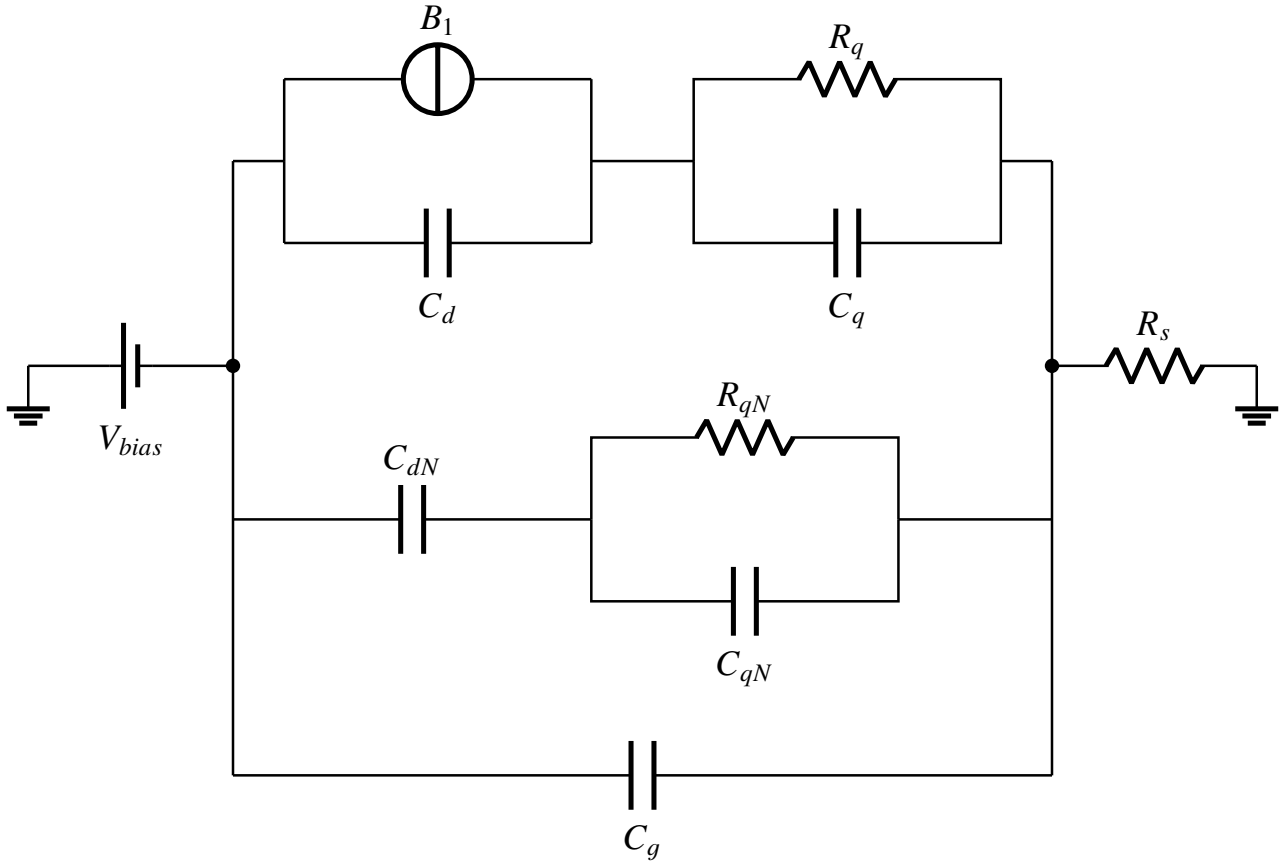


Figure 9. SiPM Equivalent Electrical Circuit

Table 1. Parameters of the SiPM Equivalent Circuit Presented in the Reference Paper [2].

Parameter	Value
N_{cell}	3600
V_{bias}	70 V
V_{ob}	1.33 V
C_d	77 fF
R_q	140 k Ω
C_q	23 fF
C_{dN}	$(N_{cell} - 1)C_d$
R_{qN}	$R_q / (N_{cell} - 1)$
C_{qN}	$(N_{cell} - 1)C_q$
C_g	28 pF
R_s	15 Ω
τ_{md}	100 ps
τ_{mr}	10 ps

Table 2. Parameters of the Hamamatsu SiPM S14160-3010PS Approximate Model, Based on the Datasheet Specifications.

Parameter	Value
N_{cell}	89984
V_{bias}	43.62 V
V_{ob}	5 V
C_d	5 fF
R_q	140 k Ω
C_q	0.89 fF
C_{dN}	$(N_{\text{cell}} - 1)C_d$
R_{qN}	$R_q / (N_{\text{cell}} - 1)$
C_{qN}	$(N_{\text{cell}} - 1)C_q$
C_g	28 pF
R_s	50 Ω
τ_{md}	100 ps
τ_{mr}	10 ps

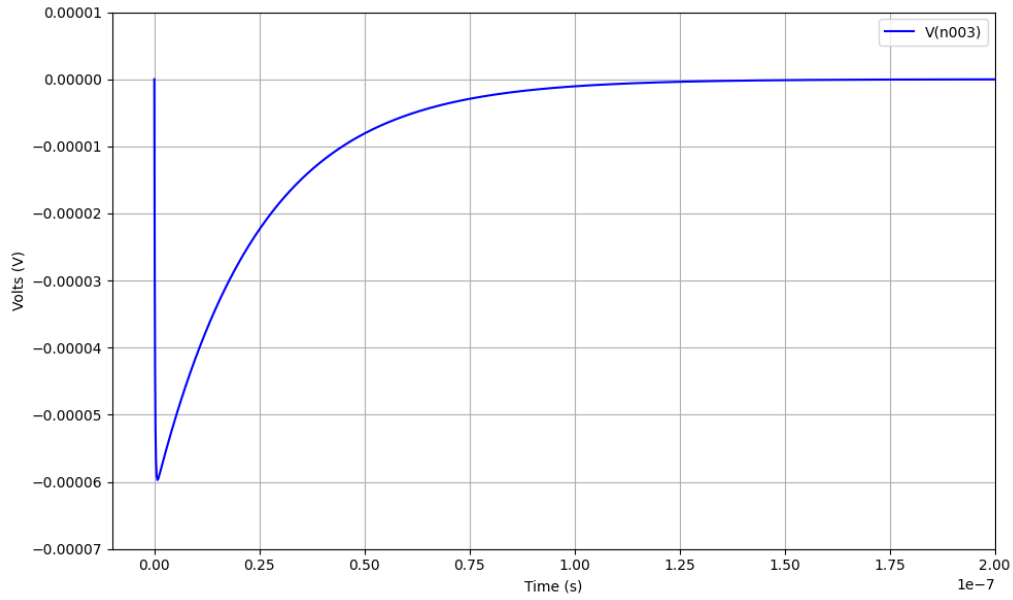


Figure 10. Simulation of the SiPM output signal based on the parameters from the Hamamatsu S14160-3010PS datasheet.

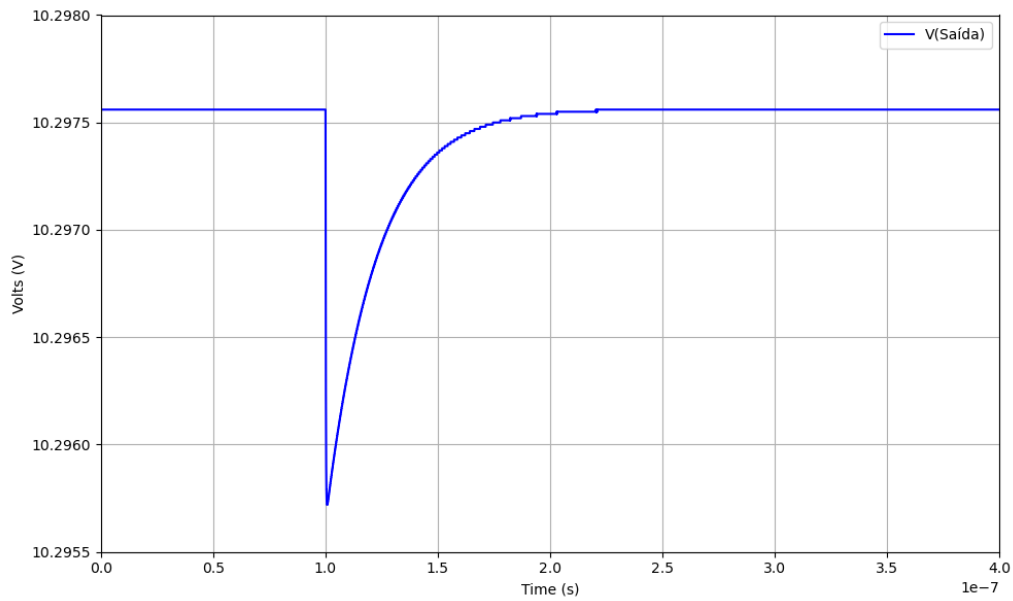


Figure 11. Low Input Impedance

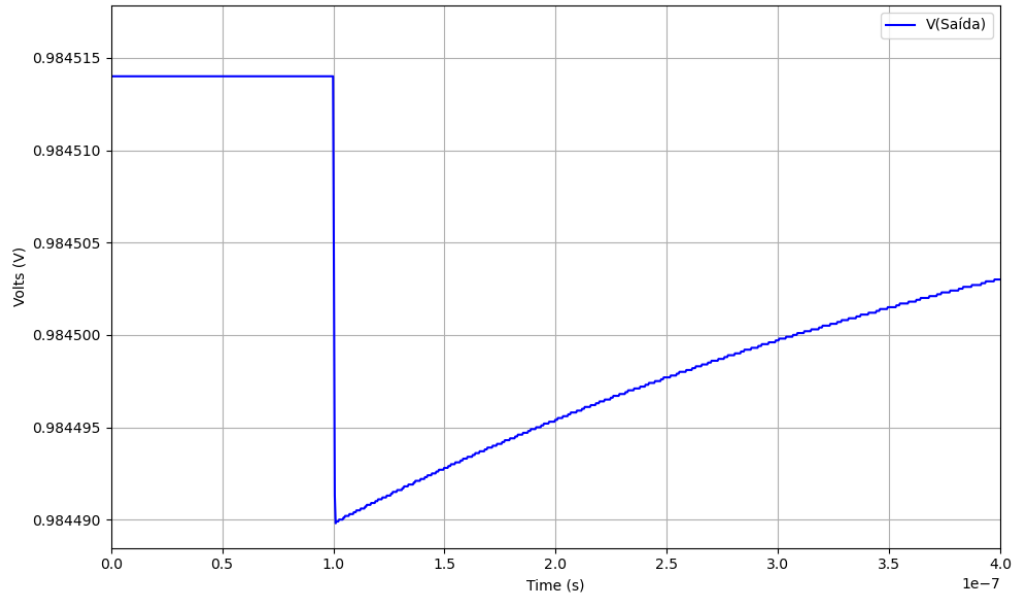


Figure 12. High Input Impedance

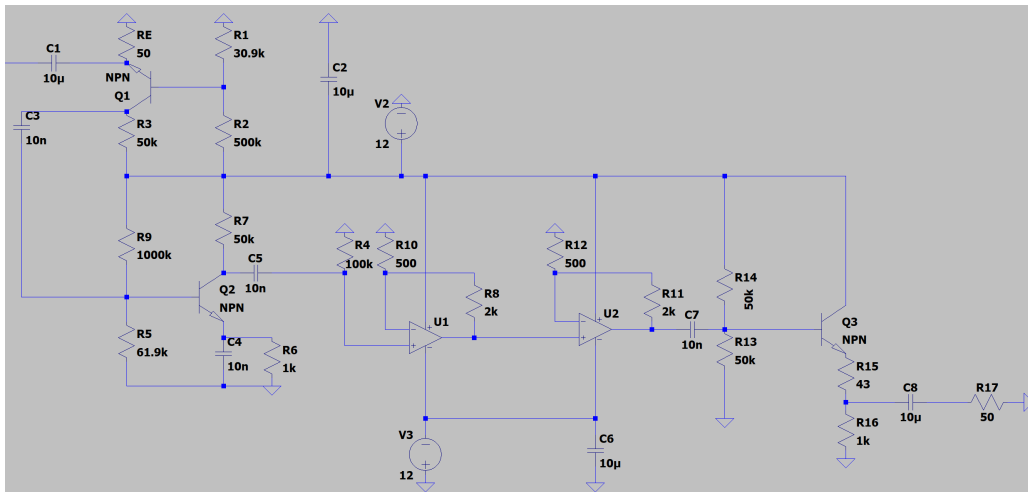


Figure 13. Complete Amplification Circuit

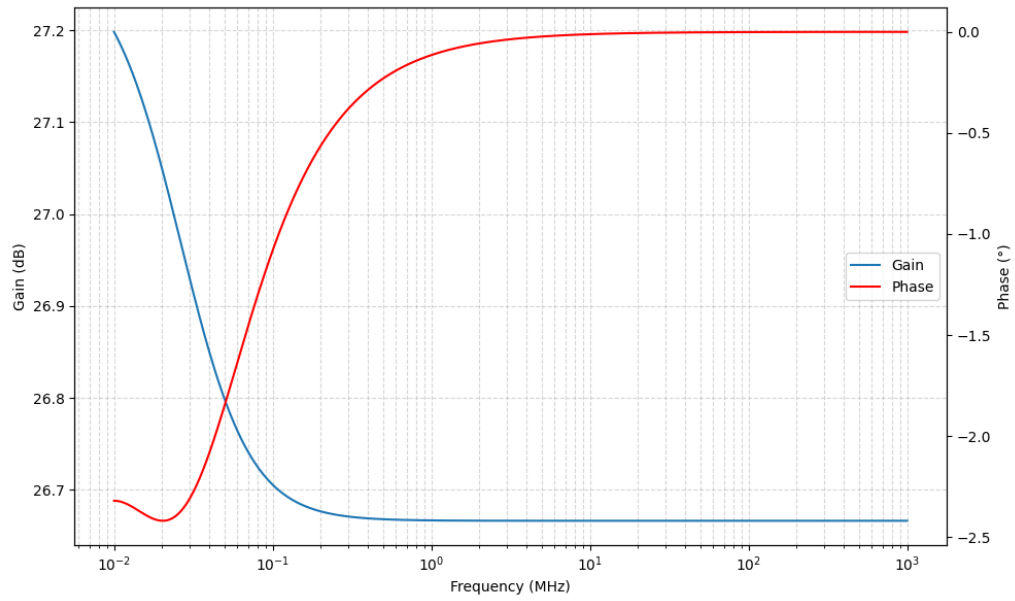


Figure 14. Voltage Gain in the Pre-amplifier

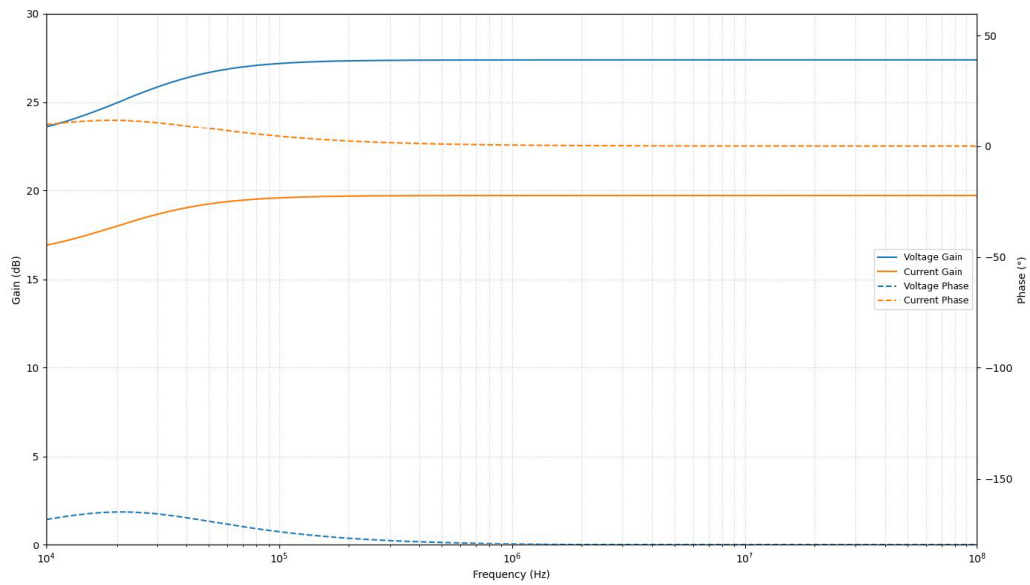


Figure 15. Current Gain in the Amplifier