

Instrumentation Development for the FLASHGuard Advanced Radiotherapy Monitoring Project

Pedro Filipe de Sousa Silva^{1,a}

¹LIP – Laboratório de Instrumentação e Física Experimental de Partículas / Instituto Superior Técnico, Lisbon, Portugal

Project supervisor: Prof. Pedro Assis, Manuel Ratola

September 30, 2026

Abstract. A Silicon Photomultiplier (SiPM) is a highly sensitive light sensor capable of detecting signals down to the single-photon level. These devices are widely used in radiation-detection systems, namely through the detection of light produced by charged particles traversing scintillating materials or through Cherenkov radiation.

SiPMs produce low-amplitude, short-duration current pulses, requiring front-end circuits capable of amplifying and conditioning the signal before further processing. In addition to pulse detection, measuring the charge associated with each event is particularly relevant, since this charge is directly related to the number of fired microcells and, consequently, to the number of detected photons.

This work develops a front-end system for SiPM readout based on a Charge-Sensitive Amplifier (CSA) with an integrating topology. The system is implemented on a Printed Circuit Board (PCB) and, in addition to the CSA, integrates a reset mechanism, a comparator circuit, a control circuit, and an Analog-to-Digital Converter (ADC), enabling the conditioning, detection, and acquisition of the signals produced by the SiPM.

SPICE simulations of the proposed circuit are also presented in order to evaluate its behaviour and validate the adopted topology prior to experimental implementation.

KEYWORDS: Silicon Photomultiplier (SiPM), Charge-Sensitive Amplifier (CSA), Parasitic Capacitance, Printed Circuit Board (PCB)

1 Introduction

The aim of this work is to develop a front-end system for SiPM readout based on a charge-sensitive amplifier. The circuit is designed and dimensioned to allow the detection of low-charge pulses while simultaneously minimising noise and ensuring system stability. Reset and threshold-detection mechanisms are also implemented, the circuit operation is validated through simulations, and a PCB is designed to minimise parasitic effects associated with the physical implementation. Finally, the influence of these parasitic effects on the overall system performance is characterised, and the resulting signal is prepared for subsequent acquisition and processing.

1.1 Silicon Photomultipliers

Silicon Photomultipliers (SiPMs) are solid-state photodetectors formed by arrays of microcells operated in Geiger mode. Their high sensitivity, compact size, and immunity to magnetic fields make them particularly useful in radiation- and particle-detection instrumentation [3, 4]. Although SiPMs detect photons rather than charged particles directly, they can be used to detect particles indirectly when the particle interaction produces light, for example through scintillation or Cherenkov emission [4, 5].

For the present work, the most relevant characteristic of the SiPM is the relation between the charge of its electrical output pulse and the number of fired microcells. Within the linear operating region, the charge corresponding to the firing of a single microcell can be written as

$$Q_{1\text{p.e.}} = Gq_e, \quad (1)$$

where G is the SiPM gain and q_e is the elementary charge. Thus, for an event in which N microcells are fired, the total charge is approximately

$$Q \approx NGq_e. \quad (2)$$

Consequently, measuring the charge associated with each pulse provides information about the number of detected photons and, indirectly, about the particle interaction that produced them [2–4].

Despite their internal gain, SiPM output signals are fast and of relatively low amplitude. The detector also presents a non-negligible capacitance, which directly affects the behaviour and stability of the readout electronics. A suitable front-end circuit is therefore required to convert these short current pulses into voltage signals that can be reliably measured and digitised [2, 3, 6].

In this work, the Hamamatsu S13360-3050CS SiPM is considered. Its electrical response is represented by an equivalent circuit and used to determine the charge corresponding to a one-photoelectron event, which is then used to dimension the readout circuit [2].

1.2 Charge-Sensitive Amplifiers

A Charge-Sensitive Amplifier (CSA) converts the charge delivered by a detector into a voltage signal. In its basic form, the detector current is applied to the inverting input of an operational amplifier with a feedback capacitor C_f , so that the pulse charge is integrated on the capacitor. For an ideal CSA, the output variation is approximately

^ae-mail: pedro.sousa.silva@tecnico.ulisboa.pt

$$\Delta V_{\text{out}} = -\frac{Q}{C_f}, \quad (3)$$

where Q is the charge delivered by the detector [6]. Unlike a conventional voltage amplifier, the output amplitude is therefore primarily determined by the total event charge rather than by the instantaneous peak value or exact temporal shape of the detector current pulse. This is advantageous for SiPM readout, where the quantity of interest is the charge associated with each event [6].

A resistor R_f is commonly placed in parallel with C_f to discharge the feedback capacitor between events. The resulting decay is characterised approximately by

$$\tau = R_f C_f, \quad (4)$$

where τ is the feedback time constant. It must be long enough to allow the detector charge to be integrated with limited loss, while remaining short enough to avoid excessive dead time and pulse pile-up [6].

In practice, the CSA response is affected by the operational-amplifier characteristics and by detector and PCB parasitic capacitances. These effects are especially important at the inverting node and in the feedback network, making component selection and PCB layout critical for stable low-charge measurements [6, 7].

2 Methodology

The proposed front-end system was designed and simulated in Altium Designer. The workflow comprised three main stages: implementation of the electronic schematic, SPICE validation of the analogue circuitry, and physical design of the printed circuit board (PCB). The schematic included the SiPM equivalent model, the charge-sensitive amplifier, the second amplification stage, the reset and comparator circuits, the ADC, and the STM32-based control electronics.

Manufacturer SPICE models were used whenever available. When no native model was available, external manufacturer models were imported where possible. For the SiPM, an equivalent electrical circuit based on the Corsi model was implemented and parameterised using data from the Hamamatsu S13360-3050CS datasheet [1, 2].

The PCB was then routed with particular attention to the analogue front-end and the CSA inverting node, where parasitic capacitance and electromagnetic coupling are most critical. This iterative design–simulation–layout process allowed the system to be refined before experimental implementation.

3 SiPM Modelling

3.1 Equivalent Circuit Based on the Corsi Model

The SiPM was represented using the equivalent-circuit model proposed by Corsi et al. [1]. This model represents

the detector by a network of resistive and capacitive elements together with a current source. The circuit was parameterised for the Hamamatsu S13360-3050CS using the manufacturer’s datasheet [2].

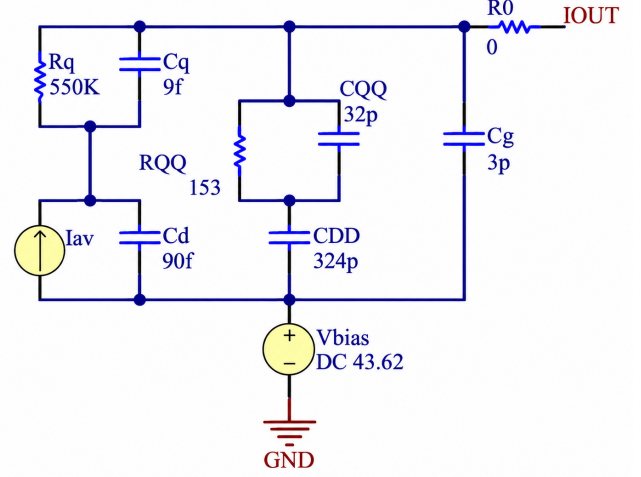


Figure 1: Corsi equivalent circuit for the SiPM considered in this work, implemented in Altium Designer.

The resistor and capacitor values of the equivalent circuit were obtained using the procedure described by Corsi et al. together with the values published in the manufacturer’s datasheet [1, 2].

The current source was modelled as a fast pulse with linear rise and fall times and a total charge equal to that expected for a one-photoelectron event. The pulse charge is calculated as $Q = Gq_e$, where G is the SiPM gain and q_e is the elementary charge [2, 3]. Using the gain of the SiPM considered here, $Q = 1.7 \times 10^6 \times 1.602 \times 10^{-19} \text{ C} = 272 \text{ fC}$. The current source was therefore defined as follows:

Parameter	Value	Description
I_{low}	0 A	Low-state current
I_{high}	22.67 μA	Maximum pulse current
t_d	2 μs	Initial delay
t_r	10 ns	Rise time
t_f	10 ns	Fall time
t_{on}	2 ns	Duration at maximum current
T	2.5 μs	Pulse period
N	0	Number of cycles

Table 1: Parameters of the current source used in the SiPM model.

3.2 SPICE Simulation of the Equivalent Circuit

To validate the equivalent SiPM model and study the behaviour of a one-photoelectron pulse, a 4 μs transient simulation was performed. The current-source pulse occurs at 2 μs , and a time step of 0.05 ns was used. The resulting waveform is shown below:

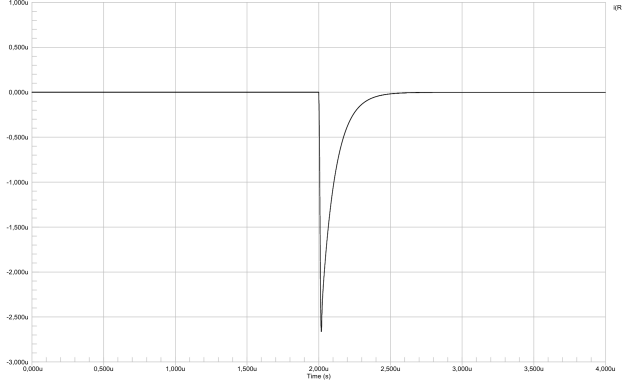


Figure 2: Transient simulation of the SiPM response to a one-photoelectron event.

The waveform is negative, with a rapid transition to approximately $-2.6\mu\text{A}$ followed by a slower exponential return to zero. The signal takes approximately $0.5\mu\text{s}$ to decay from 100% to 1% of its peak value, which corresponds to a time constant of $\tau \approx 109\text{ ns}$.

4 Implementation of the CSA and Associated Electronics

4.1 CSA Circuit

The amplification chain was implemented as a two-stage circuit, consisting of a first charge-sensitive integrating stage followed by a second inverting-amplifier stage.

For the first amplification stage, the Texas Instruments OPA656 operational amplifier was selected. The OPA820 was initially considered because it had previously been implemented in a transimpedance topology. However, the OPA820 has bipolar inputs and an input bias current of the order of microamperes, with a specified maximum of $16\mu\text{A}$ [9]. When this current flows through the feedback resistor, it can produce a significant voltage drop and shift the amplifier output by several hundred millivolts. The OPA656 was therefore selected instead. Its JFET input stage provides a typical input bias current of approximately 2 pA and a specified maximum of 5 pA , greatly reducing the corresponding DC output offset [8].

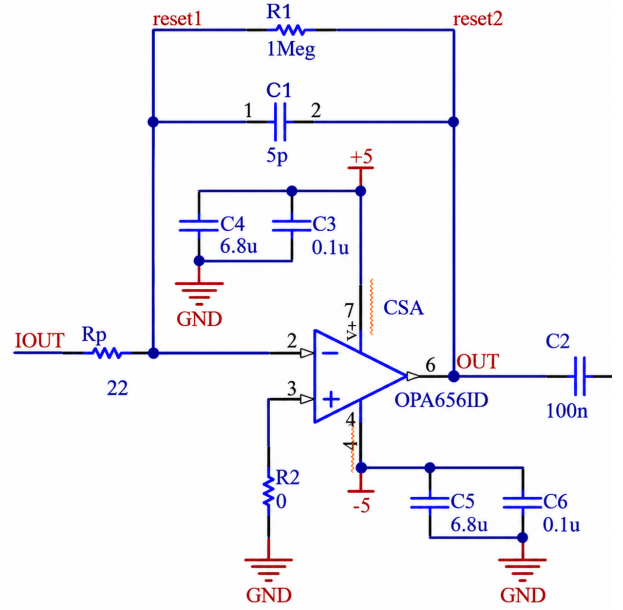


Figure 3: Circuit of the first amplification stage.

The amplifier is powered from $\pm 5\text{ V}$ supplies, in accordance with the manufacturer's specifications [8]. Its feedback network consists of a 5 pF capacitor and a $1\text{ M}\Omega$ resistor. The charge-to-voltage conversion sensitivity of the ideal CSA is therefore $1/C_f = 2 \times 10^{11}\text{ V/C}$, while the associated feedback time constant is $\tau = R_f C_f = (1\text{ M}\Omega)(5\text{ pF}) = 5\mu\text{s}$.

For a one-photoelectron signal, the charge associated with the SiPM pulse is approximately 272 fC . The expected output amplitude of the first stage is therefore $V = Q/C_f = (272\text{ fC})/(5\text{ pF}) \approx 54\text{ mV}$, which is sufficiently large to be read and processed comfortably. The equivalent SiPM model produces a one-photoelectron pulse with a characteristic decay time of approximately 109 ns , whereas the CSA feedback time constant is much larger. This allows the pulse charge to be measured without excessive discharge of the feedback capacitor during the detector pulse. Indeed, during the approximately $0.5\mu\text{s}$ required for the SiPM pulse to decay from 100% to 1%, a $5\mu\text{s}$ exponential CSA decay would reduce the stored signal by only about 9.5%.

A 22Ω resistor was placed before the amplifier inverting input in order to improve circuit stability in the presence of the SiPM capacitance. Directly connecting a capacitive load to the input of a wide-bandwidth amplifier such as the OPA656 can introduce additional high-frequency phase shift and promote ringing or even oscillation. The resistor provides a small amount of isolation between the detector and the inverting node, damping these high-frequency components. A value of 22Ω was chosen because it is small enough not to significantly degrade the signal timing while still providing useful damping and improved stability. This resistor does not determine the CSA discharge time constant, which remains primarily set by the feedback network according to $\tau = R_f C_f$ [7].

A resistor equal to the feedback resistance can also be placed at the non-inverting input of an operational amplifier to compensate for the voltage offset produced by input bias currents. In this circuit, however, such a large resistor would add significant thermal noise, and the JFET inputs of the OPA656 already provide an extremely low bias current. For this reason, this compensation resistor was not included.

The first stage is followed by a second amplification stage implemented as an inverting amplifier. This topology was selected because the first-stage output pulse is negative, so the inverting stage produces a positive output signal.

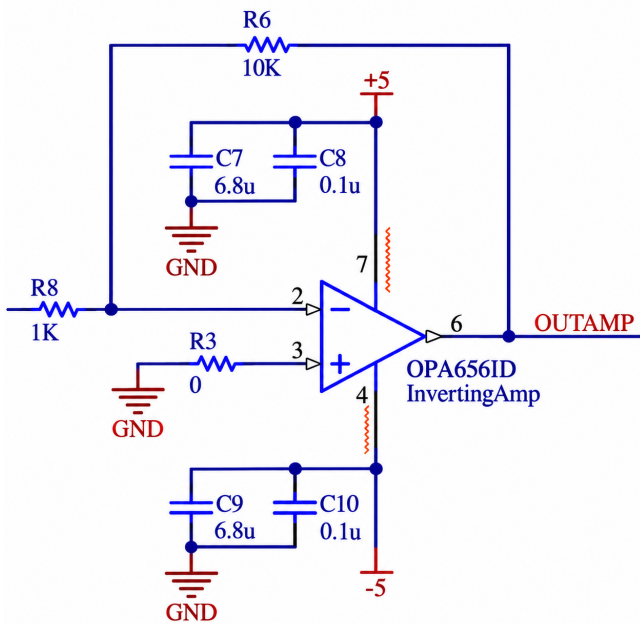


Figure 4: Circuit of the second amplification stage.

The OPA656 was again selected for the second amplification stage for the same reasons discussed above [8]. A coupling capacitor of $C = 100$ nF is placed before the inverting input of the second-stage OPA656. Together with the input resistance, it forms a high-pass coupling network and removes any residual DC offset from the previous stage.

The second-stage feedback network consists of a 10 kΩ resistor between the output and the inverting input and a 1 kΩ resistor between the inverting input and the coupling capacitor. This configuration implements an inverting gain of -10 , so a one-photoelectron signal with a first-stage amplitude of approximately 54 mV is expected to produce a second-stage amplitude of approximately 10×54 mV = 540 mV, with opposite polarity.

To stabilise the amplifier supply rails in both amplification stages, decoupling capacitors are placed at the supply pins. Each supply rail uses a 0.1 μF capacitor together with a 6.8 μF capacitor, following the manufacturer's recommendations [8].

4.2 Reset and Comparator Circuit

To increase the achievable acquisition rate and allow the system to measure a larger number of events without saturating the charge amplifier, a reset mechanism was implemented to discharge the feedback capacitor between events.

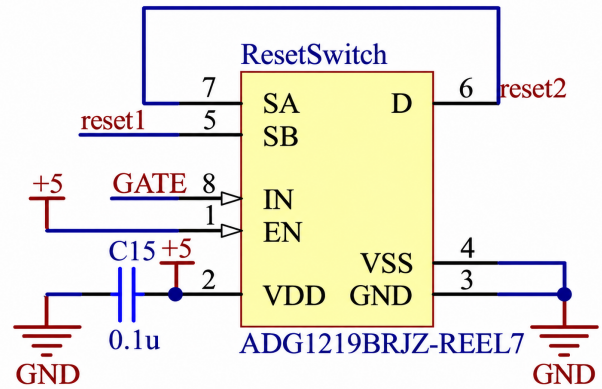


Figure 5: Reset-mechanism circuit.

The ADG1219 [11] was selected as the reset element because it is a CMOS single-pole double-throw (SPDT) analogue switch specifically characterised for low charge injection and low leakage current. Its charge injection is specified below 0.5 pC over the full signal range, with values on the order of 0.1 pC under some operating conditions, while its leakage current is specified up to approximately 0.6 nA at 85°C [11].

The ADG1219 is connected in parallel with the feedback capacitor and is controlled by the digital control circuit.

To determine when the reset mechanism should switch and discharge the feedback capacitor, a comparator circuit was also implemented. It receives the output signal from the second amplification stage and determines whether that signal exceeds a reference value set by the control circuit.

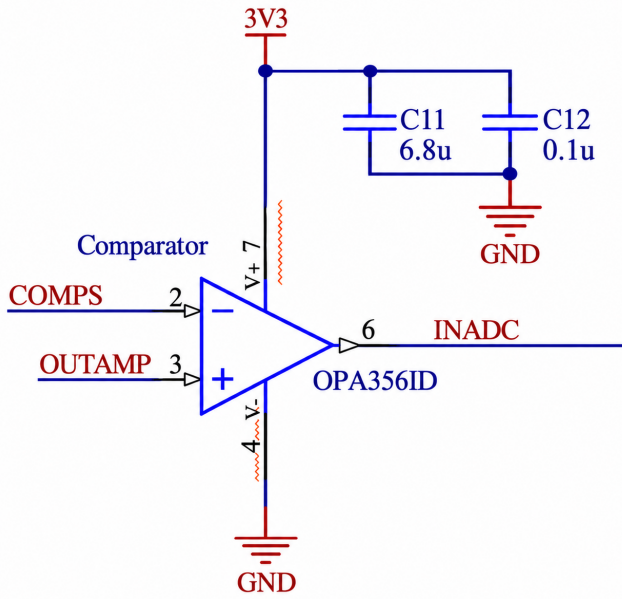


Figure 6: Comparator circuit.

This circuit was implemented using an operational amplifier in open-loop configuration. The OPA356 was selected because it provides rail-to-rail output operation and supports single-supply operation [10]. It can therefore be powered from GND and 3.3 V, producing output levels close to the two supply rails depending on whether the input signal is below or above the reference value imposed by the control circuit. Since the OPA356 output does not reach the rails exactly, these levels are approximately, rather than ideally, 0 V and 3.3 V.

4.3 ADC, Control, and Communication Circuitry

To make the output signals of both amplification stages externally accessible, each amplifier output was connected to a LEMO connector. These connectors support coaxial, shielded connections, helping to minimise externally coupled electromagnetic noise. Since coaxial cables can add significant capacitive loading, a 50 Ω series resistor was placed between each amplifier and its corresponding connector to isolate the amplifier from the cable capacitance [7]. A 50 Ω resistor to GND was also added at each connector to provide a local termination and reduce signal reflections.

To digitise the amplifier output signal, an Analog-to-Digital Converter (ADC) is required. The LTC2315ITS8-12 was selected; it is a 12-bit, 5 MSPS ADC and can therefore acquire samples at intervals as short as 200 ns [12].

A control circuit was required to manage the ADC as well as the comparator and reset mechanism.

The control circuit was based on the STM32G431CBT6 microcontroller from the STM32 family, selected because it provides substantial processing capability while remaining relatively straightforward to implement [13, 14]. The microcontroller sets the comparator reference voltage and, when a positive comparator

output is received, initiates ADC acquisition. After a short delay, it then switches the reset mechanism to discharge the feedback capacitor and begin a new measurement cycle.

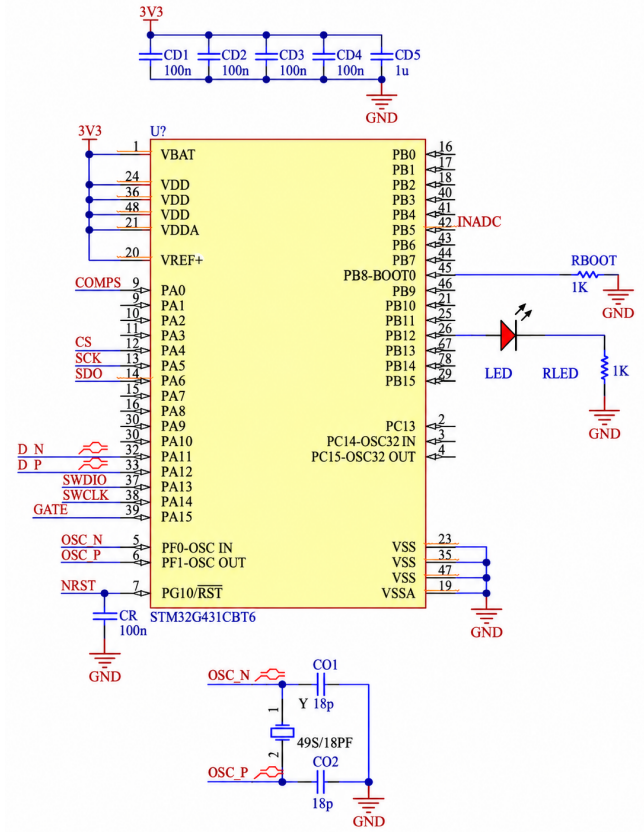


Figure 7: STM32 and associated connections.

To communicate the digitised ADC data externally, a USB-C connector connected to the microcontroller was also included. A TVS-diode array is placed close to the USB-C interface to protect the circuit against electrostatic-discharge and transient overvoltage events associated with cable connection [15].

4.4 SPICE Simulations of the Analogue Electronics

Several transient simulations were performed at different points in the circuit in order to validate and study the behaviour of the CSA electronics.

An 18 μ s simulation with a 0.05 ns time step was performed to study the response of the two amplification stages to a one-photoelectron signal. The first-stage simulation result is shown below:

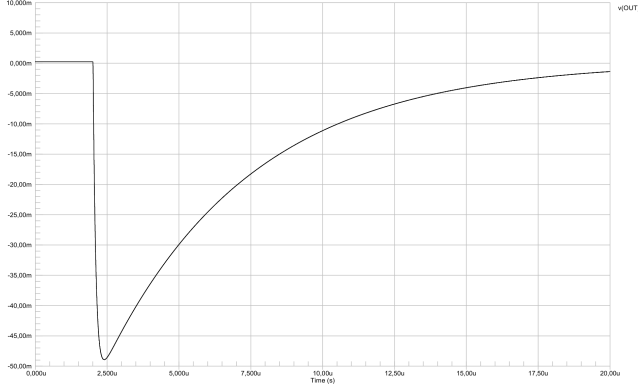


Figure 8: Response of the first amplification stage to a one-photoelectron pulse.

The simulation shows that the signal has the expected general shape and is both amplified and temporally extended. Its amplitude is approximately 49 mV, which is close to the previously predicted 54 mV. Over the simulated interval, the pulse decreases from 100% to approximately 2% in about 18 μ s. Interpreted as a single exponential over this limited range, this corresponds to an apparent time constant of approximately 4.60 μ s. This value is very similar to the nominal $R_f C_f = 5 \mu$ s time constant and is therefore in good agreement with the theoretical value. As expected, the pulse is negative and lies in the negative-voltage region.

The behaviour of the second amplification stage was also simulated using a 20 μ s transient simulation with a 0.05 ns time step. The resulting waveform is shown below:

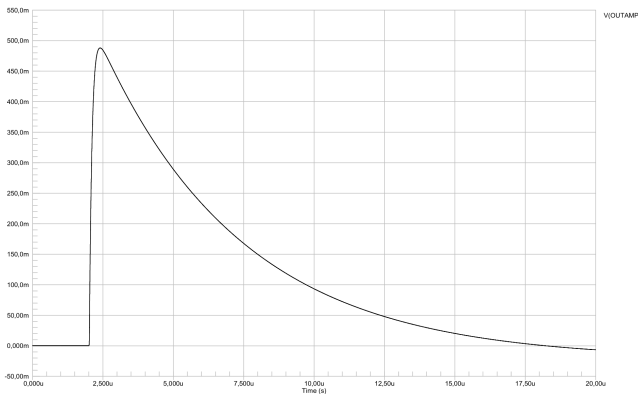


Figure 9: Response of the second amplification stage to a one-photoelectron pulse.

The pulse duration remains essentially unchanged, while the polarity is inverted from negative to positive and the amplitude increases by a factor of 10, from approximately 49 mV to 490 mV.

To simulate the behaviour of the reset mechanism and comparator, a 20 μ s simulation with a 0.05 ns time step was performed, and the second-stage output and comparator waveforms were recorded. In this simulation, the SiPM produces a pulse every 5 μ s, while the switch also commu-

tates every 5 μ s but with a delay of 2.5 μ s relative to the SiPM pulse.

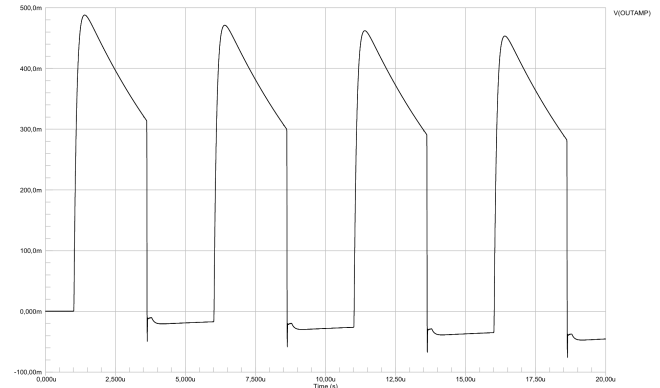


Figure 10: Second-stage response to a periodic pulse with reset switching.

The reset mechanism behaves as expected, discharging the feedback capacitor when activated. However, an approximately 100 ns delay remains between the instant at which the switch commutates and the discharge of the feedback capacitor.

Despite the very low charge injection of the switch, some residual injected charge is still observed. As a result, the reset leaves the amplifier output at approximately -20 mV rather than 0 V. This offset is small compared with the signal amplitude of approximately 490 mV, although it slightly affects subsequent pulses. Since its magnitude is known, its effect can be corrected during signal post-processing.

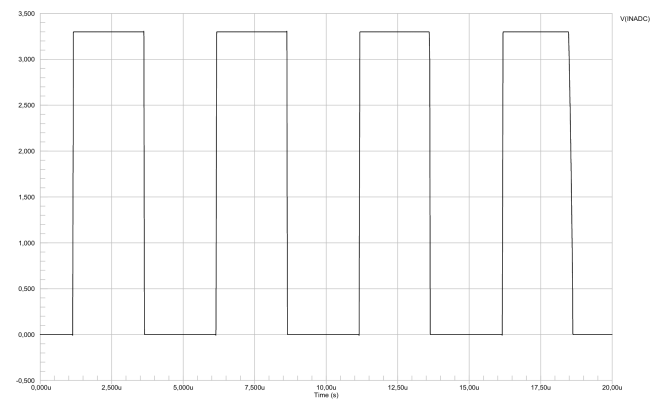


Figure 11: Comparator response to a periodic pulse with reset switching.

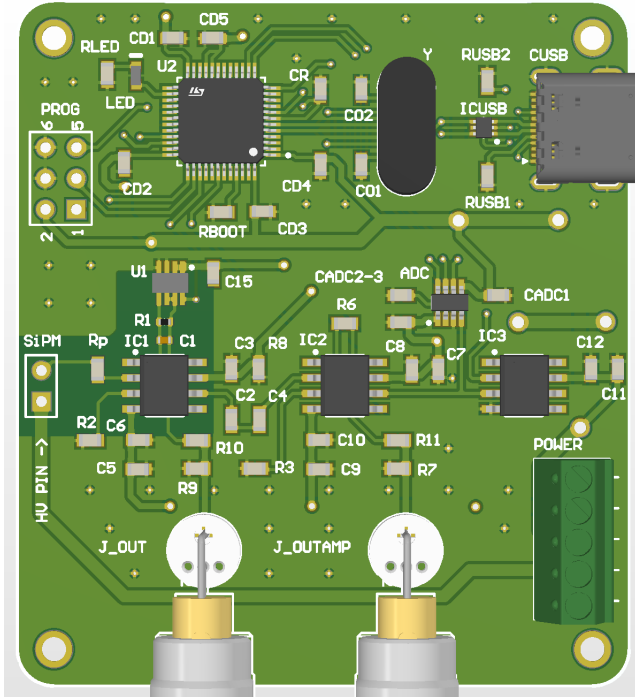
For the comparator simulation, the reference voltage was arbitrarily set to 300 mV. The comparator exhibits the expected behaviour, remaining near 0 V while the amplifier signal is below 300 mV and switching to a level close to 3.3 V when the signal exceeds this threshold.

5.1 Design Considerations

The circuit developed above must be implemented on a PCB so that it can subsequently be tested on the laboratory bench. PCB design is particularly important because it can influence system stability and because parasitic capacitance introduced by the physical implementation can affect CSA operation. The PCB must therefore integrate the CSA and the analogue electronics while limiting both parasitic capacitance and electromagnetic noise [6, 7].

5.2 PCB Implementation of the System

To minimise the influence of the control electronics on the CSA, particularly through added noise, the PCB was divided into two main regions: one containing the two amplification stages and the comparator, and another containing the STM32-based control circuitry.



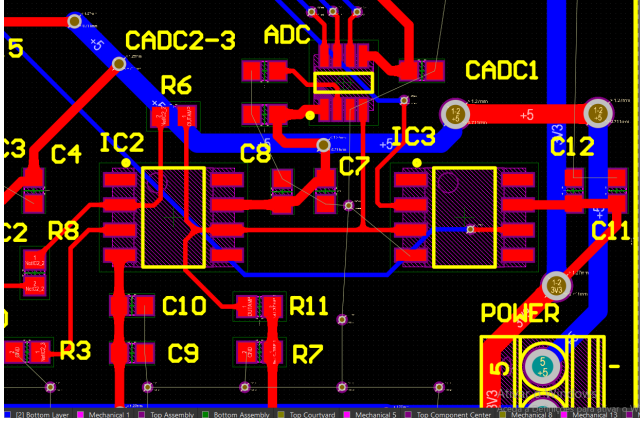


Figure 14: Second amplification stage (IC2), comparator (IC3), and ADC. R6 and R8 form the feedback network of the inverting amplifier.

The comparator follows the second amplification stage and was implemented using layout precautions similar to those applied to the preceding analogue circuits.

In this region of the board, signal traces with a width of 0.254 mm were used because high currents are not expected and narrower traces help reduce parasitic capacitance. Power traces, however, were made approximately 0.5–1 mm wide to provide additional current-carrying capability and reduce resistive heating.

The control circuit was implemented in a separate region of the PCB in order to reduce electromagnetic-noise coupling and parasitic coupling into the CSA. The STM32 decoupling capacitors were placed close to the microcontroller to improve supply stability [13, 14]. The oscillator was placed as far as practical from the inverting node of the first amplification stage because its switching activity can increase EMI coupling into this sensitive node. A programming connector was also placed close to the STM32, and the ADC was positioned between the second amplification stage and the STM32.

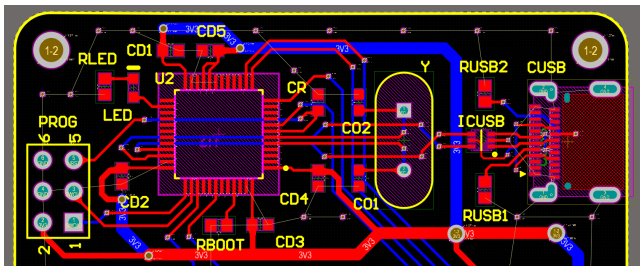


Figure 15: Control circuit with the STM32 (U2), oscillator (Y), and USB-C connector.

The LEMO connectors were placed close to the CSA to minimise the length of the corresponding signal traces. The board power connector was placed as far as practical from the first-stage inverting node in order to reduce unwanted coupling. The USB connector was likewise placed away from the CSA and at the edge of the board.

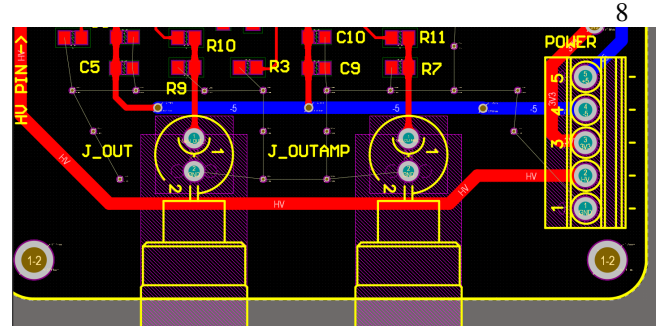


Figure 16: LEMO connectors (J_OUT and J_OUTAMP) and the power connector.

A GND plane was added across most of the board to provide a low-impedance ground reference, reduce EMI, and improve heat spreading.

Finally, rounded board corners were added for safety and mounting holes were included for practical assembly.

5.3 Parasitic Capacitance Analysis

To analyse the effects of parasitic capacitance on the PCB, the method described by Peterson was applied [16].

The most critical region of the CSA with respect to parasitic capacitance is the inverting node of the first amplification stage, since any additional capacitance at this high-impedance node can directly alter the noise gain, frequency response, and stability of the amplifier [6, 7].

Parasitic capacitance at this node arises mainly from two mechanisms: coupling between the trace and nearby copper planes, and coupling between the trace and neighbouring signal traces [16].

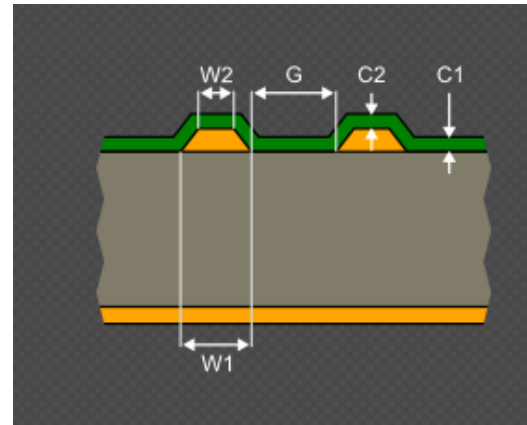


Figure 17: Copper planes and neighbouring traces introduce parasitic capacitance.

Using the Altium tools described by Peterson [16], the capacitance per unit length between the inverting-node trace and the GND plane was estimated as 85.93465 pF/m. Since the inverting-node trace is 15 mm long, this corresponds to a parasitic capacitance of $(85.93465 \text{ pF/m})(15 \text{ mm}) = 1.289 \text{ pF}$, or approximately 25.8% of the nominal 5 pF CSA feedback capacitance. This is a significant contribution.

To suppress this contribution, the GND plane was removed in the region around the inverting node by defining a copper keepout. Parasitic capacitance due to coupling with neighbouring copper traces nevertheless remains.

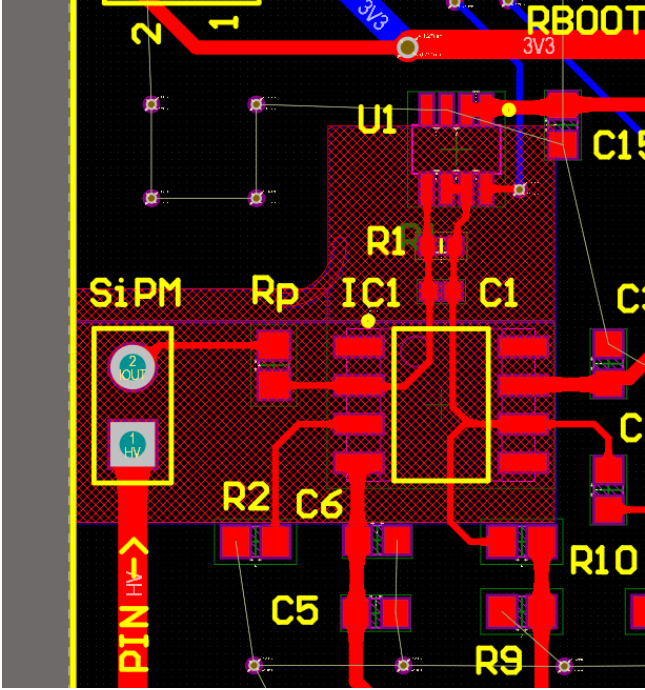


Figure 18: Region around the CSA inverting node with a GND-plane keepout.

The output-node trace is, on average, approximately 0.5 mm away from the inverting-node trace. Following the method described by Peterson [16], the associated mutual parasitic capacitance was estimated as 5.685 pF/m. For a 15 mm trace, this corresponds to $(5.685 \text{ pF/m})(15 \text{ mm}) = 85.3 \text{ fF}$, which is approximately 1.71% of the nominal CSA feedback capacitance. This contribution is considerably more acceptable. Thus, removing the GND plane from both copper layers in the region surrounding the first-stage inverting node reduced the dominant parasitic-capacitance contribution by a factor of approximately 15.

6 Conclusion and Future Work

The first objective of this work was to implement and validate, in Altium Designer, a charge-sensitive front-end capable of measuring signals at the single-photoelectron level from the Hamamatsu S13360-3050CS SiPM. The SiPM equivalent model established a one-photoelectron charge of approximately 272 fC, which was used as the reference input for the front-end design. A feedback network with $C_f = 5 \text{ pF}$ and $R_f = 1 \text{ M}\Omega$ was found to provide a suitable compromise between charge sensitivity and discharge time, corresponding to an ideal conversion of approximately 54 mV per photoelectron and a feedback time constant of 5 μs . The simulated first-stage amplitude of approximately 49 mV and apparent decay constant of

4.60 μs are close to these theoretical values, supporting the selected CSA dimensioning.

The simulations also showed that the second inverting stage provides the intended polarity reversal and gain of 10, increasing a one-photoelectron signal to approximately 490 mV and therefore providing a more convenient signal level for digitisation. The reset architecture based on the ADG1219 successfully discharges the CSA feedback capacitor, although a residual offset of approximately -20 mV remains due to charge injection. This result indicates that the switch is suitable for the intended reset function, while also showing that the residual offset should be characterised experimentally and, if necessary, compensated in post-processing. The comparator simulation likewise confirmed that the threshold-detection concept can generate a digital-level trigger for the control electronics.

A second objective was to translate the analogue design into a PCB while limiting the parasitic effects that are especially critical at the CSA inverting node. The layout analysis showed that a nearby GND plane would contribute approximately 1.289 pF to a 15 mm inverting-node trace, corresponding to about 25.8% of the nominal 5 pF feedback capacitance. This result demonstrated that a conventional uninterrupted ground plane is not appropriate directly beneath this high-impedance node. Introducing a keepout on both copper layers removes the dominant plane-coupling contribution, leaving an estimated mutual capacitance of approximately 85.3 fF to the neighbouring output trace, or about 1.71% of C_f . The analysis therefore supports the adopted layout strategy of minimising critical trace length, placing the feedback network close to the OPA656, using small 0402 components in the most sensitive region, and separating the analogue and digital sections of the board.

The next stage of the project is the experimental characterisation of the assembled PCB with a real SiPM. This should include measurement of the single-photoelectron response, noise and signal-to-noise ratio, comparison of the measured gain and decay time with the SPICE predictions, verification of the reset-induced offset, and evaluation of the maximum sustainable event rate. The ADC, STM32 control logic, comparator threshold generation, and USB-C data transfer should also be validated as a complete acquisition chain. These measurements will determine how closely the implemented hardware follows the simulated behaviour and whether further optimisation of the CSA, reset network, or PCB layout is required.

Acknowledgements

I would like to express my sincere gratitude to my supervisors, Prof. Pedro Assis and Manuel Ratola, for their continuous guidance, support, and valuable feedback throughout the development of this project. I would also like to thank Miguel Ferreira, from the Electronics Laboratory, for his availability, technical assistance, and invaluable help throughout the different stages of the work. Finally, I would like to thank LIP – Laboratório de Instrumentação e Física Experimental de Partículas for providing me with the opportunity to carry out this project in a

stimulating and collaborative environment, which allowed me to further develop my technical knowledge, gain valuable practical experience, and learn more about the challenges involved in the development of instrumentation for experimental physics.

References

- [1] F. Corsi, A. Dragone, C. Marzocca, A. Del Guerra, P. Delizia, N. Dinu, C. Piemonte, M. Boscardin and G. F. Dalla Betta, *Modelling a Silicon Photomultiplier (SiPM) as a Signal Source for Optimum Front-End Design*, Nuclear Instruments and Methods in Physics Research Section A, vol. 572, no. 1, pp. 416–418, 2007. doi: 10.1016/j.nima.2006.10.219.
- [2] Hamamatsu Photonics K.K., *MPPC S13360-3050CS – MPPC for Precision Measurement*, manufacturer datasheet. Product page: https://www.hamamatsu.com/eu/en/product/optical-sensors/mppc/mppc_mppc-array/S13360-3050CS.html.
- [3] A. Ghassemi, K. Kobayashi and K. Sato, *A Technical Guide to Silicon Photomultipliers (MPPC)*, Hamamatsu Photonics K.K., 2018.
- [4] F. Simon, *Silicon Photomultipliers in Particle and Nuclear Physics*, Nuclear Instruments and Methods in Physics Research Section A, vol. 926, pp. 85–100, 2019. doi: 10.1016/j.nima.2018.11.042.
- [5] G. F. Knoll, *Radiation Detection and Measurement*, 4th ed., John Wiley & Sons, 2010.
- [6] H. Spieler, *Semiconductor Detector Systems*, Oxford University Press, Oxford, 2005. doi: 10.1093/acprof:oso/9780198527848.001.0001.
- [7] X. Ramus, *Transimpedance Considerations for High-Speed Amplifiers*, Texas Instruments, Application Report SBOA122, 2009.
- [8] Texas Instruments, *OPA656: 550 MHz, Unity-Gain Stable, FET-Input Operational Amplifier*, datasheet, Rev. I, 2024.
- [9] Texas Instruments, *OPA820: Unity-Gain Stable, Low-Noise, Voltage-Feedback Operational Amplifier*, datasheet, Rev. D, 2016.
- [10] Texas Instruments, *OPA356/OPA2356: 200 MHz, Video CMOS Operational Amplifier*, datasheet, Rev. A, 2001.
- [11] Analog Devices, *ADG1219: Low Capacitance, Low Charge Injection, ± 15 V/12 V iCMOS SPDT in SOT-23*, datasheet, Rev. A, 2009.
- [12] Analog Devices, *LTC2315-12: 12-Bit, 5MSPS Serial Sampling ADC in TSOT*, datasheet, 2013.
- [13] STMicroelectronics, *STM32G431x6, STM32G431x8, STM32G431xB: Arm Cortex-M4 32-bit MCU+FPU, 170 MHz*, datasheet DS12589.
- [14] STMicroelectronics, *STM32G4 Series Advanced Arm-Based 32-bit MCUs*, Reference Manual RM0440.
- [15] Texas Instruments, *ESD and Surge Protection for USB Interfaces*, Application Report SLVAF82B, Rev. B, 2024.
- [16] Z. Peterson, *Parasitic Extraction with an Electromagnetic Solver in PCB Routing*, Altium Resources, 2022.
- [17] Vishay, *Frequency Response of Thin Film Chip Resistors*, Technical Note, Document No. 60107, Rev. 04-Feb-09, 2009.
- [18] Texas Instruments, *THS4601: High-Speed FET-Input Operational Amplifier*, datasheet SLOS388B, revised June 2002.
- [19] J. Winkelholz, M. Hitzemann, A. Nitschke, A. Zygmanski, and S. Zimmermann, *Resistive High-Voltage Probe with Frequency Compensation by Planar Compensation Electrode Integrated in Printed Circuit Board Design*, Electronics, vol. 11, no. 21, article 3446, 2022. doi: 10.3390/electronics11213446.