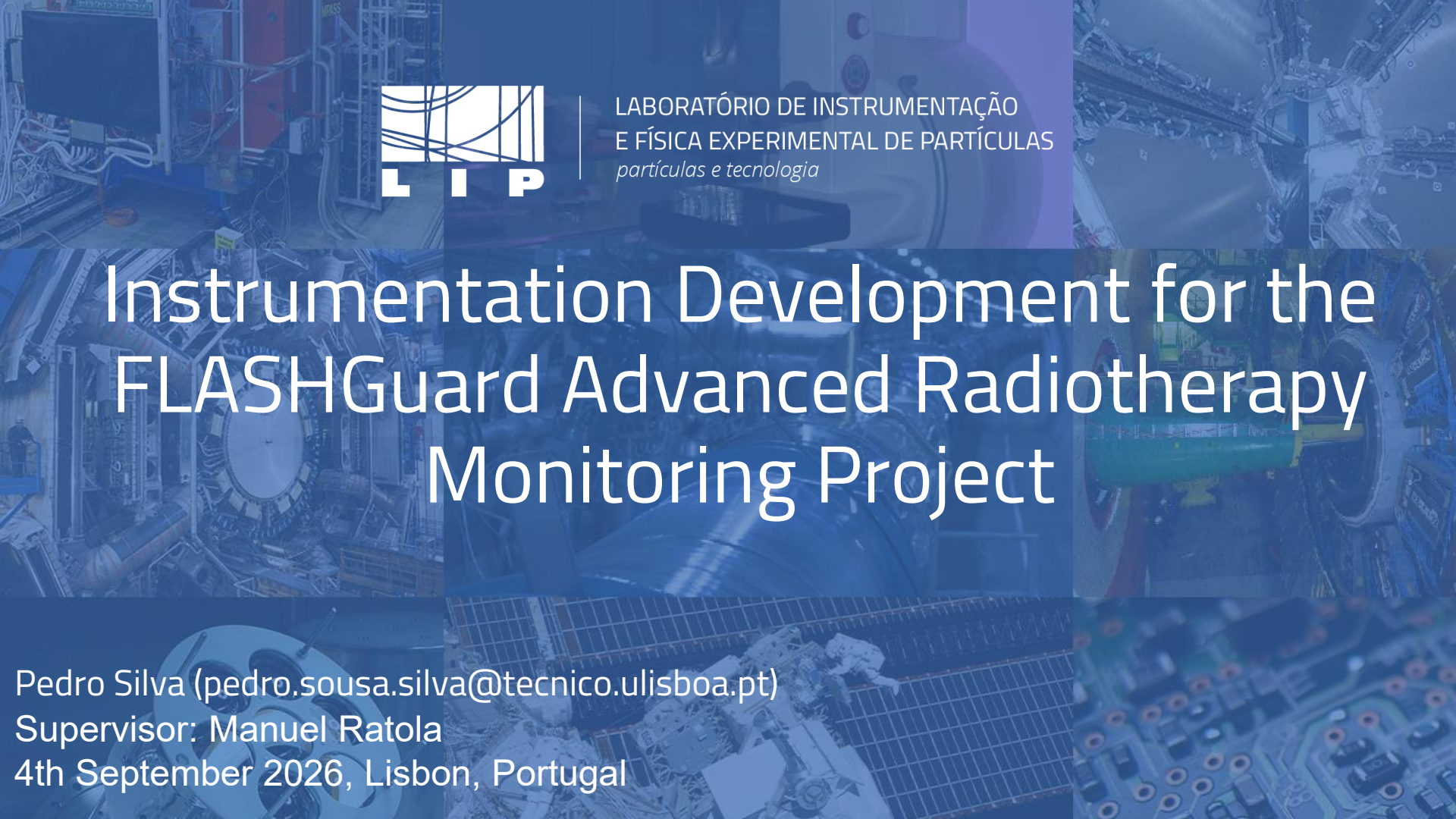

LABORATÓRIO DE INSTRUMENTAÇÃO
E FÍSICA EXPERIMENTAL DE PARTÍCULAS
partículas e tecnologia

Instrumentation Development for the FLASHGuard Advanced Radiotherapy Monitoring Project

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Supervisor: Manuel Ratola
4th September 2026, Lisbon, Portugal

Motivation and Objectives

- SiPM signals are fast and low-amplitude
- Event charge carries information about the number of detected photons
- Front-end electronics are required for signal conditioning and acquisition

- Develop a SiPM readout front-end
- Convert charge into a measurable voltage using a CSA
- Integrate ADC and digital control
- Design a PCB minimising parasitic effects
- Validate the system through SPICE simulations

Silicon Photomultiplier (SiPM)

Photon

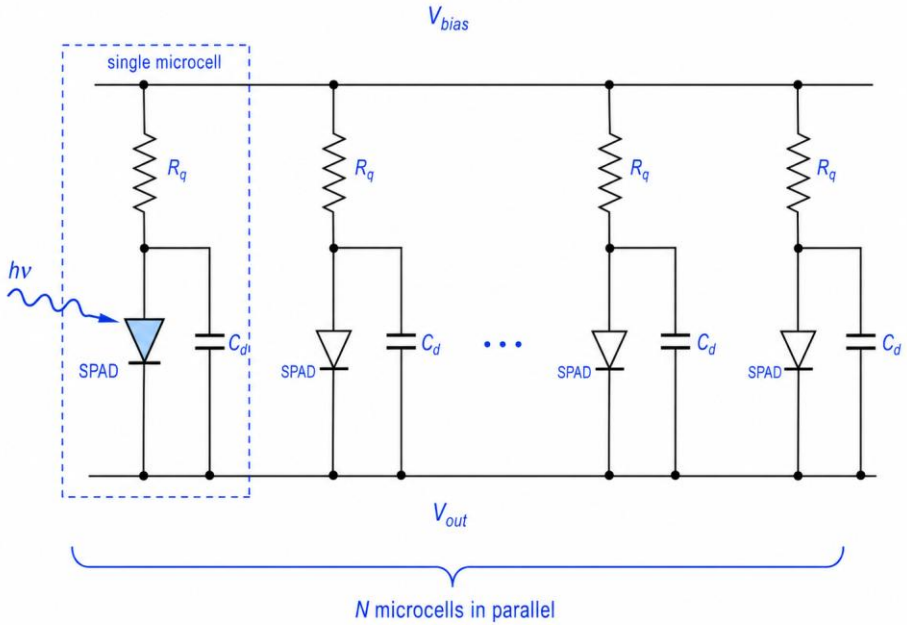
↓

SPAD Avalanche

↓

Pulse

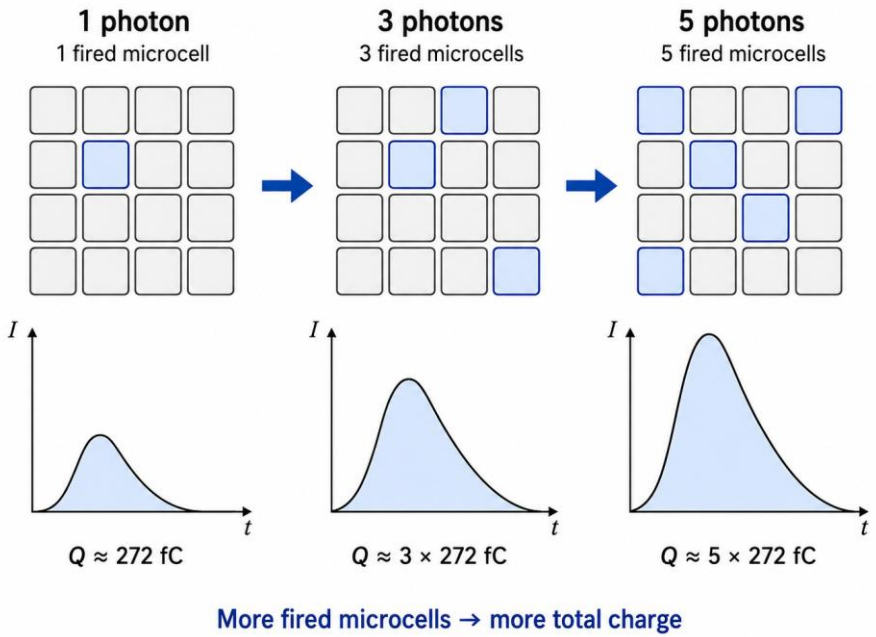
Array of Geiger-mode SPAD microcells connected in parallel



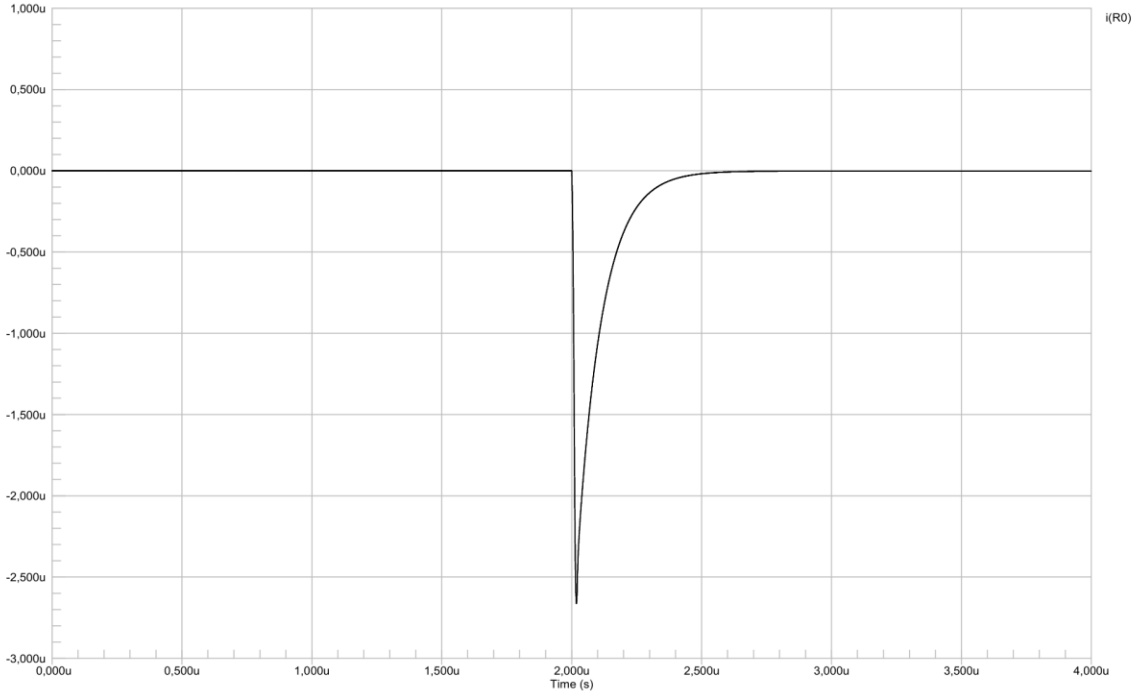
Why Measure Charge

$$Q_{1,p.e.} = G * q_e$$
$$Q_{total} \approx N * G * q_e$$
$$1\ p.e \rightarrow 272fC$$

Total charge ≈ number of fired microcells ≈ number of detected photons



The Readout Challenge



Small and fast signal

For 1 p.e. :

$I = -2{,}6\mu A,$

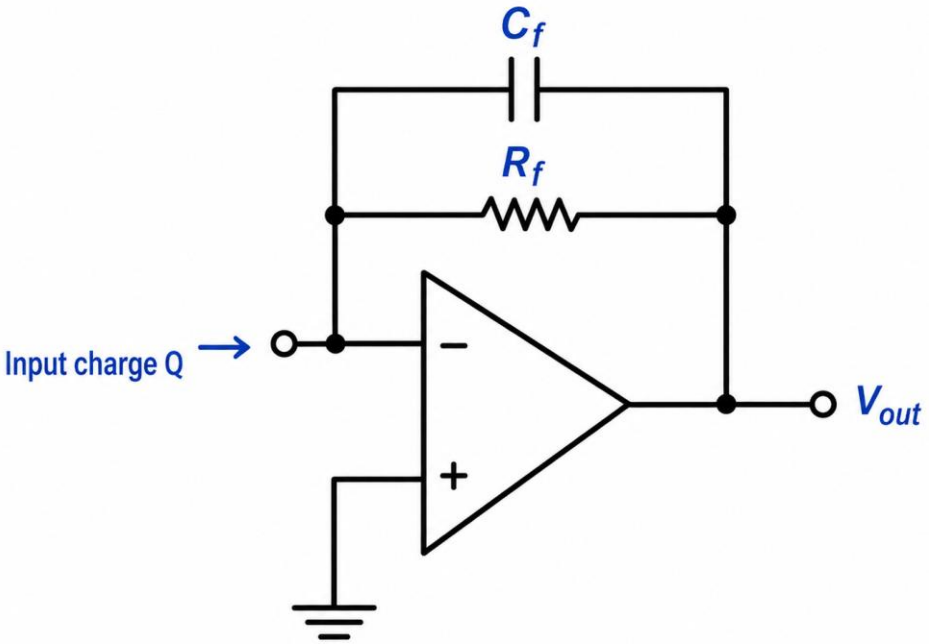
$\tau = 109ns$

Charge-Sensitive Amplifier (CSA)

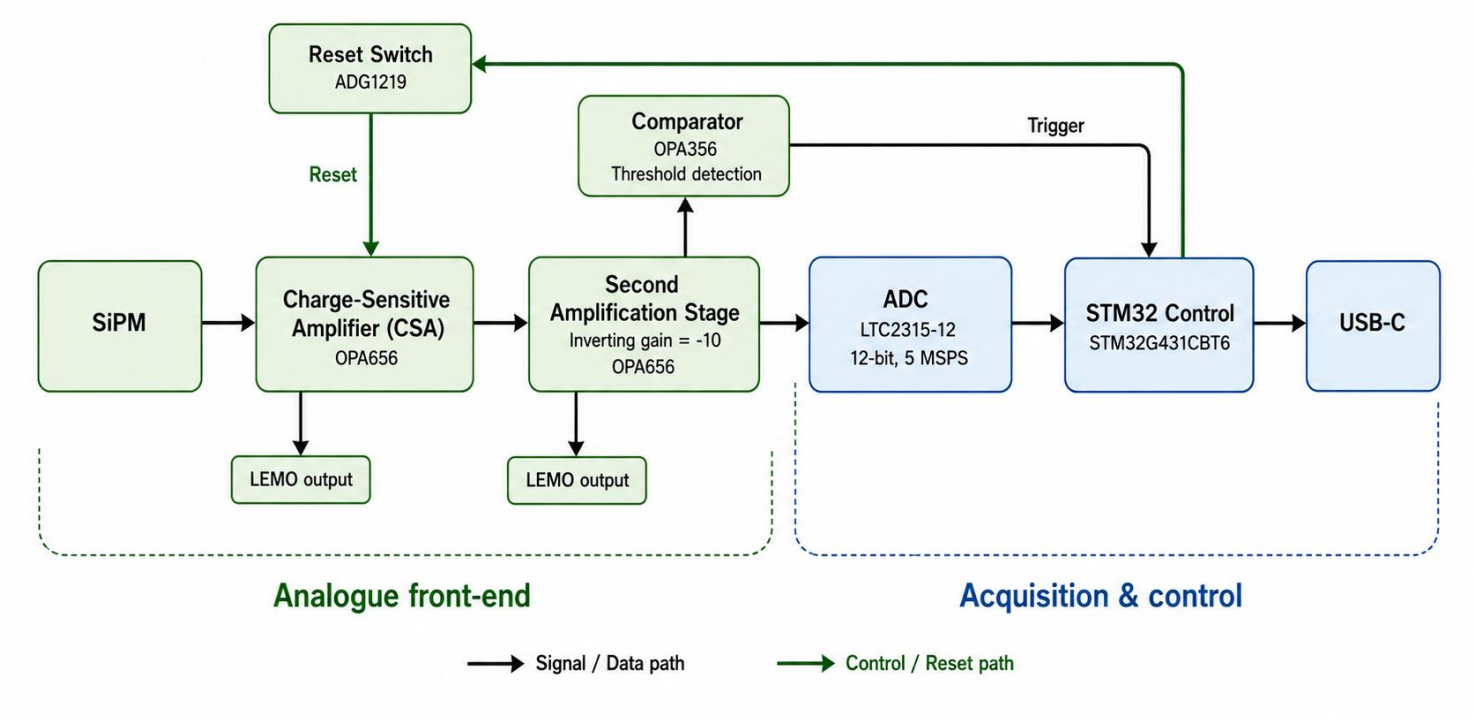
$$\Delta V_{Out} \approx -\frac{Q}{C_f}$$

$$\tau = R_f * C_f$$

The CSA transforms a small current signal in a readable voltage



System Architecture

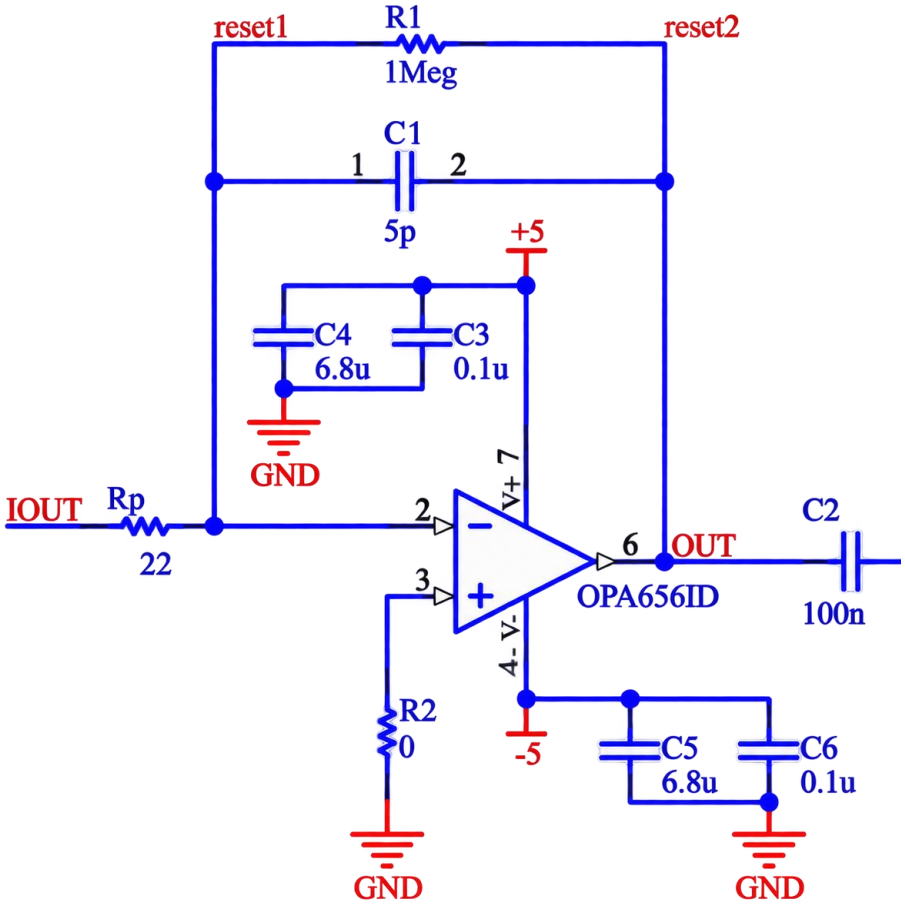


First Stage: CSA

Implemented using the OPA656 (bias current = 2pA).

$$C_f = 5pF, R_f = 1M\Omega.$$
$$\tau = C_f * R_f = 5\mu s$$

1 p.e. -> 54mV expected



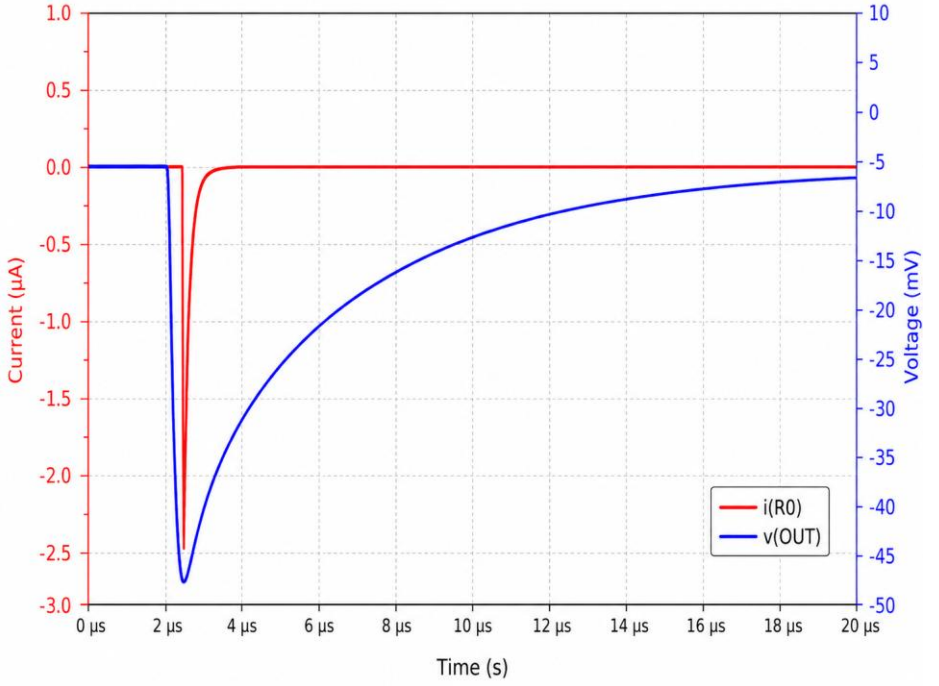
CSA SPICE Simulation

1 p.e. -> 54mV expected

↓

49mV Obtained

Apparent time constant 4,6µs

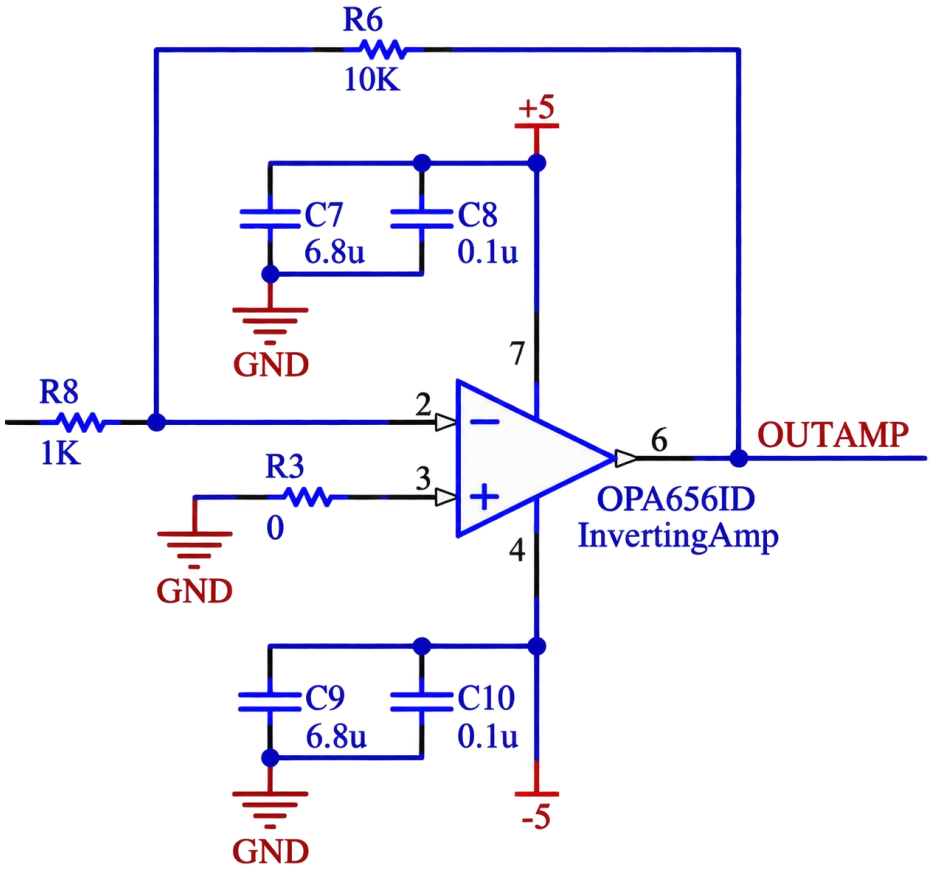


Second Stage: Inverting Amplifier

Implemented using the OPA656 (bias current = 2pA).

$$R_1 = 1K\Omega, R_2 = 10K\Omega$$
$$G = -10\text{x}$$

1 p.e. -> 540mV expected
(after 2nd stage)



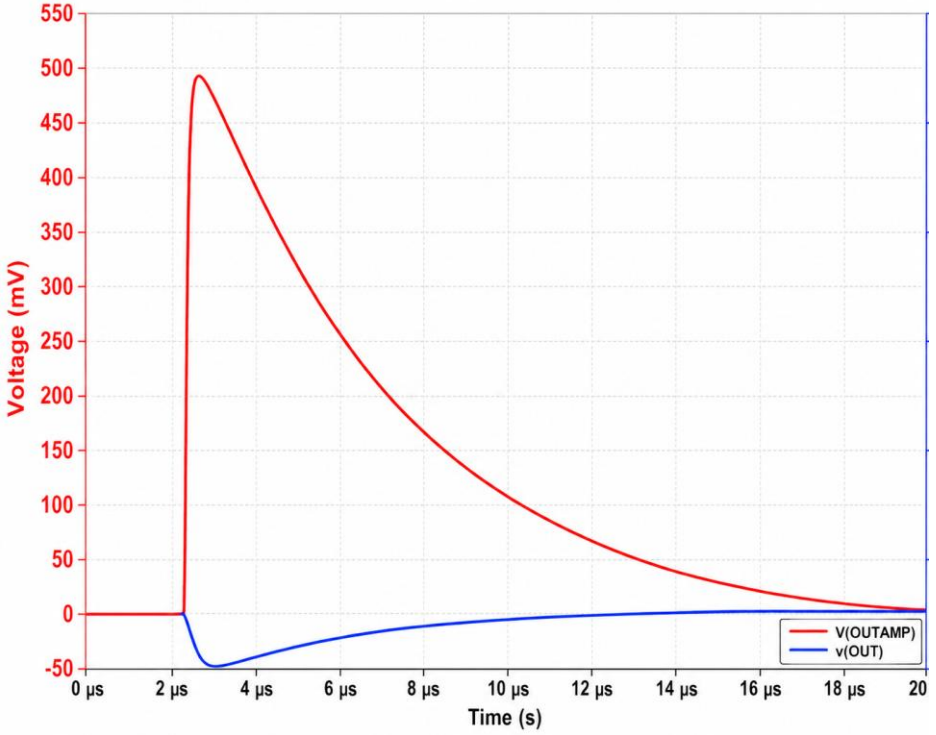
Inverting Amp SPICE Simulation

1 p.e. -> 540mV expected

↓

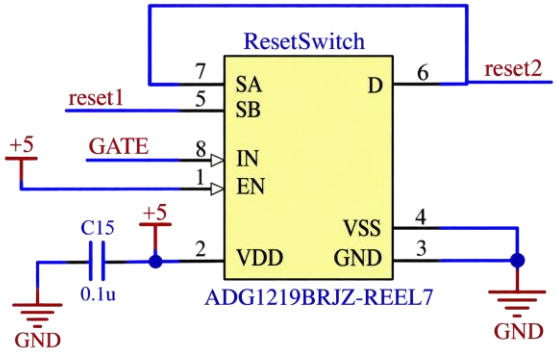
490mV Obtained

Apparent time constant 4,6µs



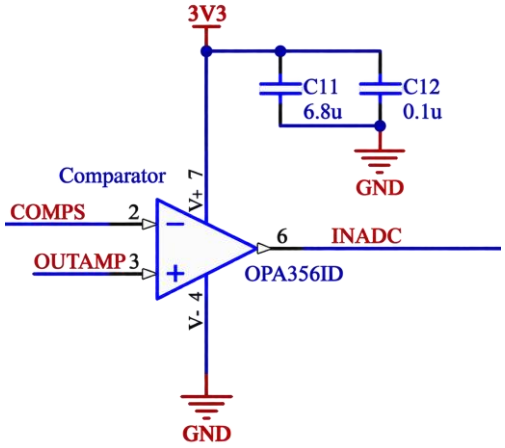
Comparator and Reset Circuit

Reset Switch



CMOS switch in parallel with Cf with very low charge injection

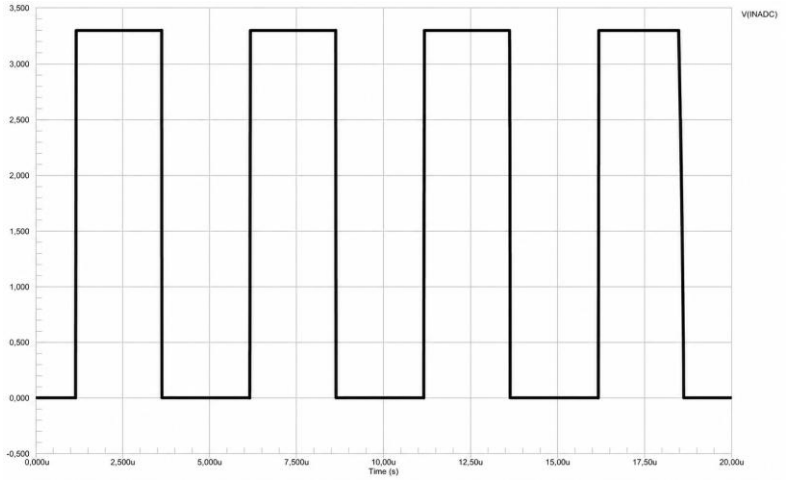
Comparator



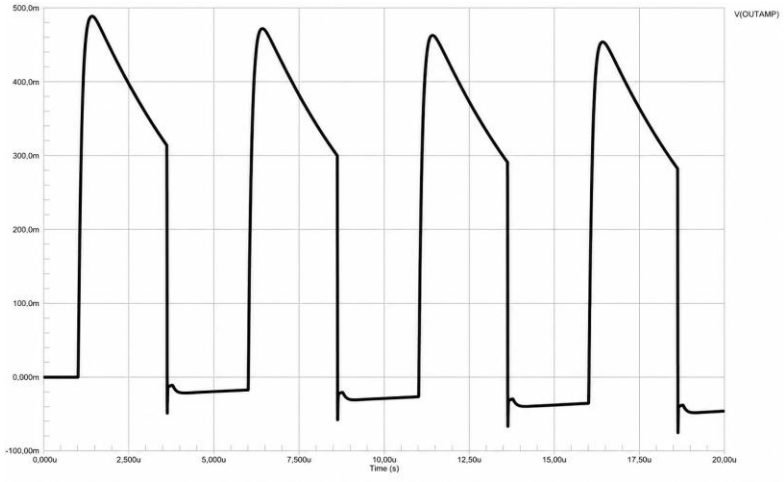
Open-loop, rail-to-rail output, 3.3 V supply

Comparator and switch allow to systematically discharge the CSA feedback, reseting the sample aquisition

Comparator and Reset SPICE Simulation



Comparator SPICE Simulation

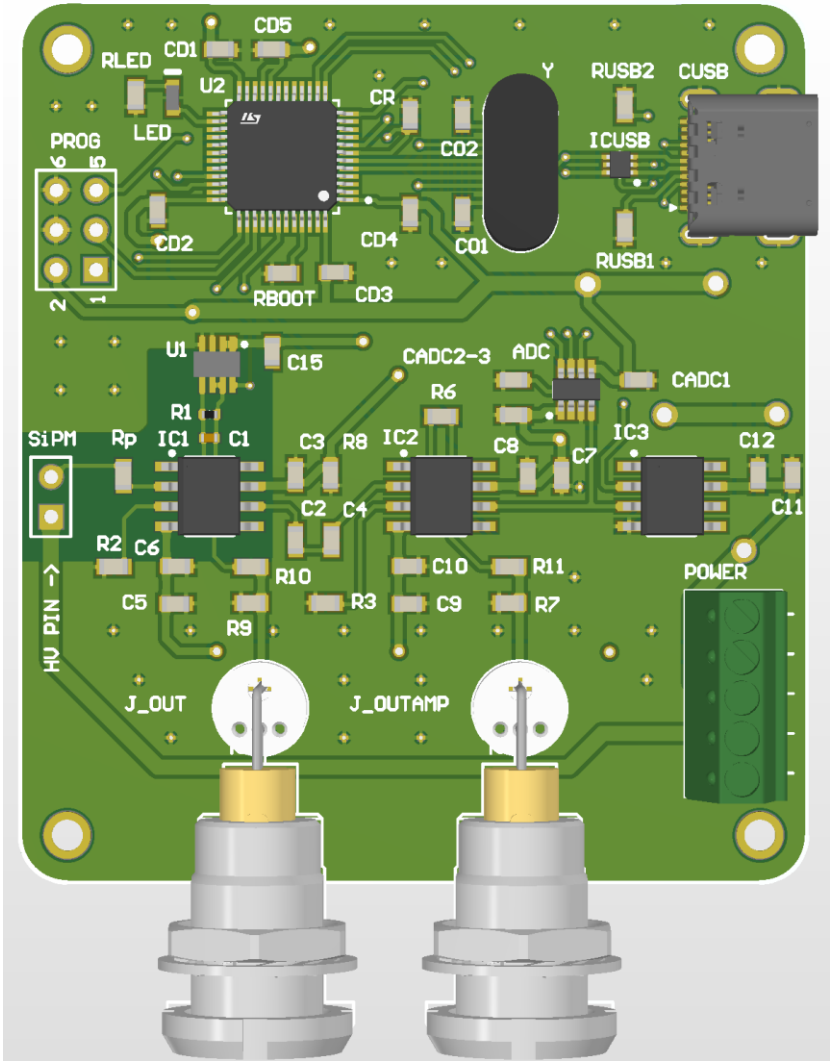


Reset SPICE Simulation

Comparator operates as expected. Reset shows ≈100 ns delay and ≈−20 mV residual offset due to charge injection.

PCB Design

- Implement the analog front-end circuitry (CSA + inverting amp + comparator + reset) and digital control
- Minimize **parasitic capacitance (p.c.)** at the CSA input

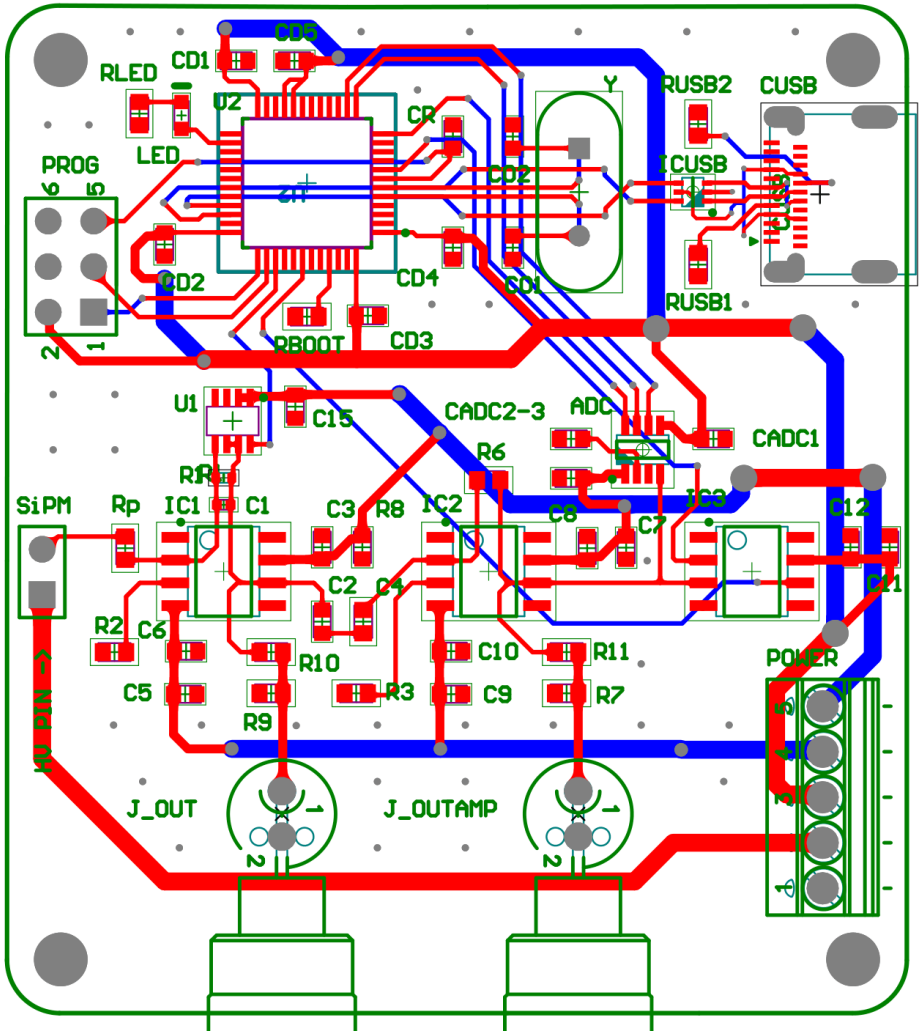


PCB Design

Several factors can impact the parasitic capacitance

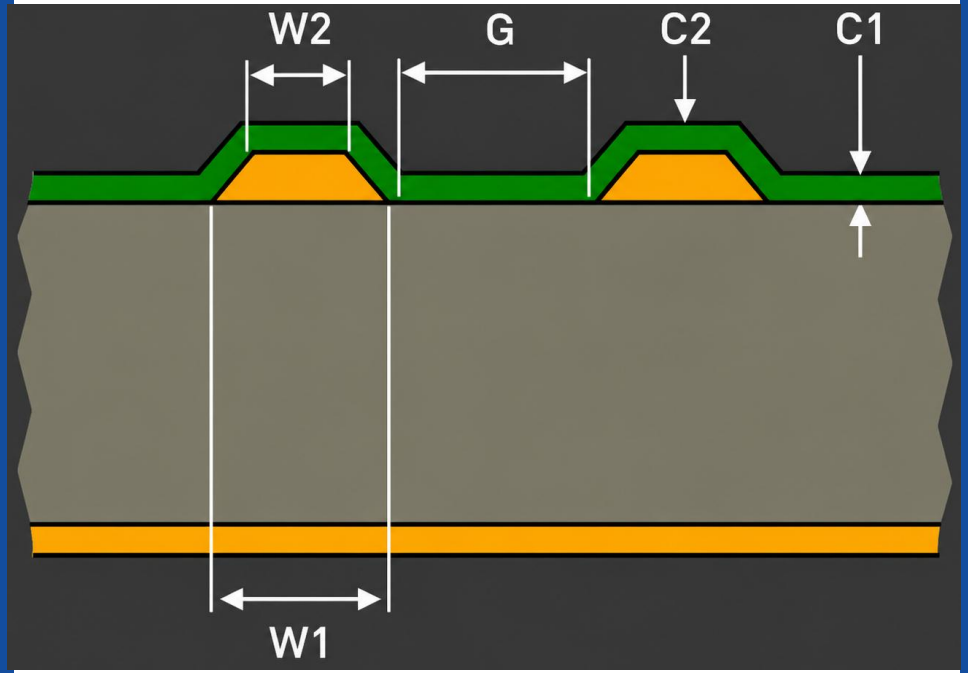
Rf and Cf packages can add p.c. (0603 adds 0,040pF while 0402 adds 0,026pF)

Components, copper traces and planes will also add p.c.



Minimizing C.P.

Proximity of the CSA inverting node to copper tracks and planes will add a high amount of parasitic capacitance

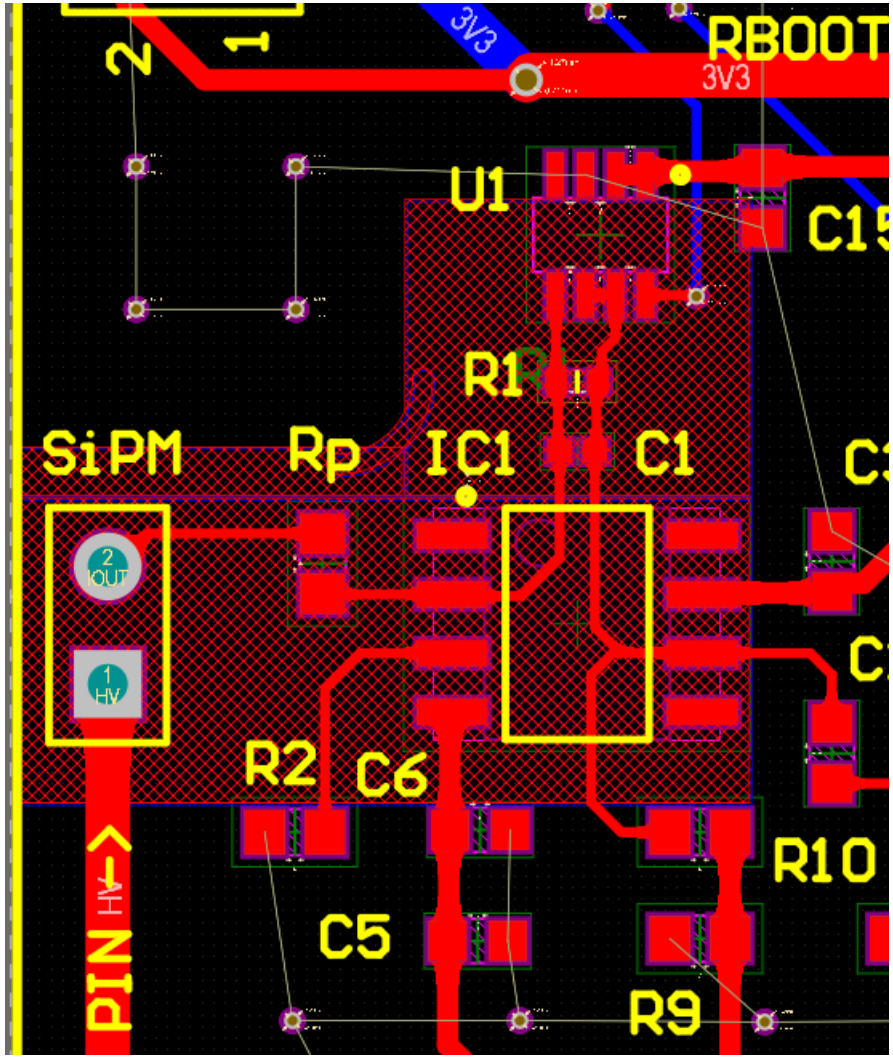


Minimizing C.P.

Removing the GND plane around the CSA minimizes the parasitic capacitance

W/ GND Plane: C.p. = 1,3pF
W/o GND Plane: C.p. = 85,3 fF

Reduced C.P. by a factor of 15!



Summary and Next Steps

- Single-photoelectron-scale readout
- Complete analogue + control architecture
- SPICE results agree with theoretical design
- PCB optimised for parasitic capacitance
- PCB fabrication and assembly for future in-lab testing and characterization with a real SiPM