Nanoelectronic chip design:
from physics principles to circuit design for production

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Projecto Integrador de 2º Ciclo

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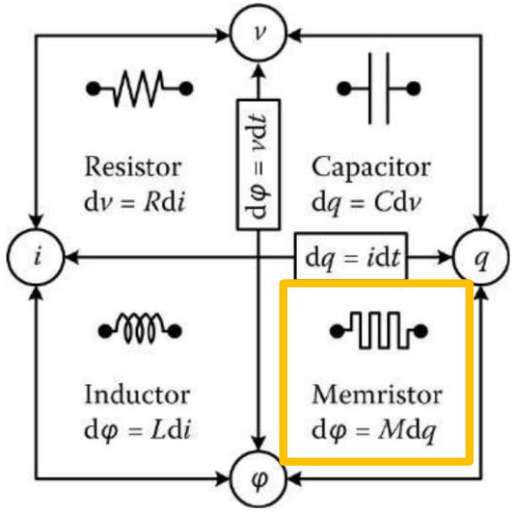
Motivation: Neuromorphic hardware is a solution for the von Neumann bottleneck

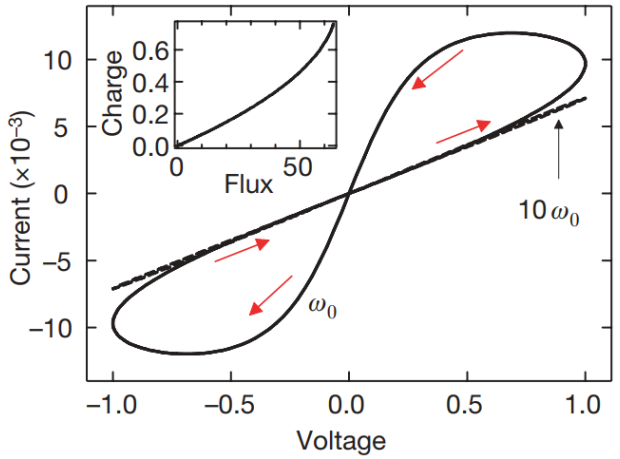
Thesis goal: Design and fabricate a simple neuromorphic chip with memristors

PIC2: Study, fabricate and simulate memristors

What is a memristor?

- Resistor with **memory**
- **4th** fundamental circuit element
- I-V curve: **pinched hysteresis**

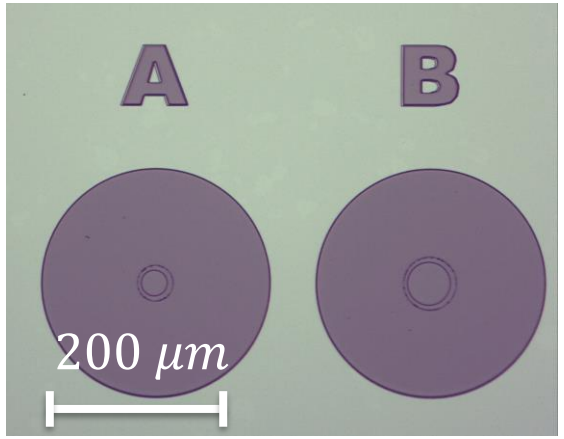




Fabrication

- **Si/Ag**-based memristors
- Electrochemical Metallization Mechanism (**ECM**)
- 9 samples were fabricated

Samples during the fabrication process



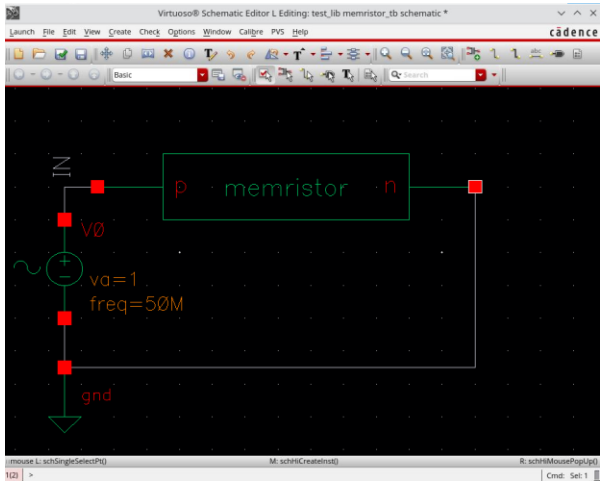
Final devices on the microscope

Simulation

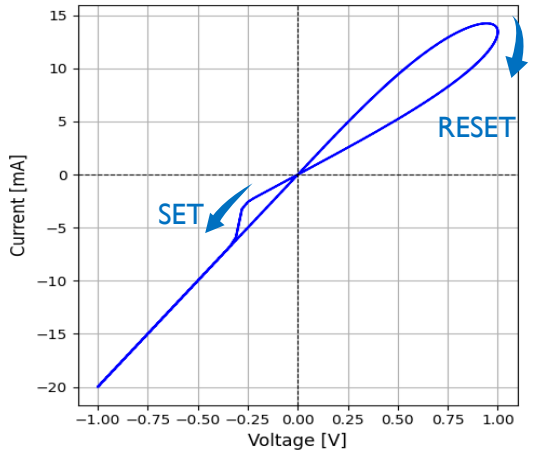
Software: **Cadence** (industry-standard for circuit design)

Language: **Verilog-A** (hardware description language)

Model: **VTEAM** (Voltage Threshold Adaptative Model)



Cadence environment

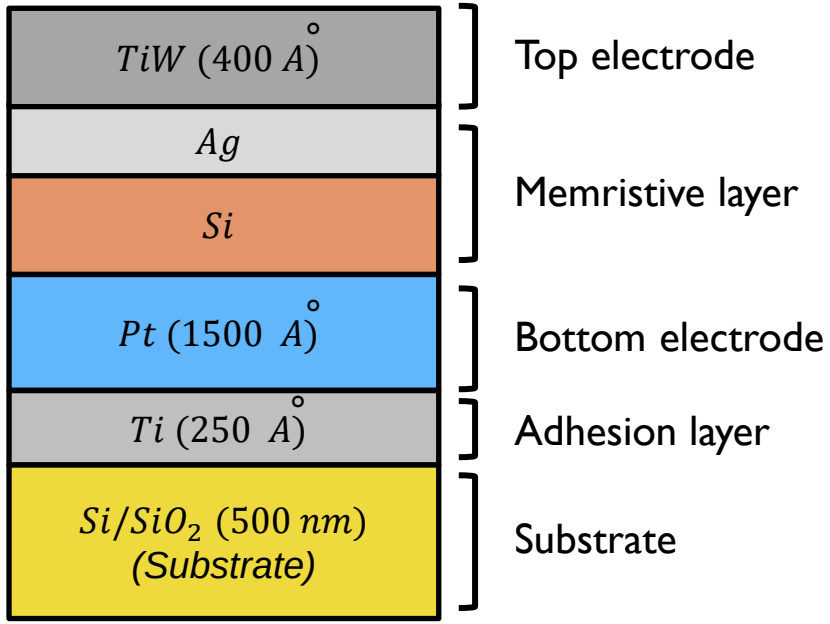


I-V curve simulation

Thank you for your attention!

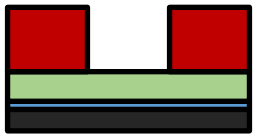
Full stack:

Si/SiO2 / Ti (250 Å) / Pt (1500 Å) / Si/Ag / TiW (400 Å)

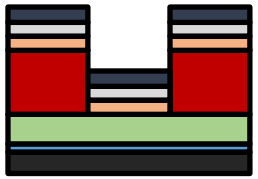


Sample #	Si (Å)	Ag (Å)
1	200	20
2		30
3		50
4		80
5		100
6	100	20
7		30
8		50
9		80

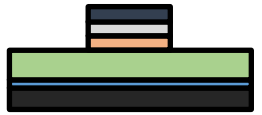
1. Deposition of Ti and Pt (N8800)



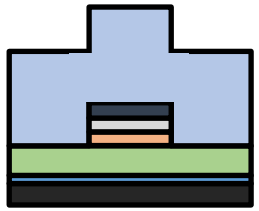
2. 1st Lithography



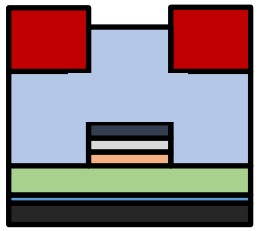
3. Deposition of Si/Ag (Alcatel) and TiW (N7000)



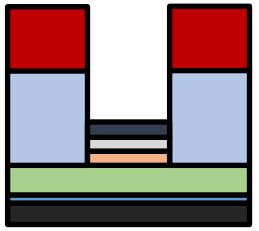
4. Lift-off



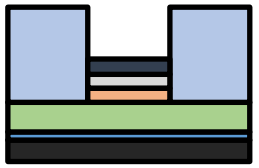
5. Passivation (Oxford PECVD)



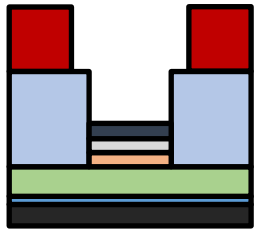
6. 2nd Lithography



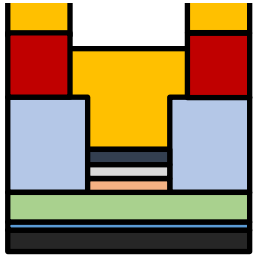
7. Reactive Ion Etching



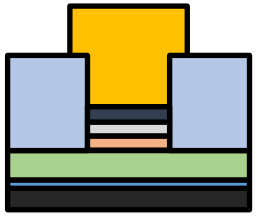
8. Resist Strip



9. 3rd Lithography



10. Top Metalization (N700)



11. Lift-off

AlSiCu (600 nm)
SiO_2 (300 nm)
TiW (40 nm)
Al
Si
Pt (150 nm)
Ti (25 nm)