ATLAS Upgrade

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on behalf of the ATLAS-LIP group

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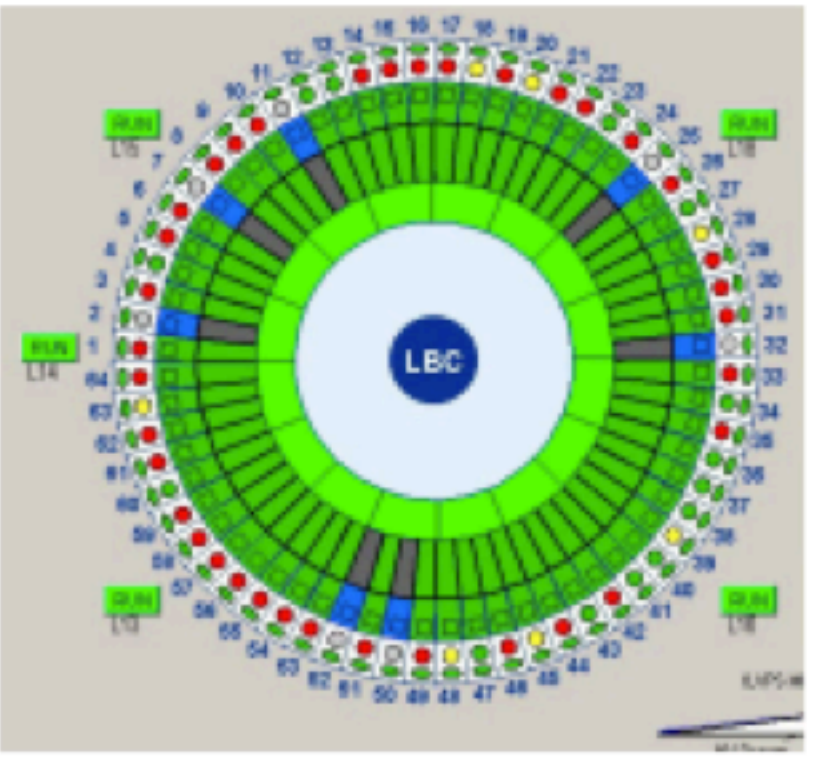
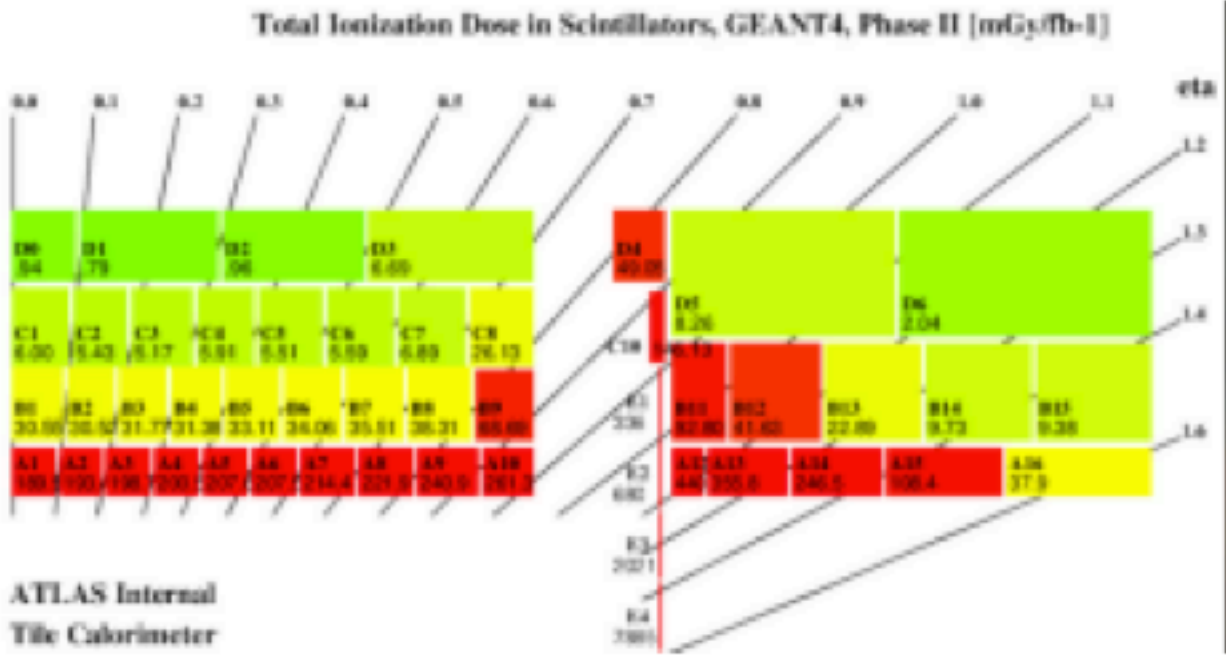
ATLAS-LIP current operations overview

TileCal

Leading DCS and Calibration



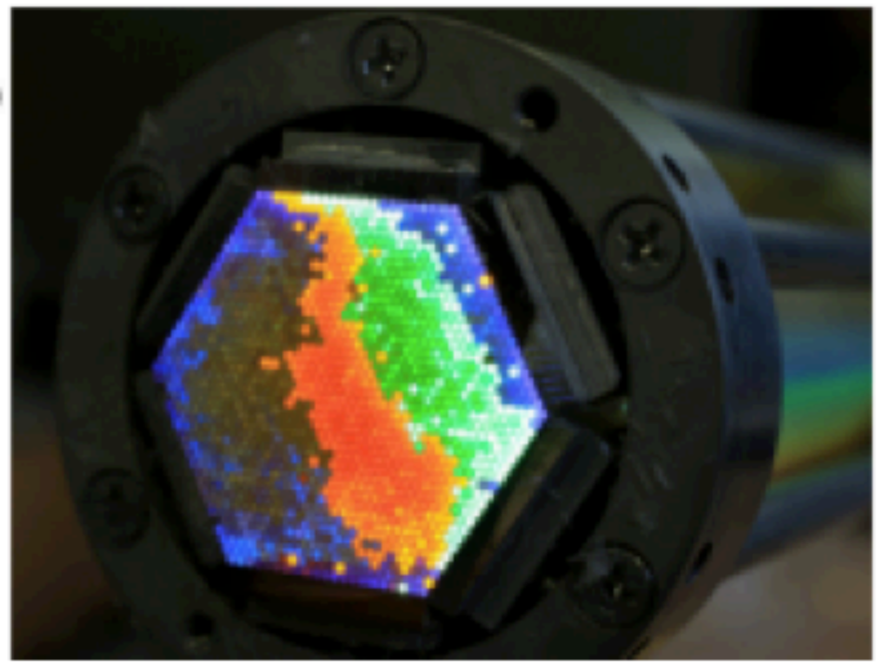


Distributed computing

Iberian cloud coordination

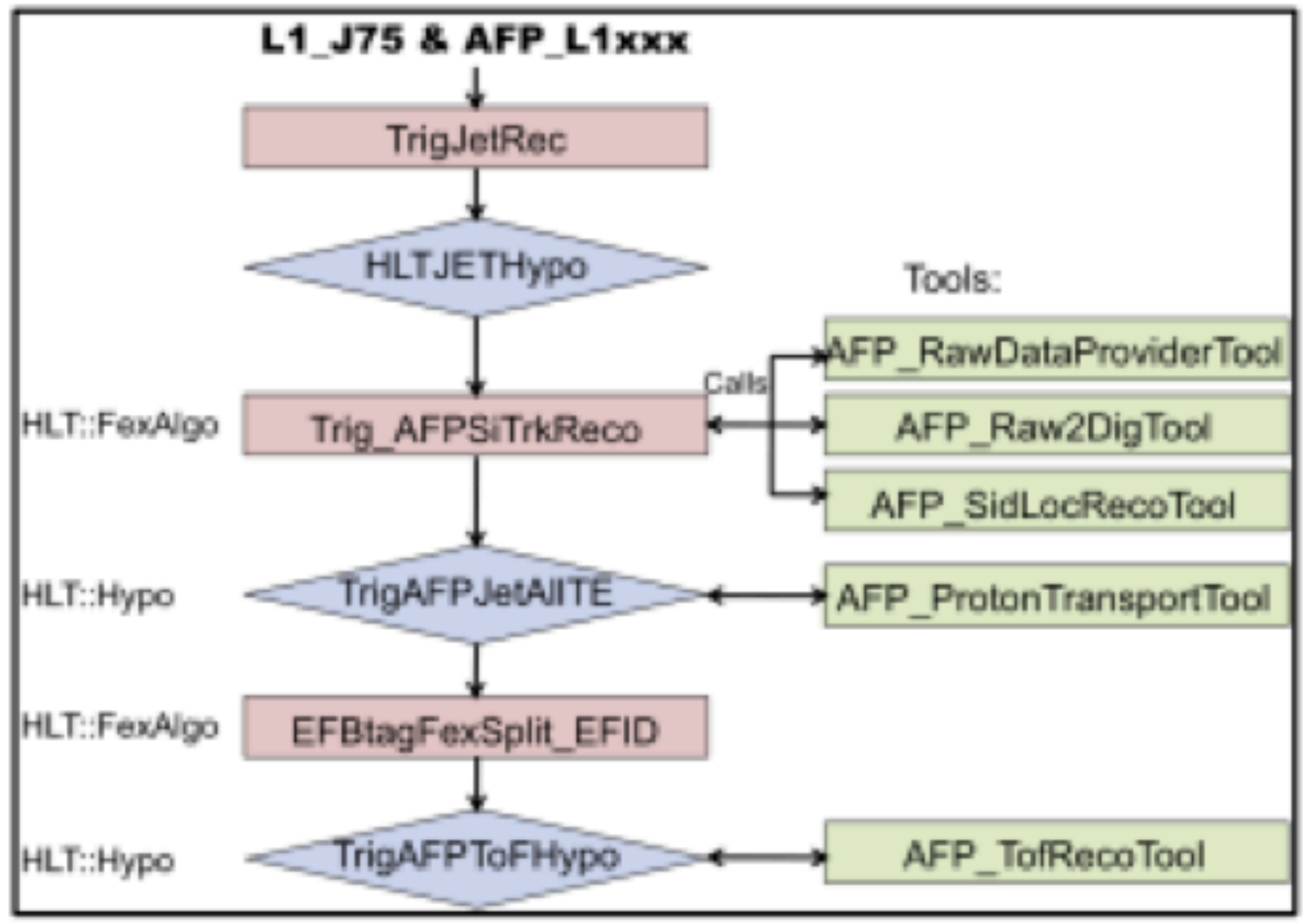
Monitoring tools

Tier-2 infrastructure responsibility



Jets HLT

Operations, validation



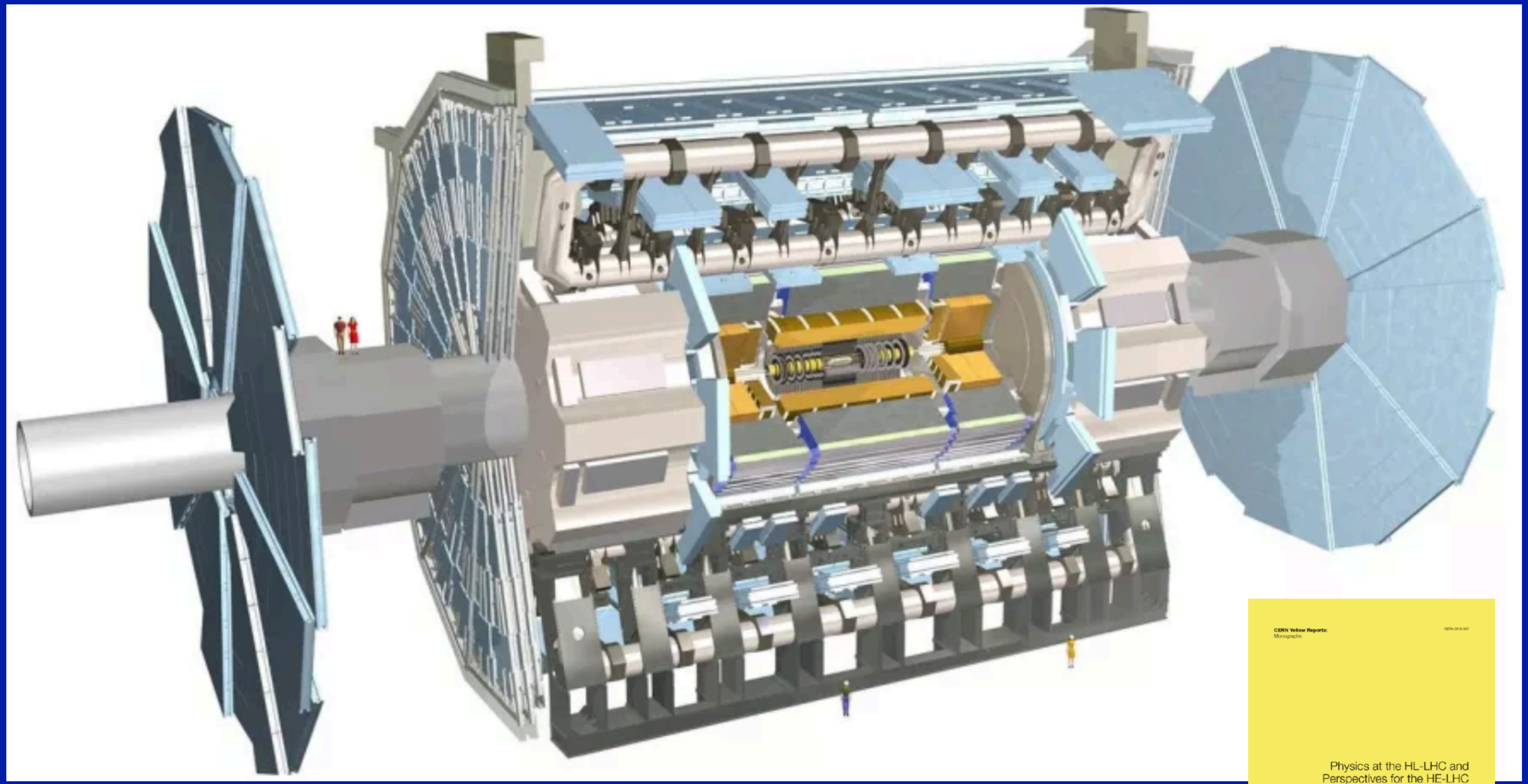
ATLAS Roman Pot Detectors

Co-leading DCS

HLT algorithms

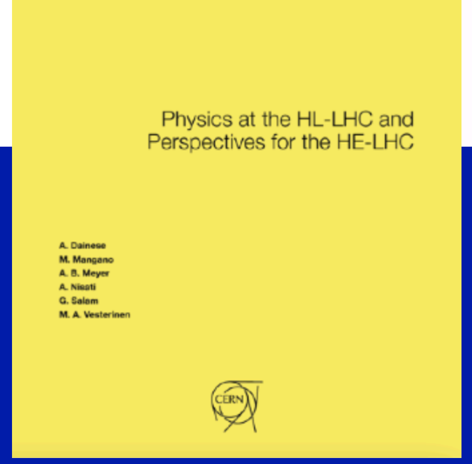
ATLAS Phase-2 upgrade

Trigger and Data Acquisition:
- First level tigger at 1 MHz, 5.2 TB/s, 10 μs latency
- Event Filter 10 kHz, ~52 GB/s



Electronics upgrade:
- On/Off-detector electronics for Calorimeters and Muon systems
- 40 MHz readout and finer trigger segmentation.

High Granularity Timing Detector:
- 30 ps precision timing using Silicon Low Gain Avalanche Detectors (LGAD)
- Improves pileup separation and luminosity measurement

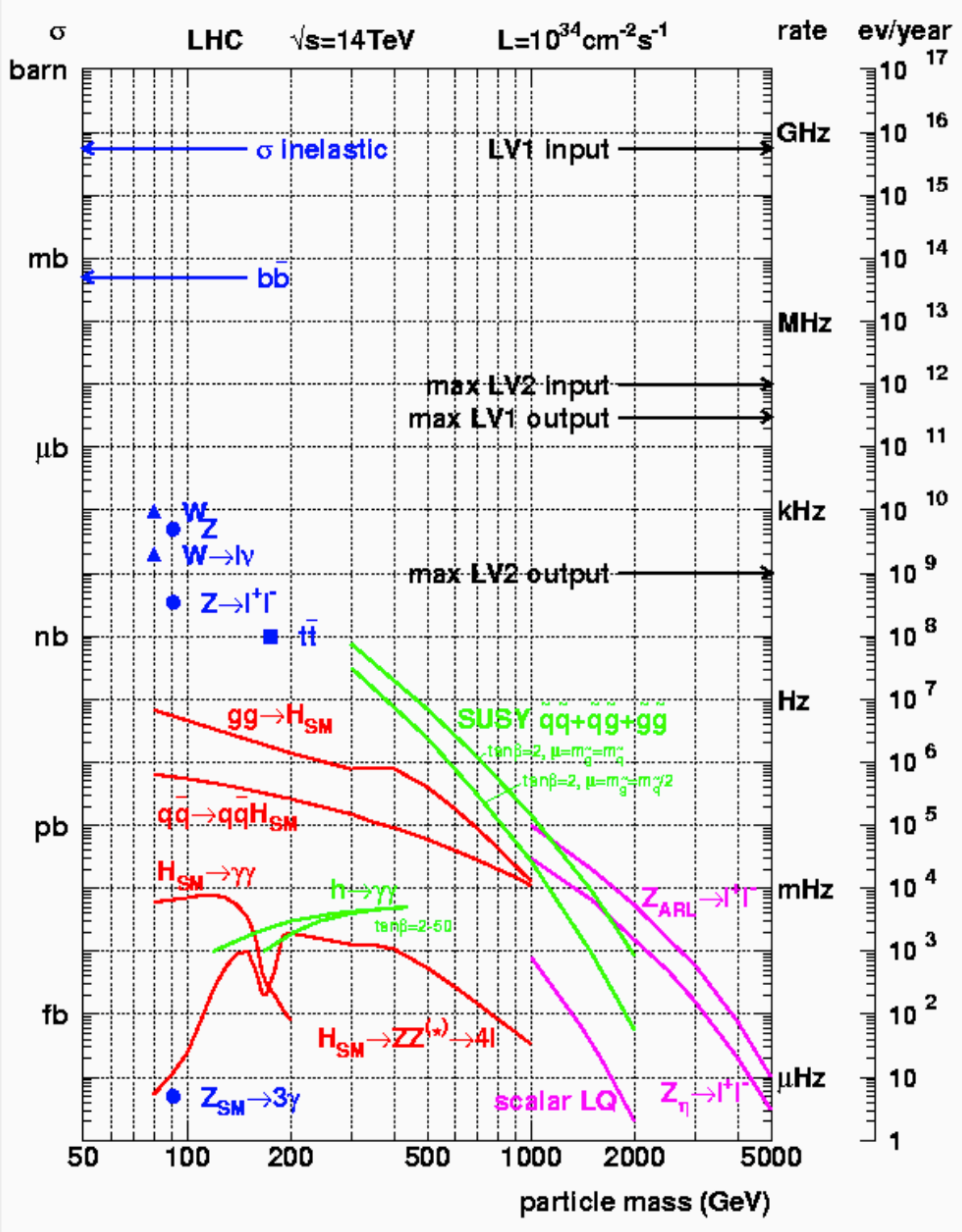


New Inner Tracker Detector:
- All Silicon.
- 9 layers for $|\eta|<4$.
- Reduced material budget. - Finer segmentation.

New muons chambers:
- Inner barrel with new RPCs, sMDTs and TGCs.
- Improves momentum resolution, trigger efficiency and fake rejection.

Additional upgrades:
- Luminosity detectors (1% precision),
- Zero degree calorimeter for Heavy Ion physics.

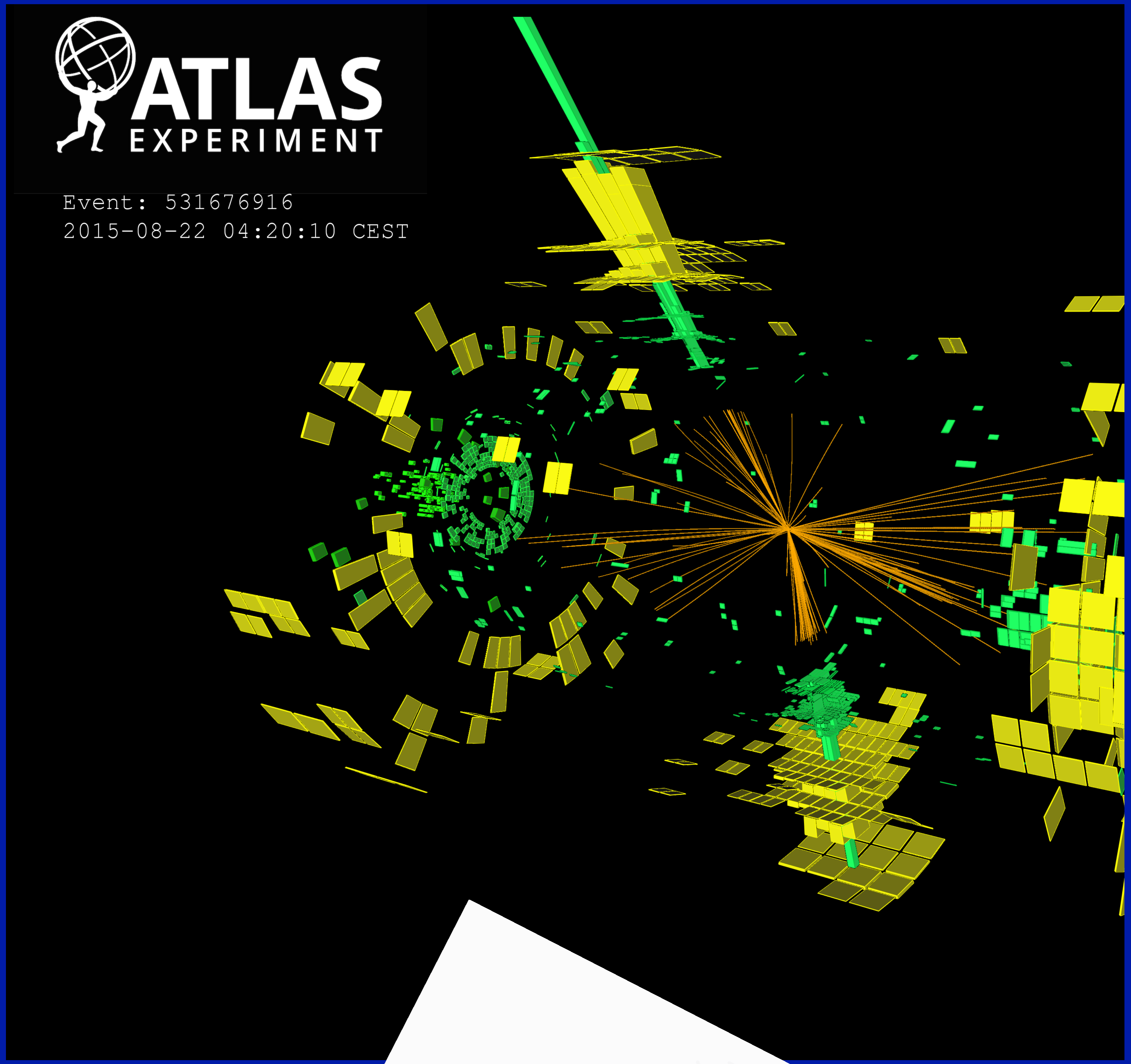
LHC upgrade challenges



- Many interesting processes have small cross-sections
- Large increase of pileup
- The trigger system has to process & select events in real time

	Run 2	Run 3	Run 4
Energy (√s)	13TeV	13.6 TeV	14 TeV
Max. Luminosity ($cm^{-2}s^{-1}$)	$1\text{-}2\times10^{34}$	$2\text{-}3\times10^{34}$	$5\text{-}7\times10^{34}$
Interactions/event	40	55-80	140-200
Bunch crossing rate	40 MHz	40 MHz	40 MHz
Offline storage rate	1 kHz	1.5 kHz	10 kHz
Bunch spacing	25 ns	25 ns	25 ns

GPUs for accelerating trigger algorithms



HLT farm size is limited by power and cooling

and

CPU time increases with pileup

- Tracking algorithms dominate, but calorimeter clustering important too

GPGPUs: provide massive parallelisation potential

- Thousands of cores per processor

  New paradigm: single instruction-multiple data

- Require handling internal memory of the GPU correctly

Developing calorimeter clustering on GPUs

HLT calorimeter reconstruction

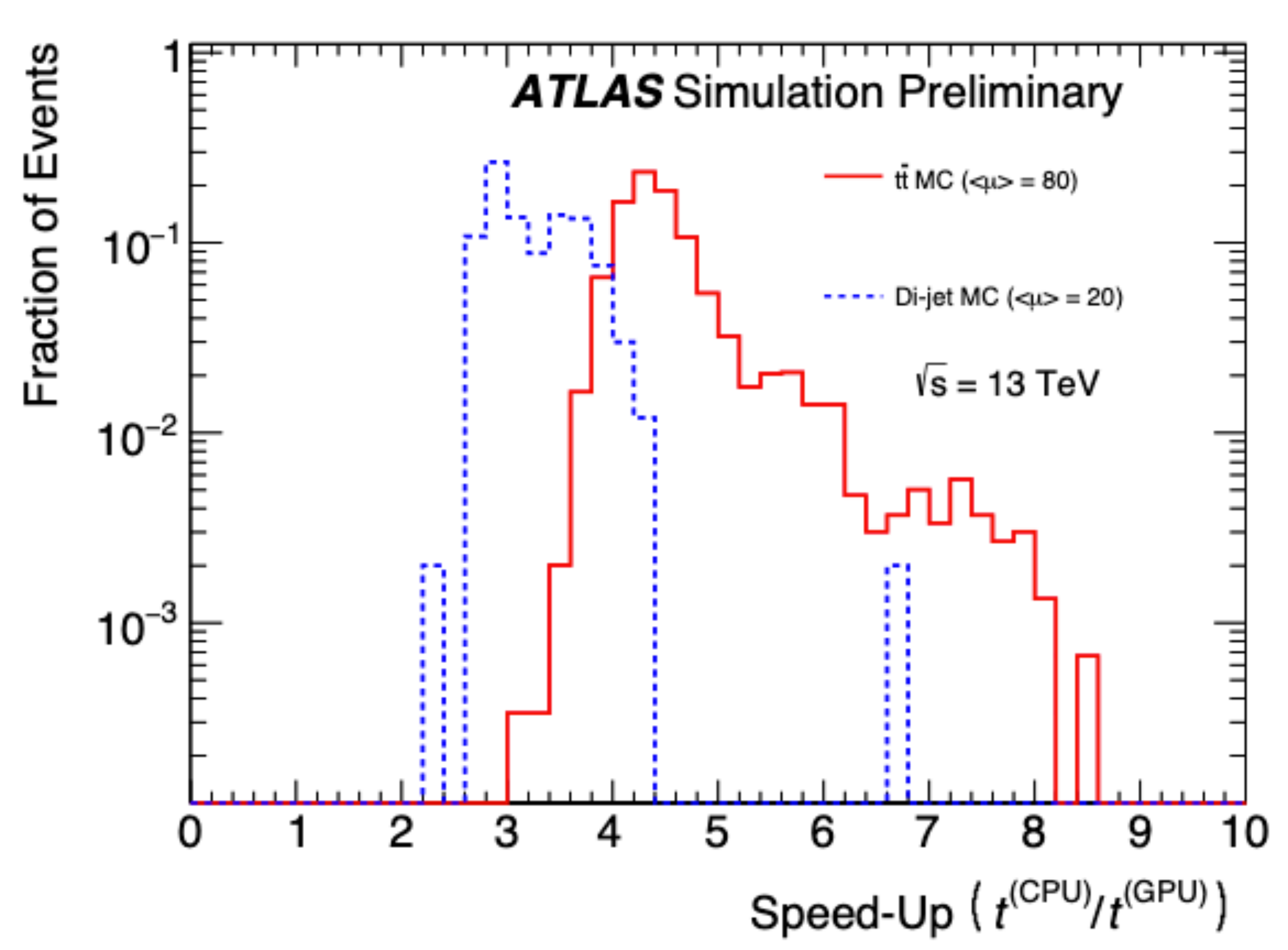
Test results

- Calorimeter clusters compared one by one when reconstructed with CPU and GPU

- Timing measurements obtained by running on the full sample and subtracting the cell making and Athena execution times. GPU times include cluster growing, cluster splitting, data conversions and data transfers from CPU to GPU and back

- Very preliminary speed-up factors: 3.5 for di-jet events (⟨μ⟩=20) and 5.5 for ttbar events (⟨μ⟩=80)

- Fraction of time dedicated to the algorithms (CPU-TopoClustering vs GPU-Topo-Automaton Clustering - see backup) is <20%. Remaining time being taken in data conversions and data transfers



A Common Tracking Software (ACTS)

Tracking of charged particles is the most complex and CPU consuming phases of event reconstruction
Will become even greater during HL-LHC

ACTS

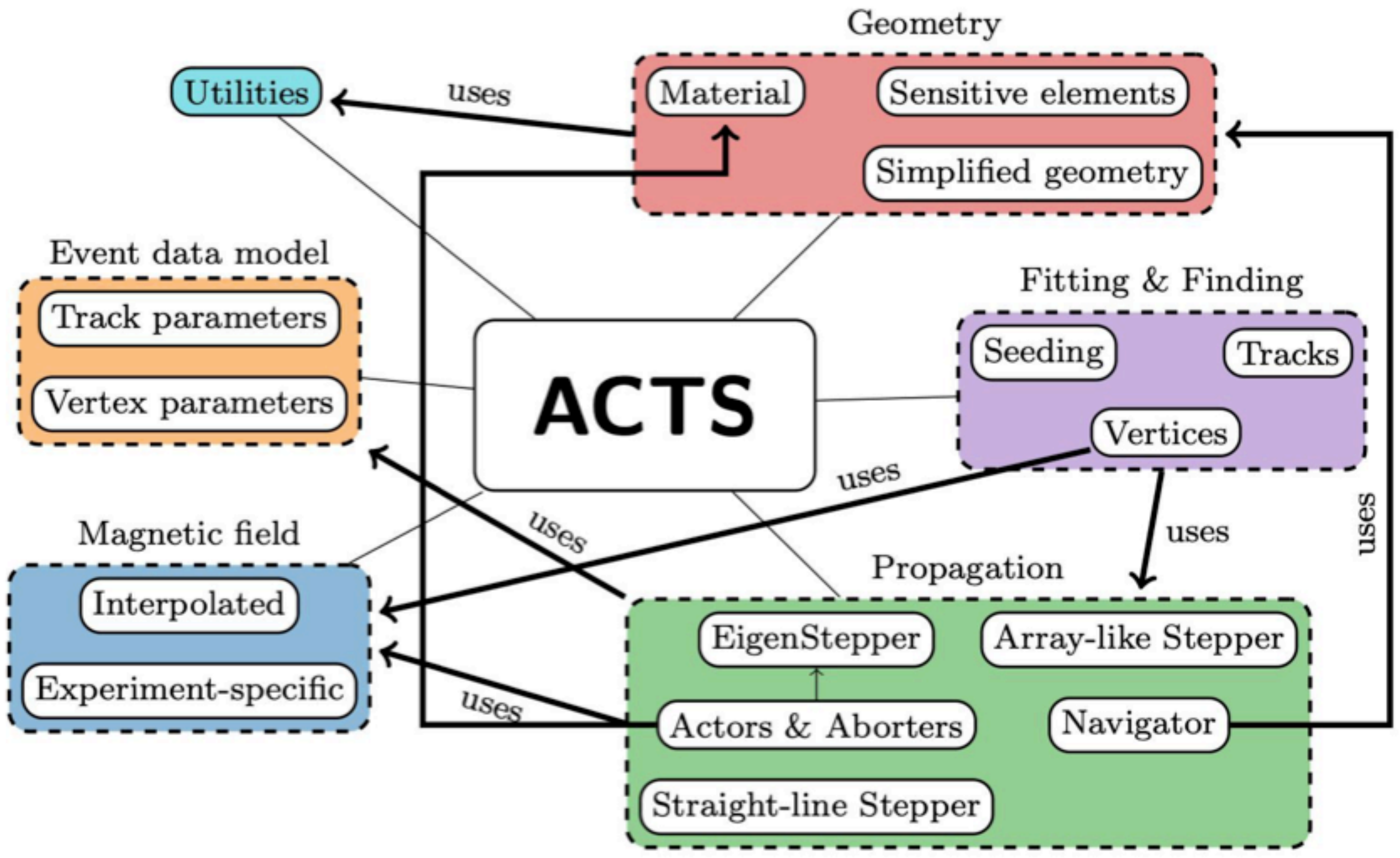
- Experiment-independent toolkit for track reconstruction
- Designed for modern computing architectures and multi-threaded event processing

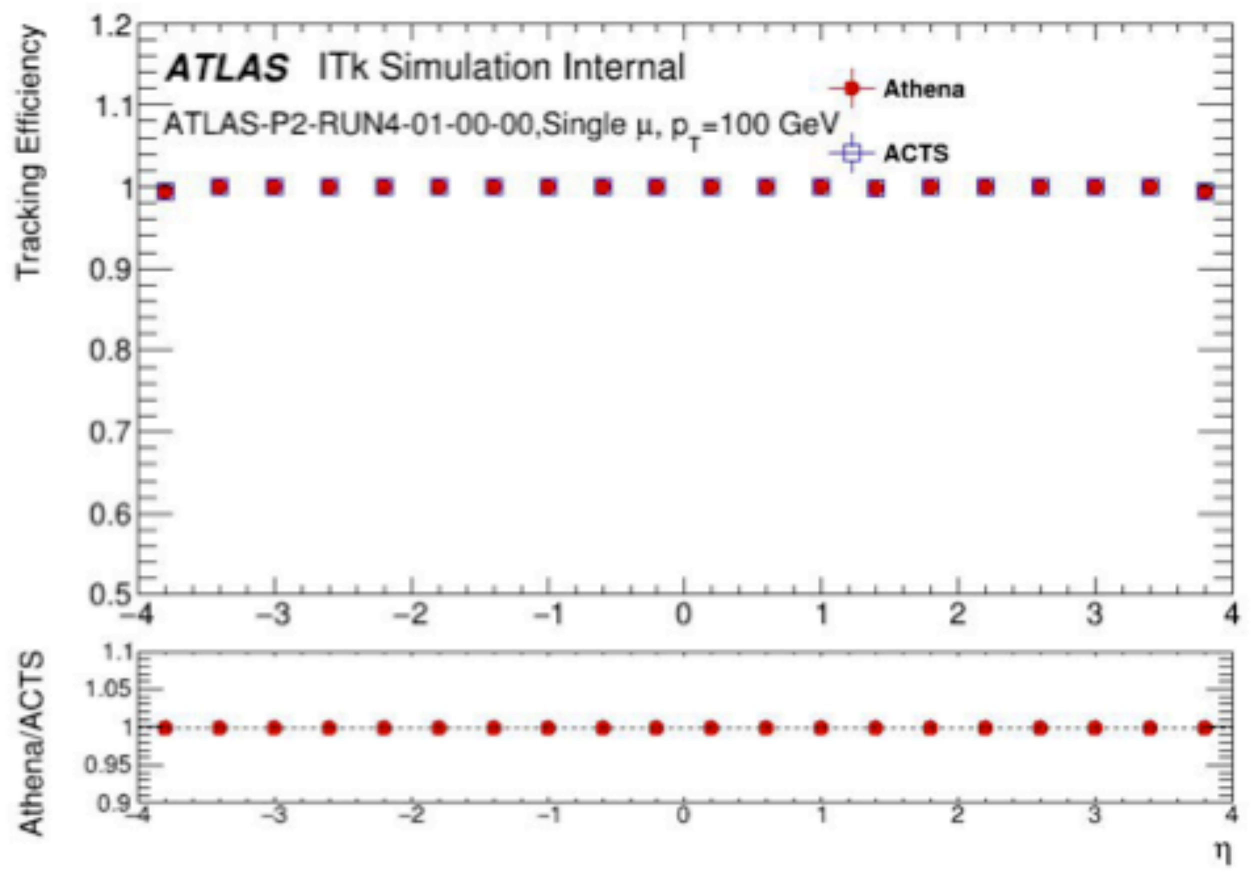
Goal

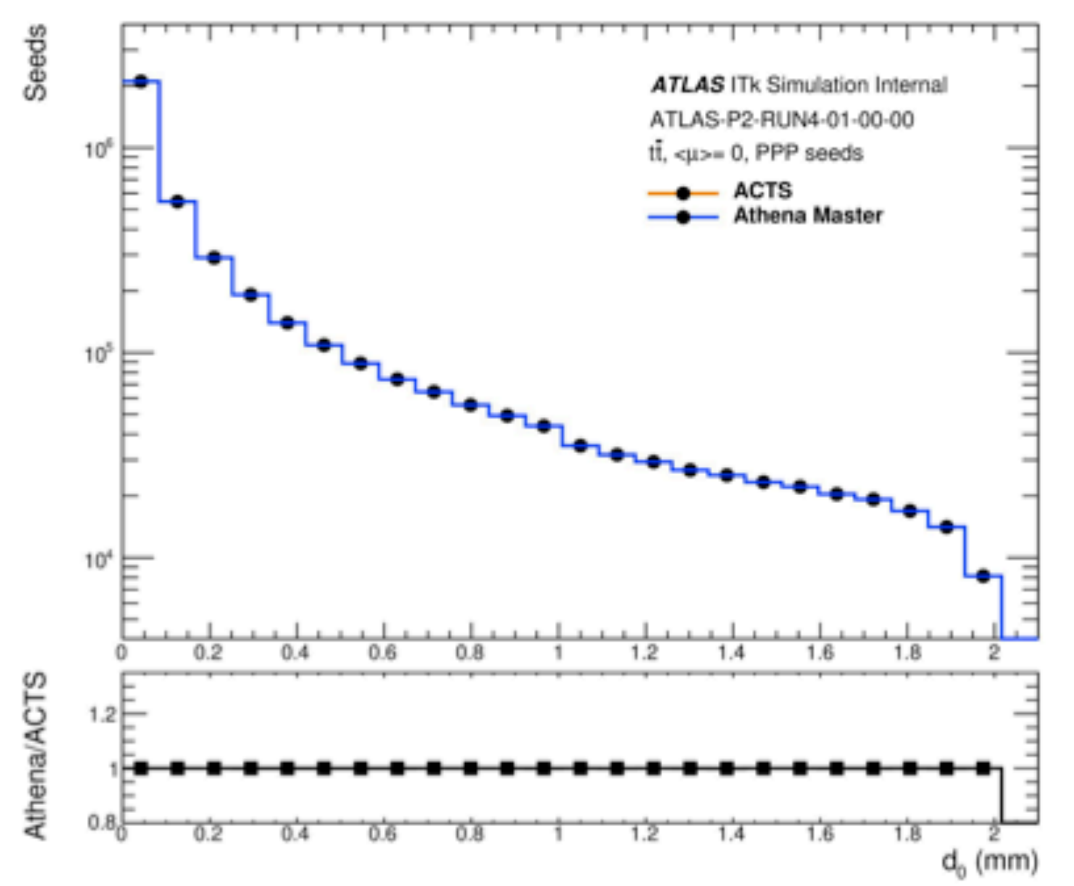
- Implement ITk Seeding Algorithm in ACTS, integrate into standard ATLAS code and validate its performance

The Seeding Algorithm

- Forms track seeds consisting of triplets of space-points (SP) based on geometrical assumptions relative to the interaction point



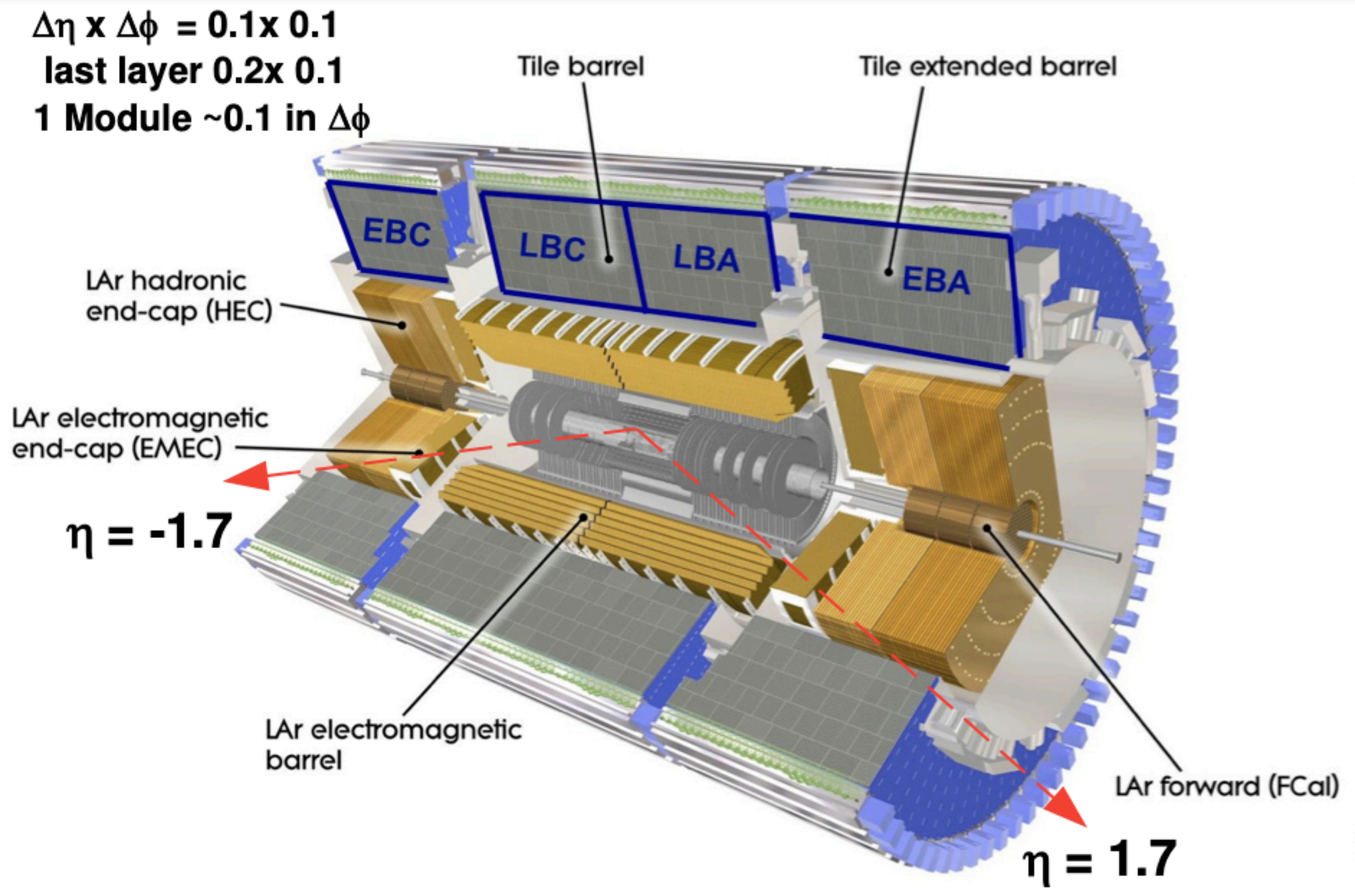


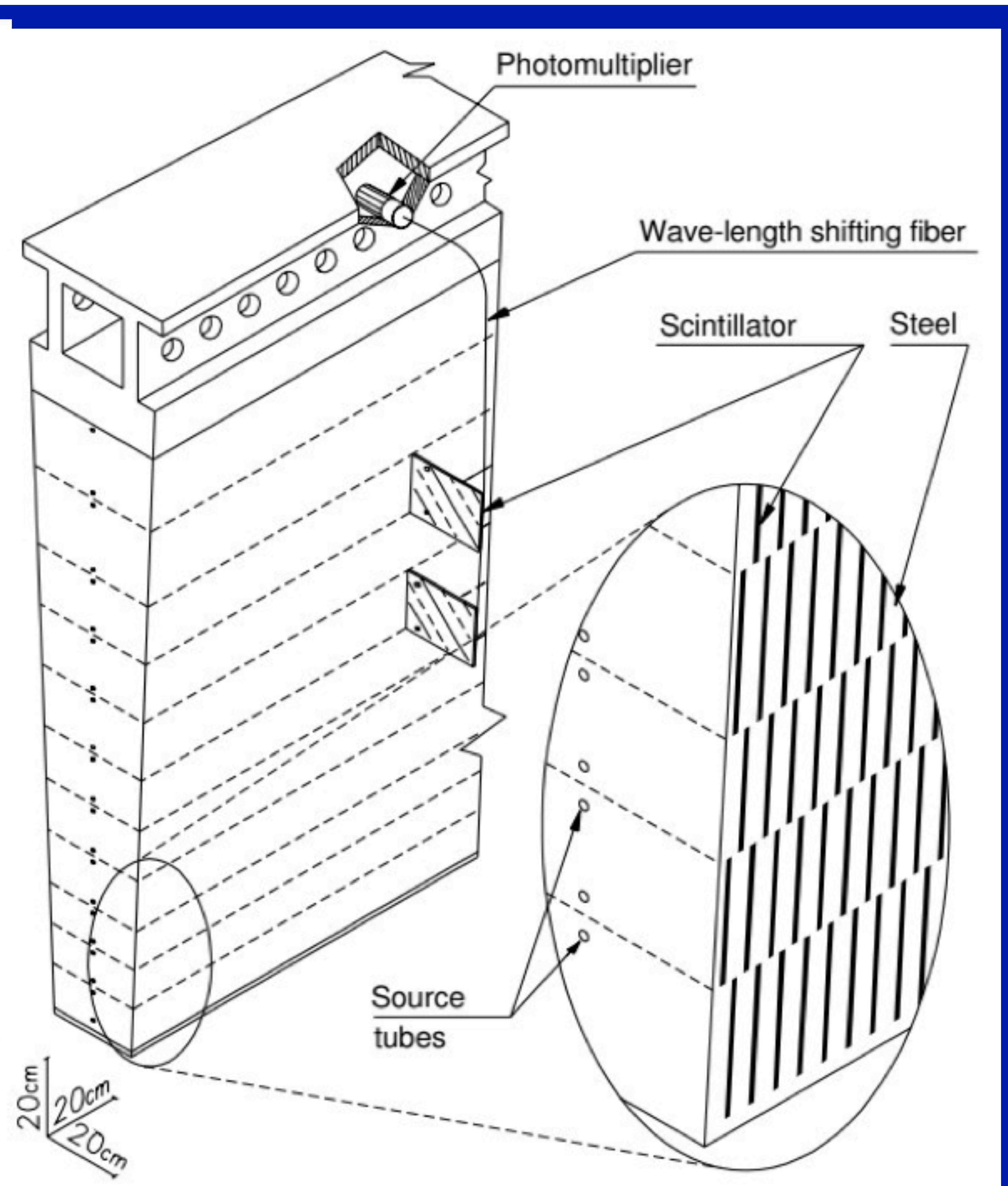


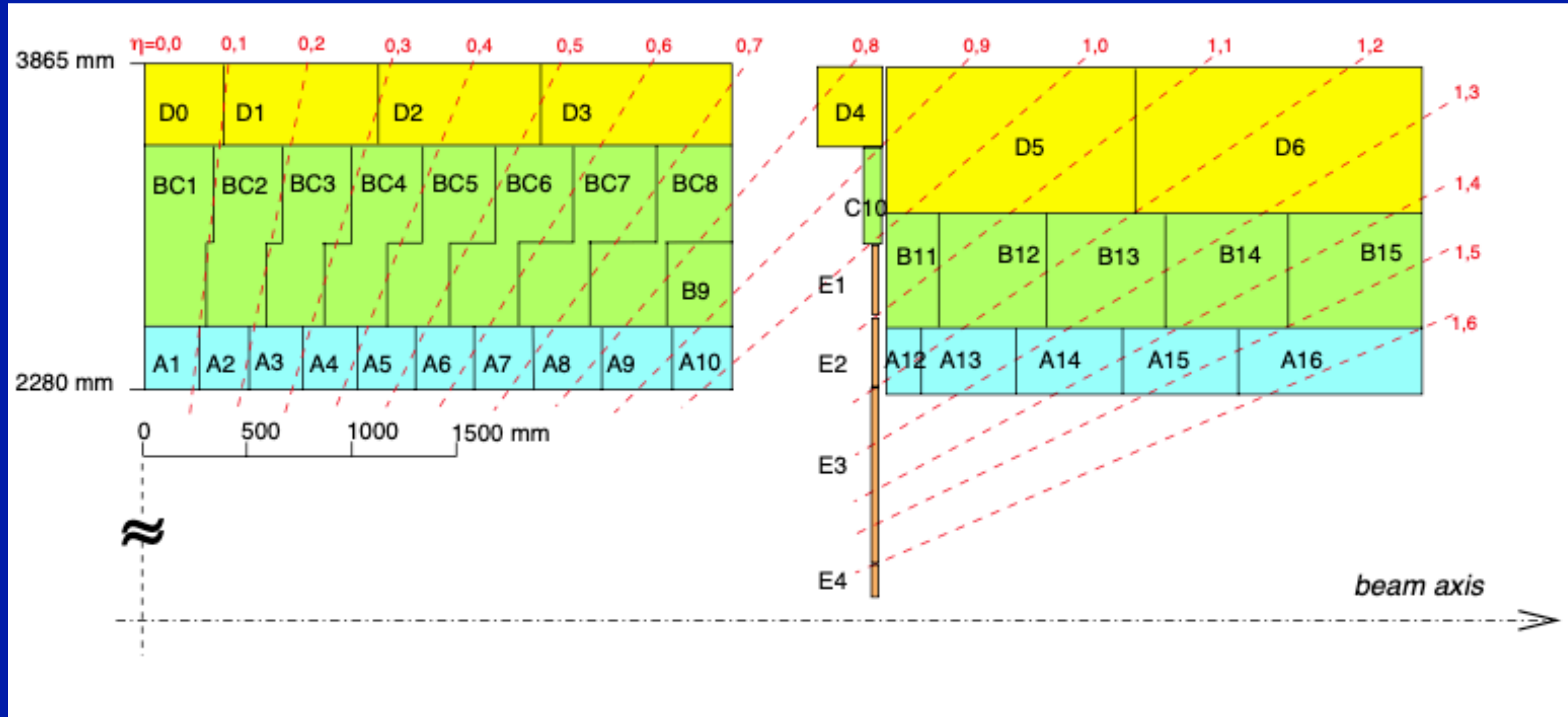
ATLAS TileCal

One long barrel (|η| < 1.0) and 2 extended barrels 0.8 < |η| < 1.7, each composed of 64 modules in φ (256 modules in total).

Steel plates and plastic scintillators (the tiles) coupled to wavelength shifting fibres.







Tilecal pseudo projective cell layout

About 5000 pseudo-projective cells.
each cell readout by 2 PMTs (~10000 PMTs in total)

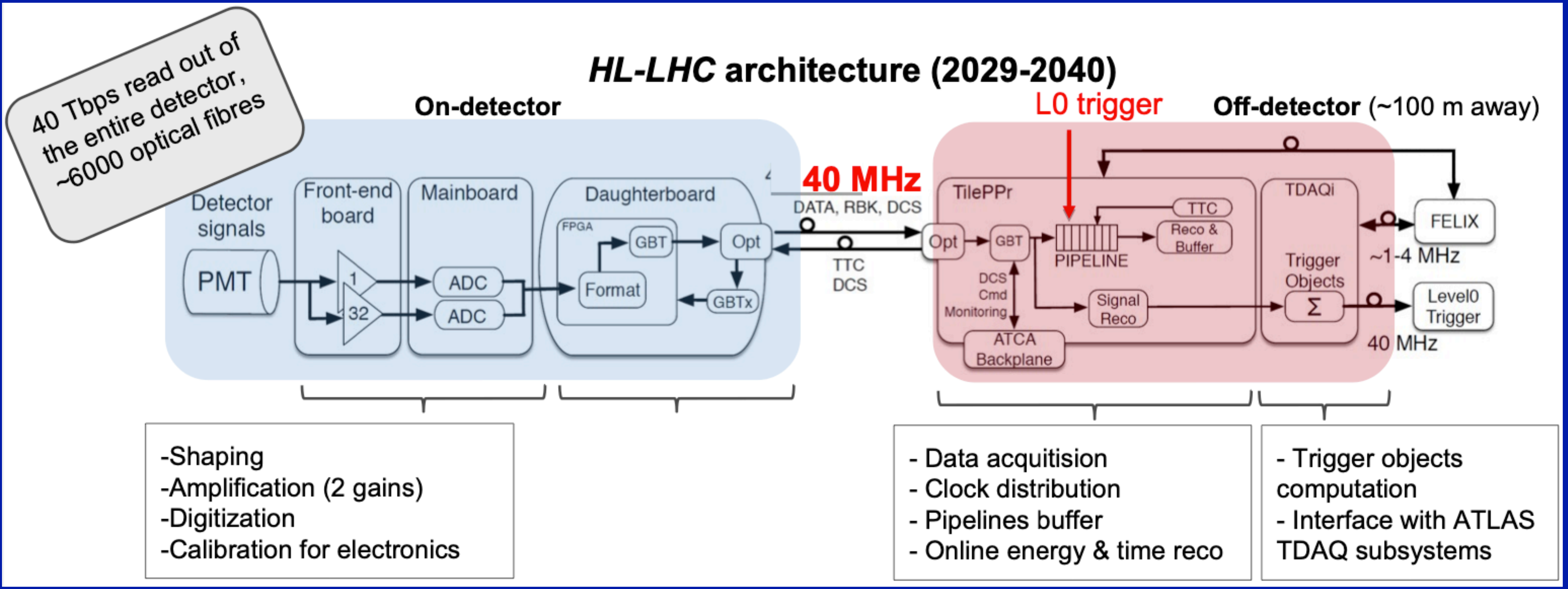
Dynamic range 10 MeV to 2 TeV per cell.

$$\frac{\sigma_E}{E} = \frac{50\,\%}{\sqrt{E[\mathrm{GeV}]}} \oplus 3\,\%$$

TileCal's upgrade

Motivated by

- Lifetime extension (HL-LHC 2029-2040).
- Higher radiation environment (lumi x5-7 compared to nominal LHC)
- New trigger requirements



Upgrade

- Active dividers on the PMTs
- Complete replacement of on- and off-detector electronics
- 40 MHz readout to off-detector electronics. 40 Tb/s over 6000 optical fibres
- Improve reliability (full readout redundancy, new HV and LV systems) and maintainability (new mechanics)

TileCal High-Voltage System

System parameters:

10000 PMTs

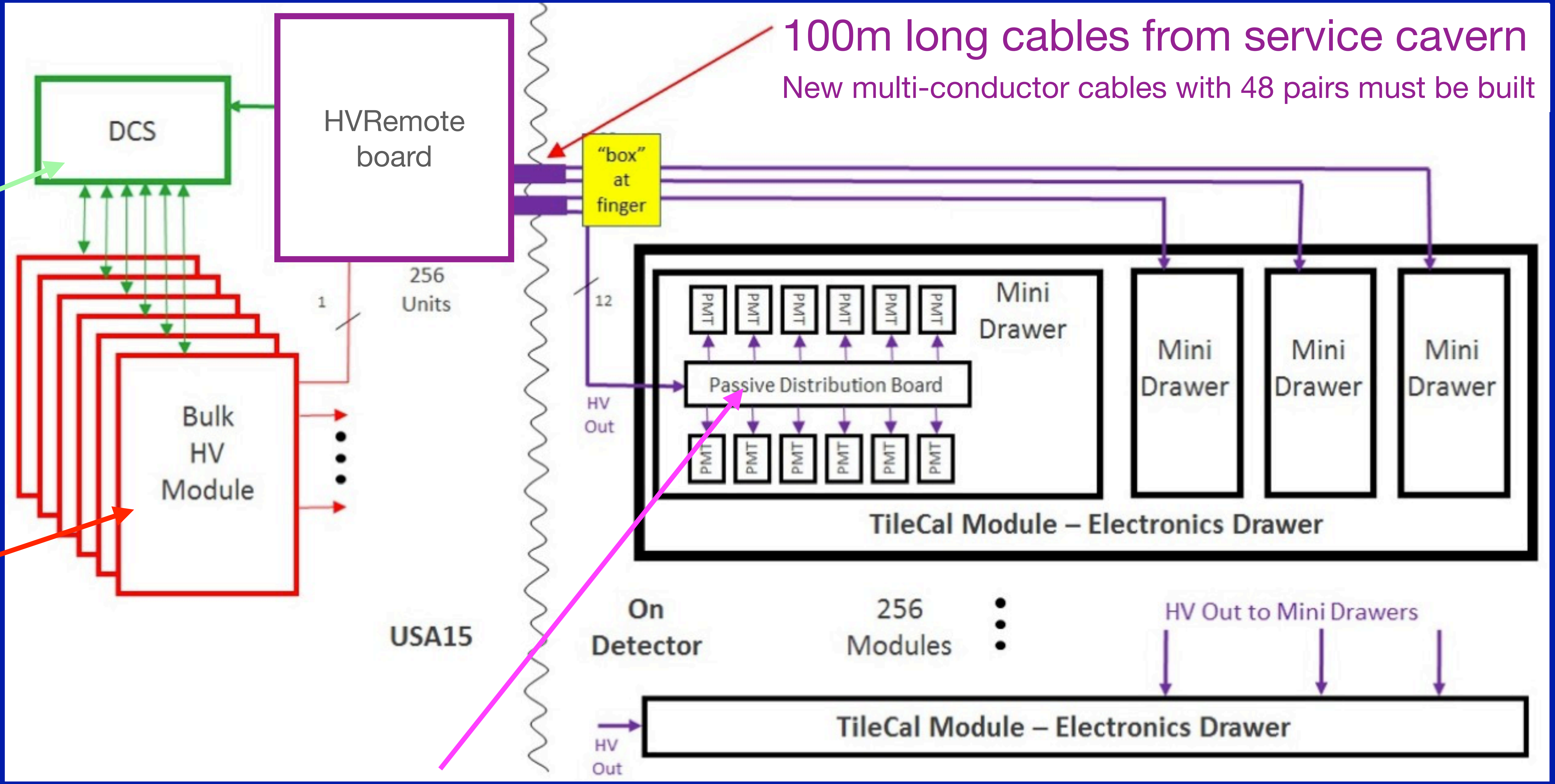
High Voltage < 950 V; Individual currents < 400 μA

High Voltage stability < 0.5 V rms

LIP responsability

DCS system: SoC board for High Voltage control and monitoring

HVRemote boards: Regulation and control of the 48 PMTs in each module off detector at USA15 (256 boards)



HVBus: passive distribution board distributes HV to PMTs (1024 boards)

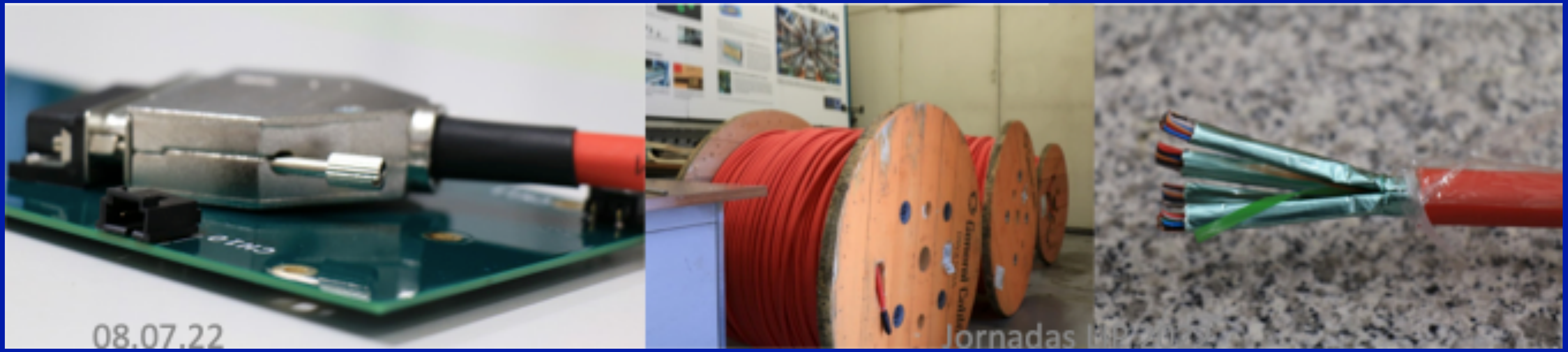
High-Voltage distribution

Cables

- New 48 wire pairs cable 100 m long developed in Portugal with …
  10000 PMTs => 20000 wires
  - Wire diameter: 0.4mm
  - Aluminium/PETP tape screen and drain wire ensures electromagnetic shielding
  - Prototypes produced

HVBus

- HV bus and short cables for HV distribution produced and tested



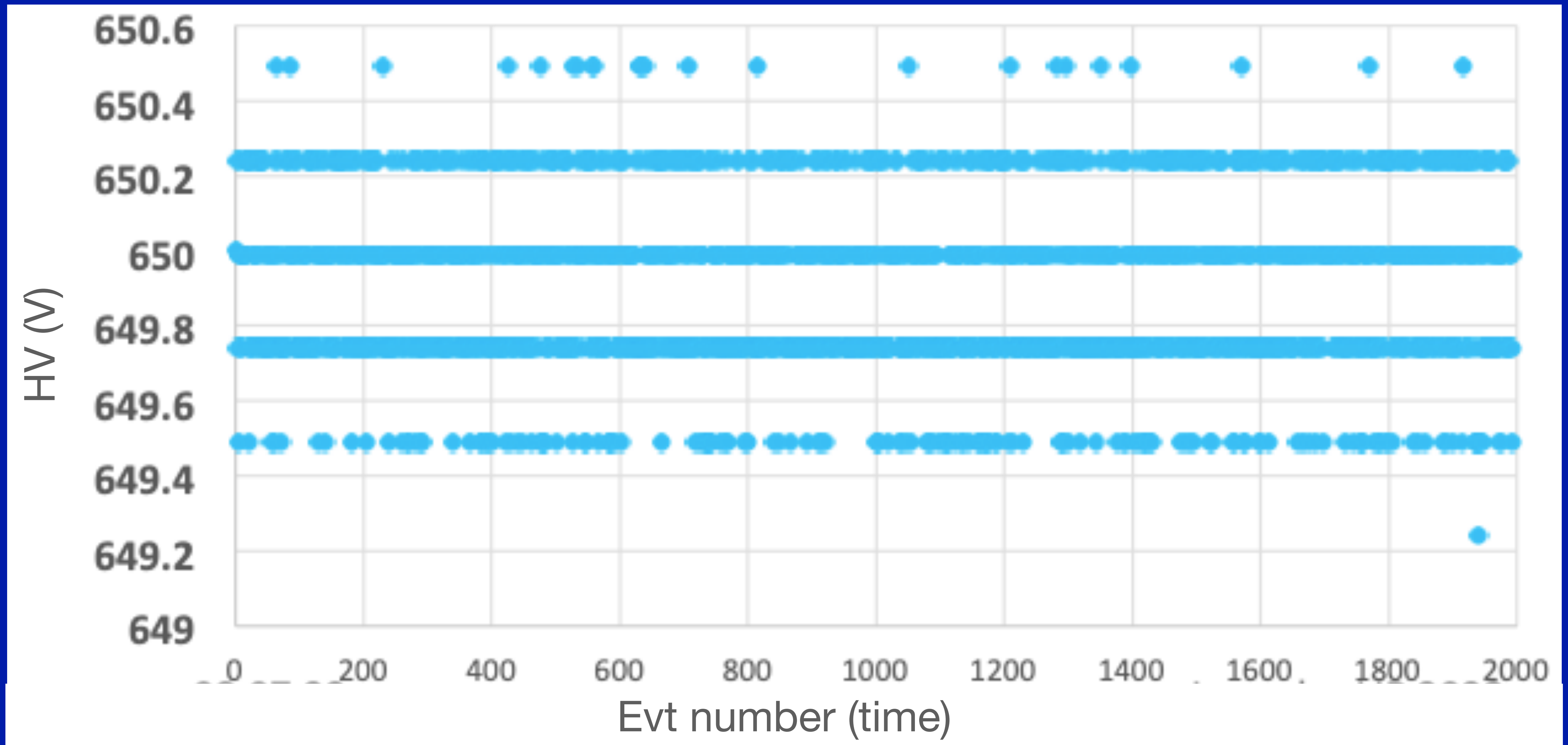
Testing Programme

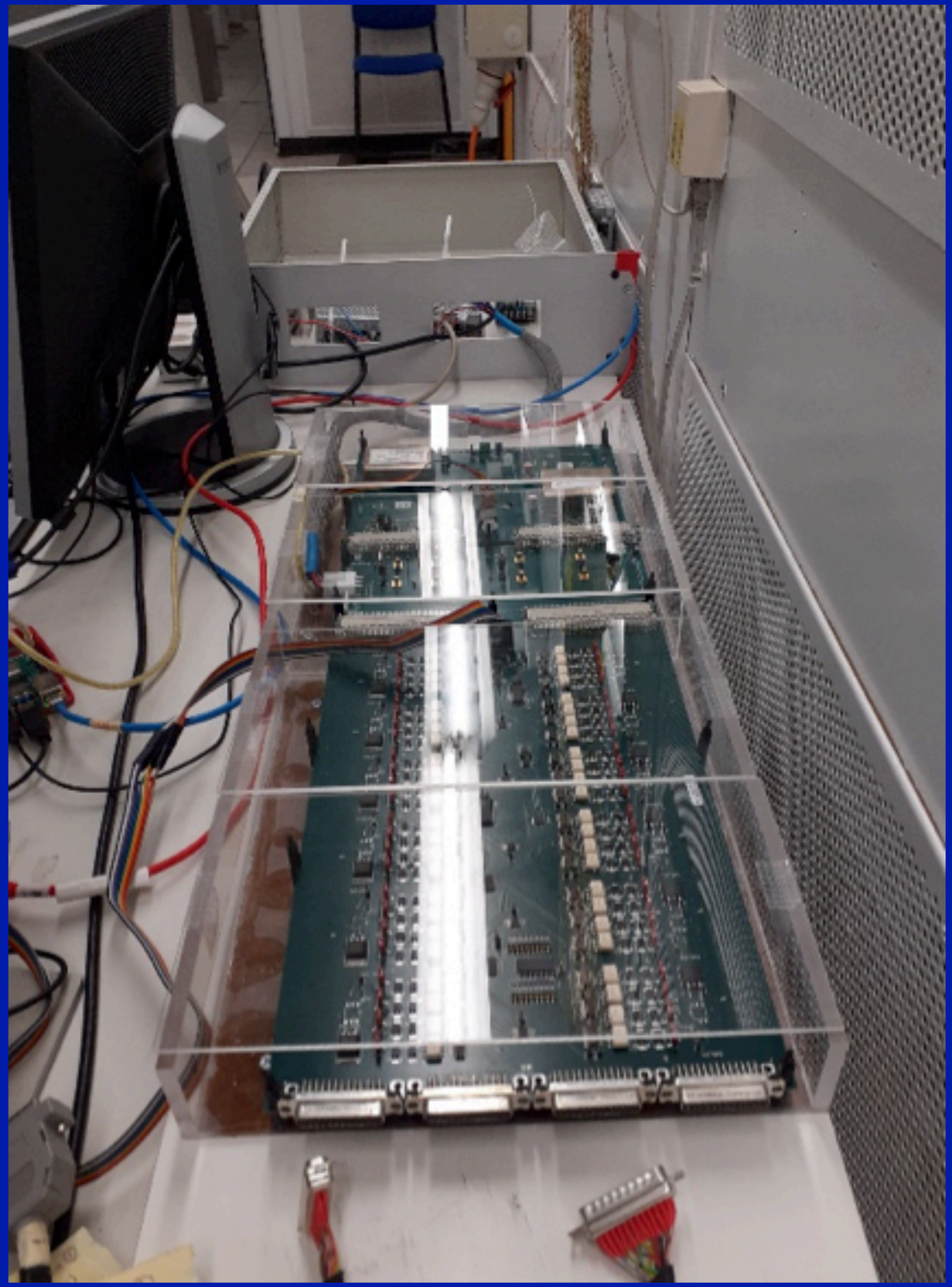
Testbeam

- HVRemote + HVBus boards tested in 2021 and June 2022
- Crate + SoC interface + final boards tested in November 2022
- Stability tests:

  > 5h long tests

  rms ≈0.21–0.23V





High Granularity Timing Detector - HGTD

30 ps resolution timing using Silicon Low Gain Avalanche Detectors (LGAD)

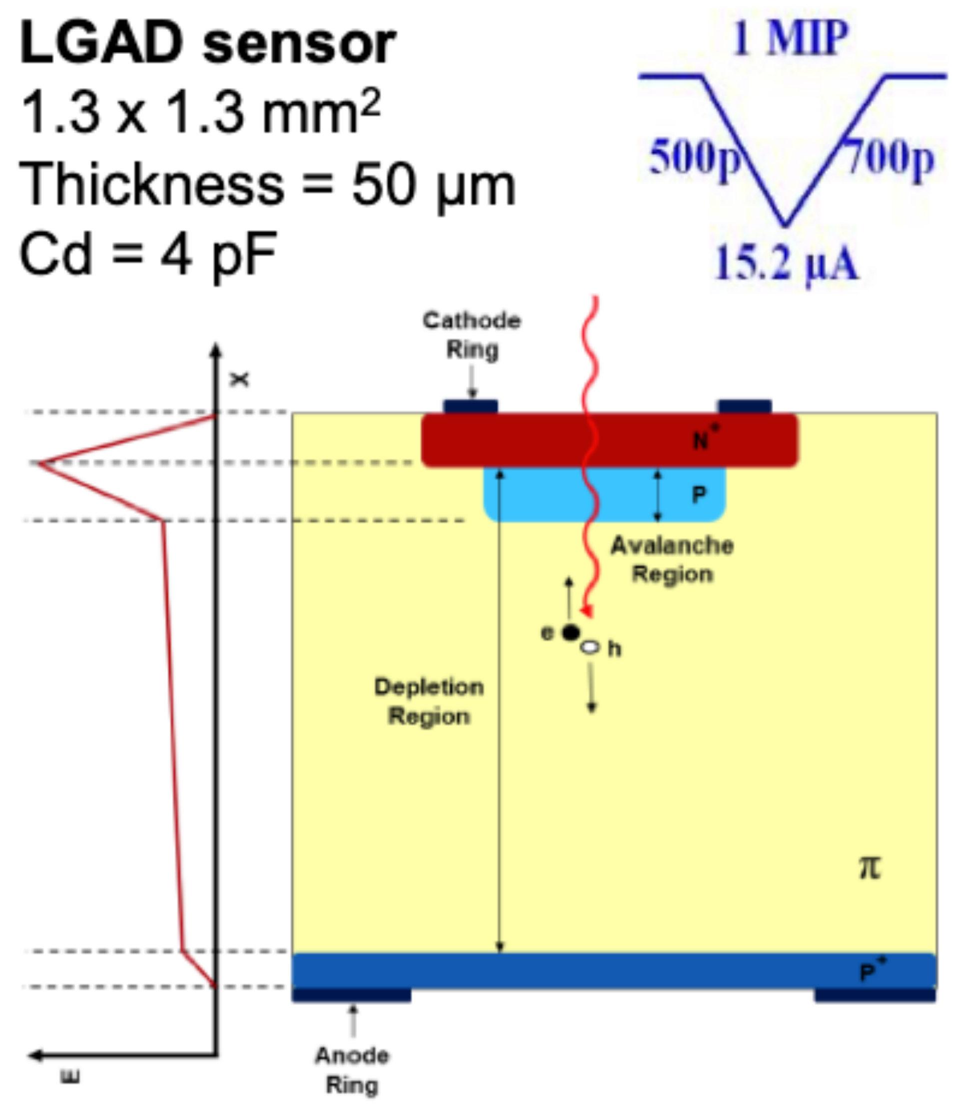
Improves pileup vertex separation and luminosity measurements

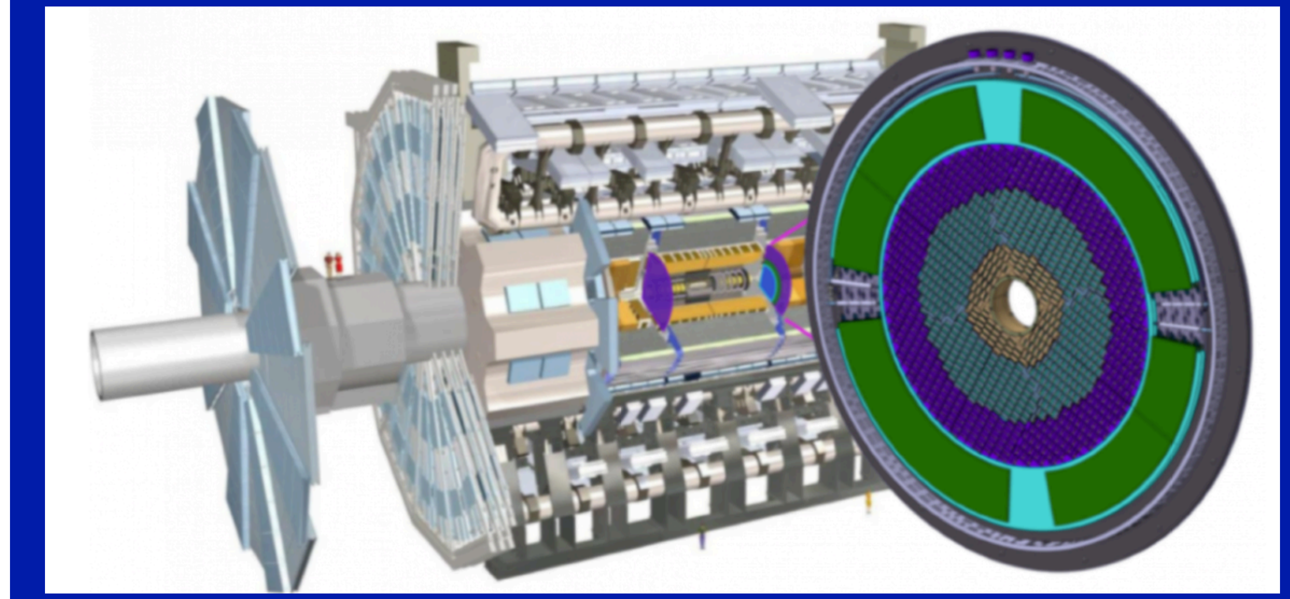
LIP contributes to several areas

- Electronics: readout ASIC tests, High Voltage filtering
- Detector slow control and safety Interlocks
- Monitoring

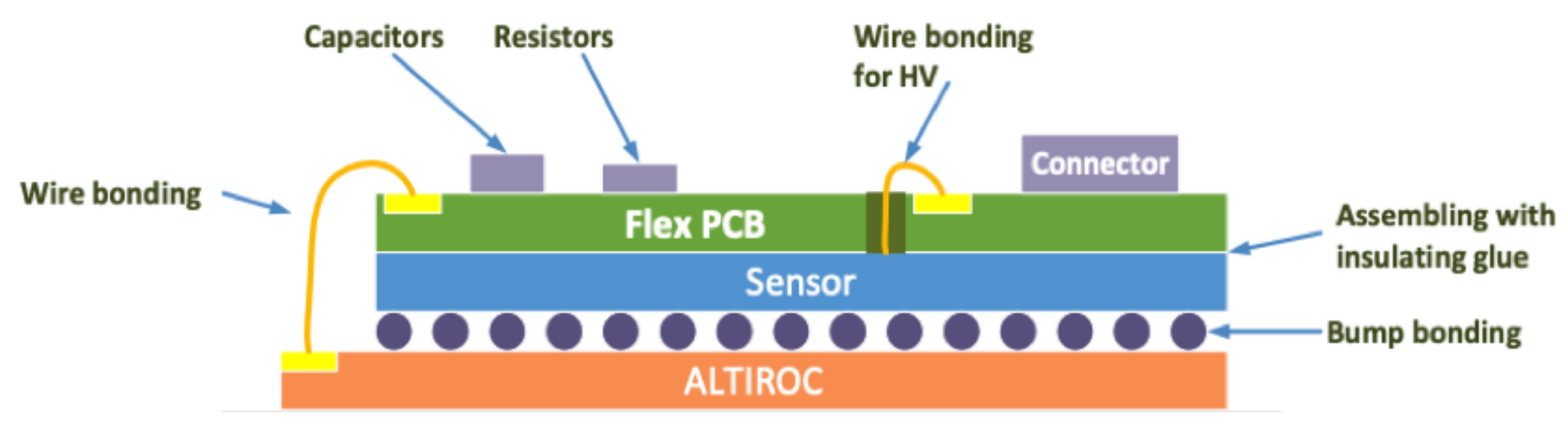
Other possibilities being followed

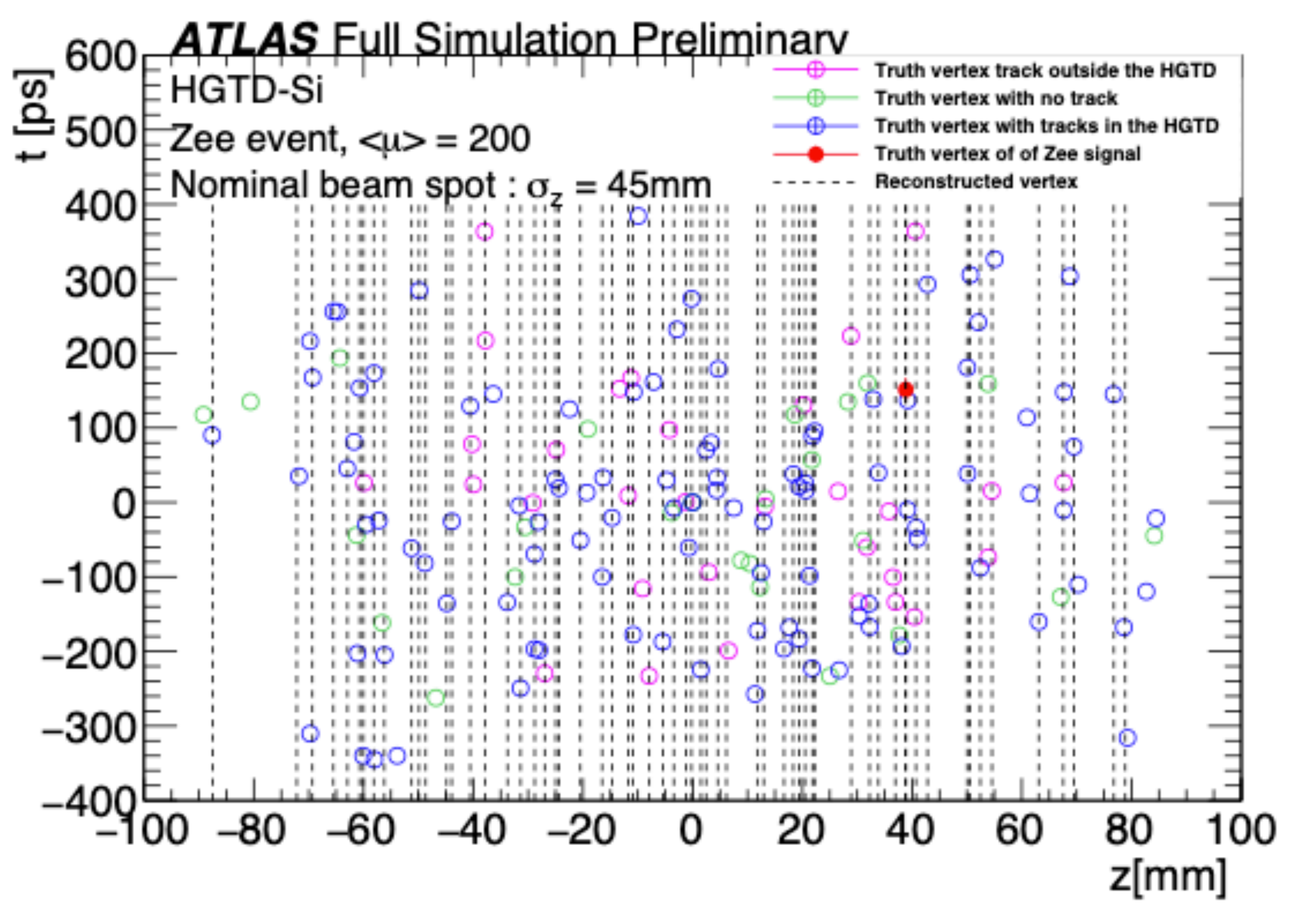
- Cable production in Portuguese industry
- Mechanical design and production at LIP





2.4 < |η| < 4.0

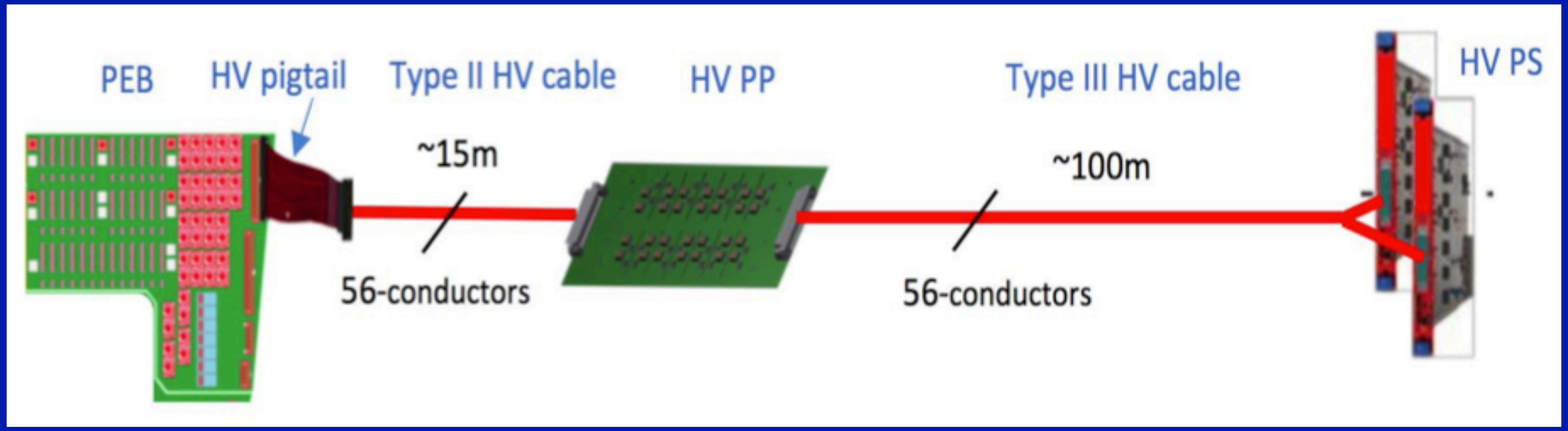


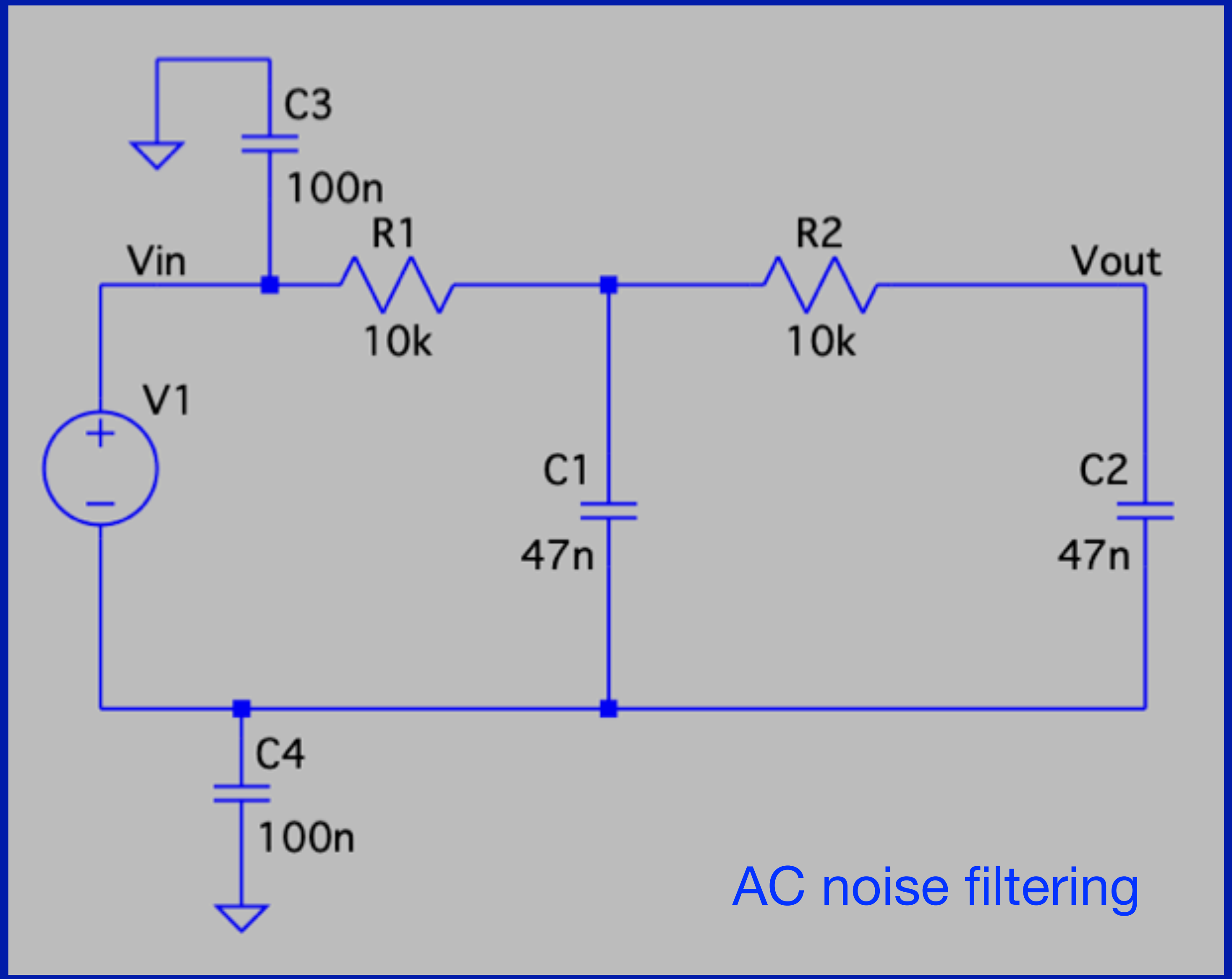


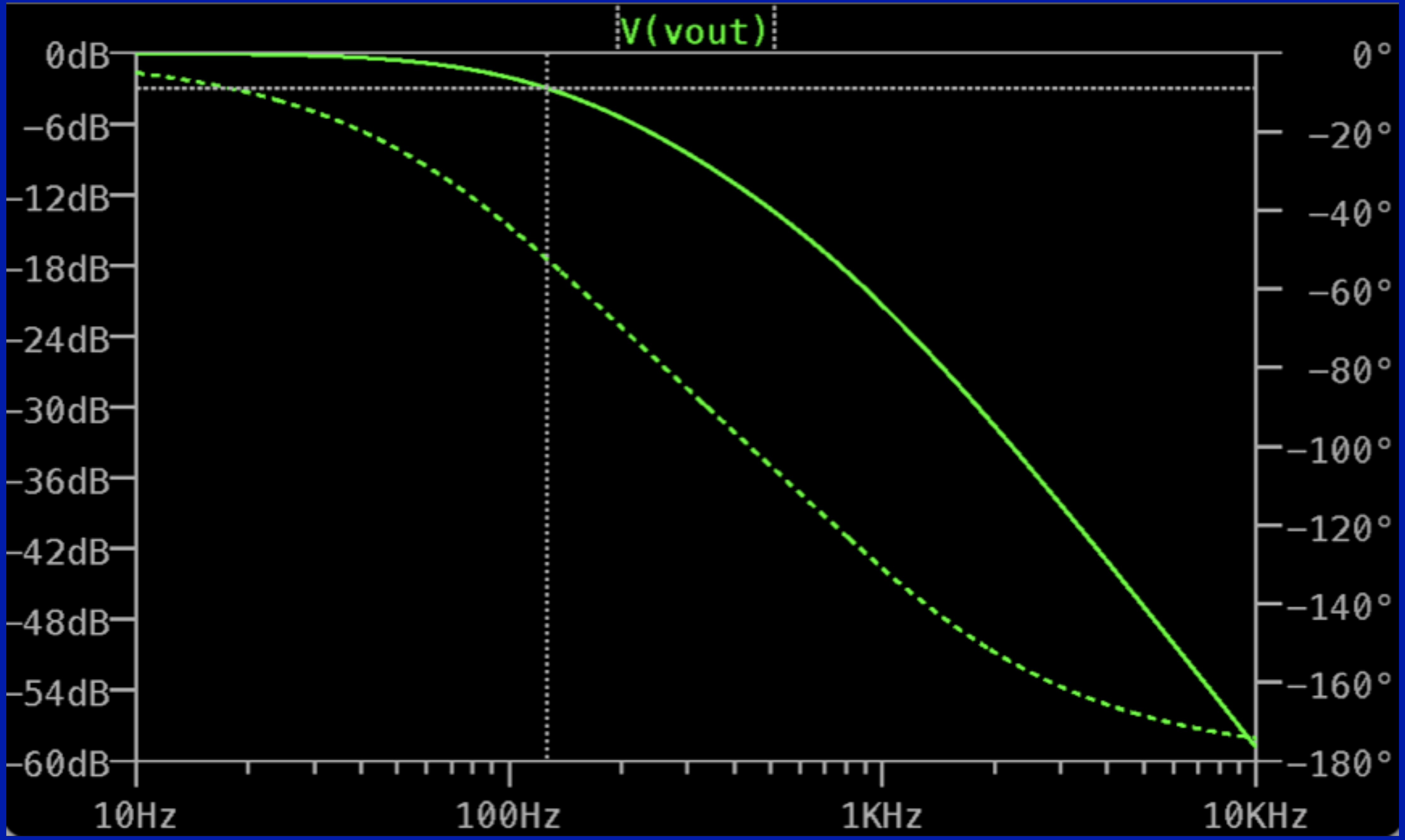
Electronics and High-Voltage

HV patch panels (PP)

- Routing the High Voltage to HGTD detector
- HV brought to low pass filters in the PP to filter AC noise
- LIP responsability

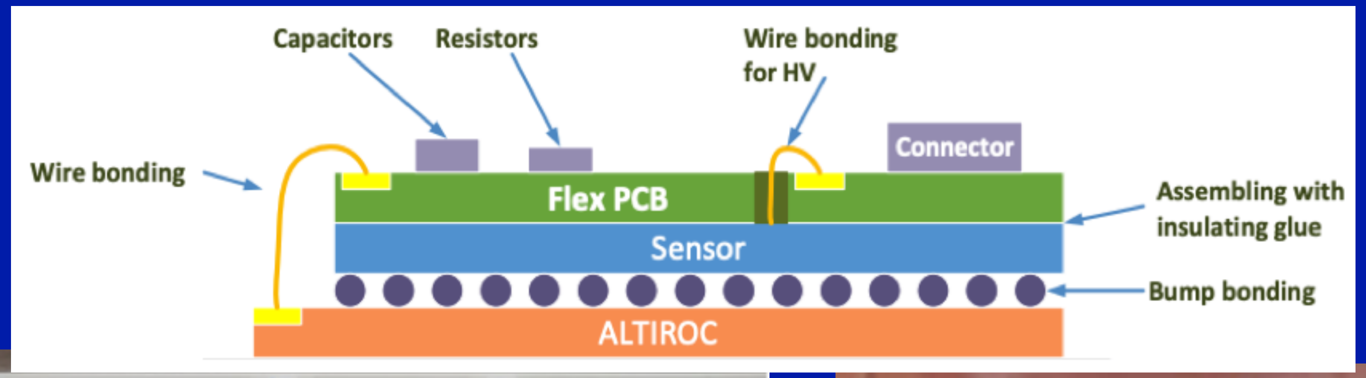


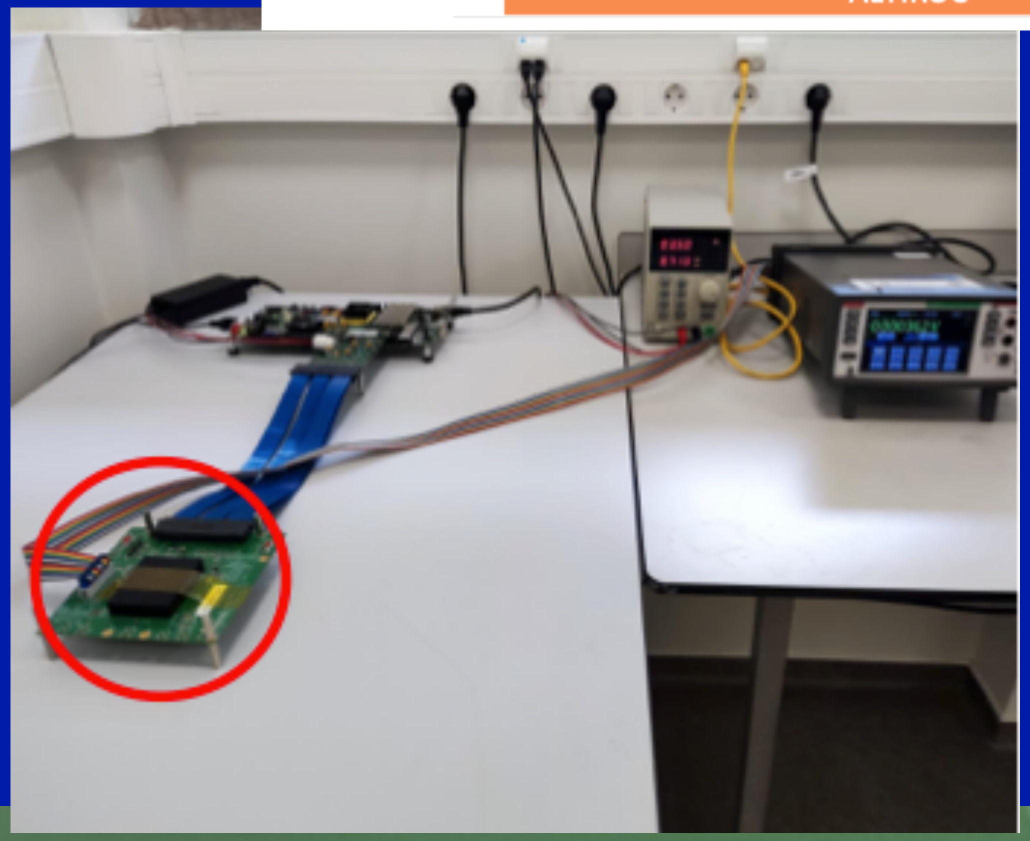


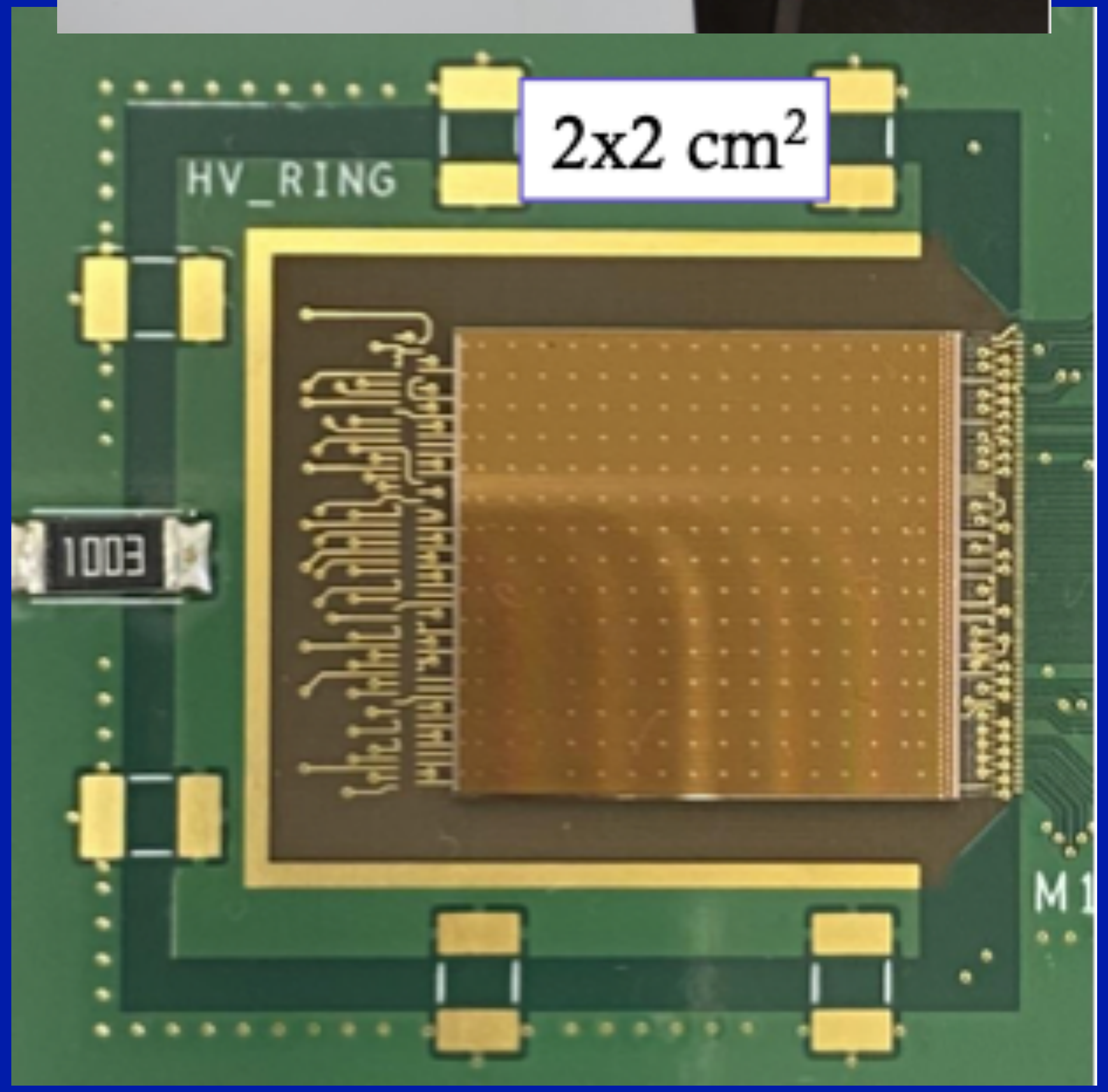


Electronics and High-Voltage

ALTIROC (ASIC under development for LGAD readout)



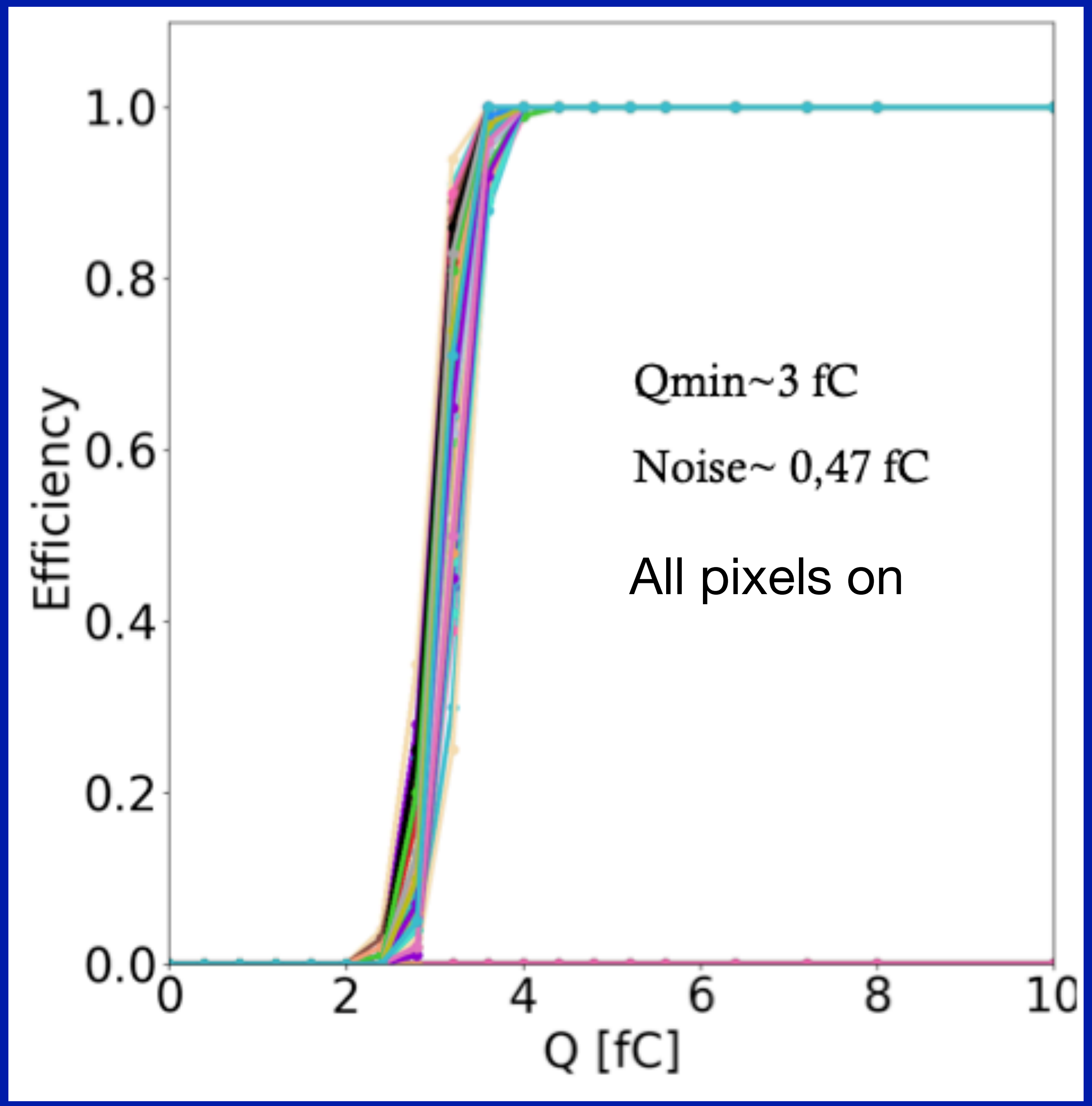




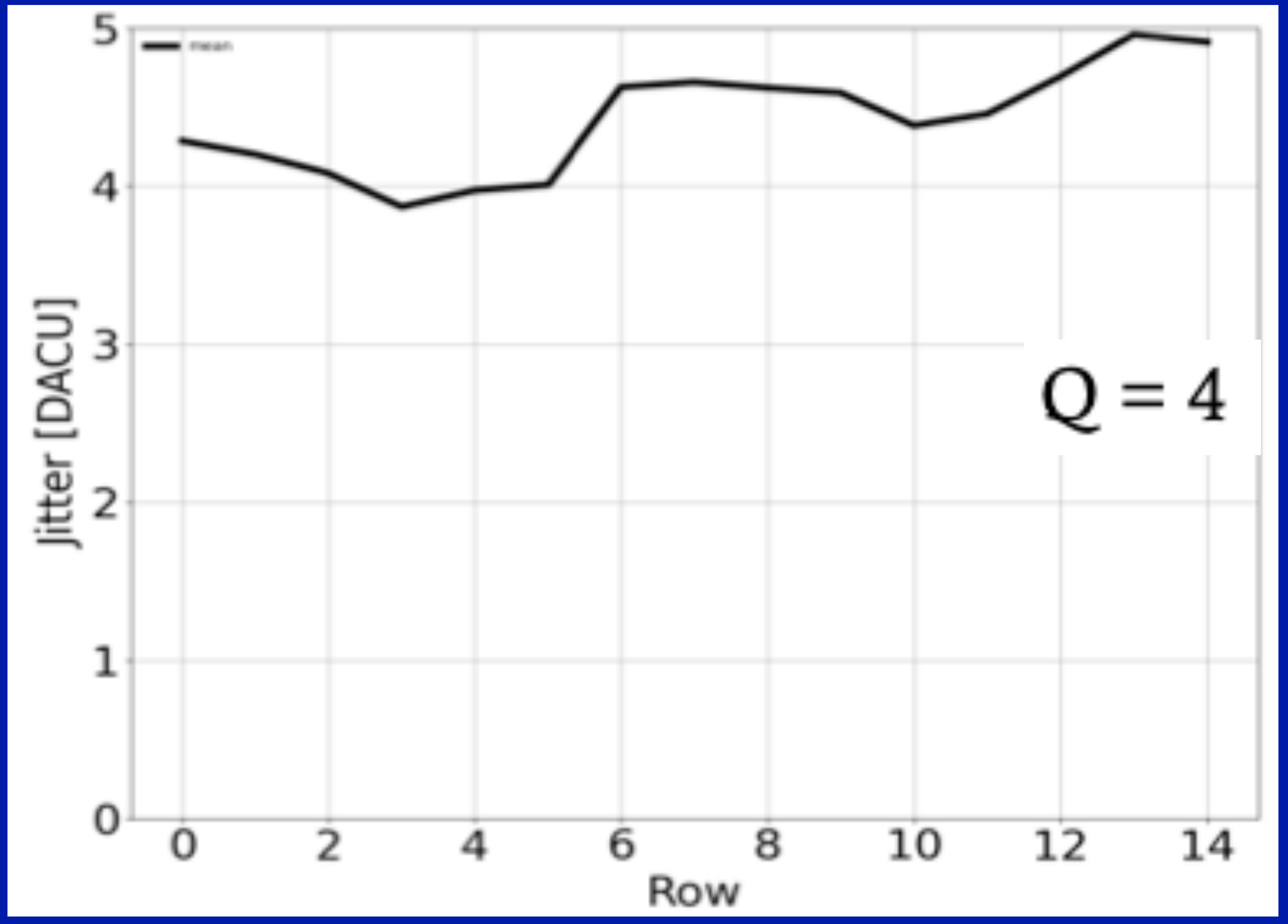
- TID @ 200MRad
- Module at-40 ºC

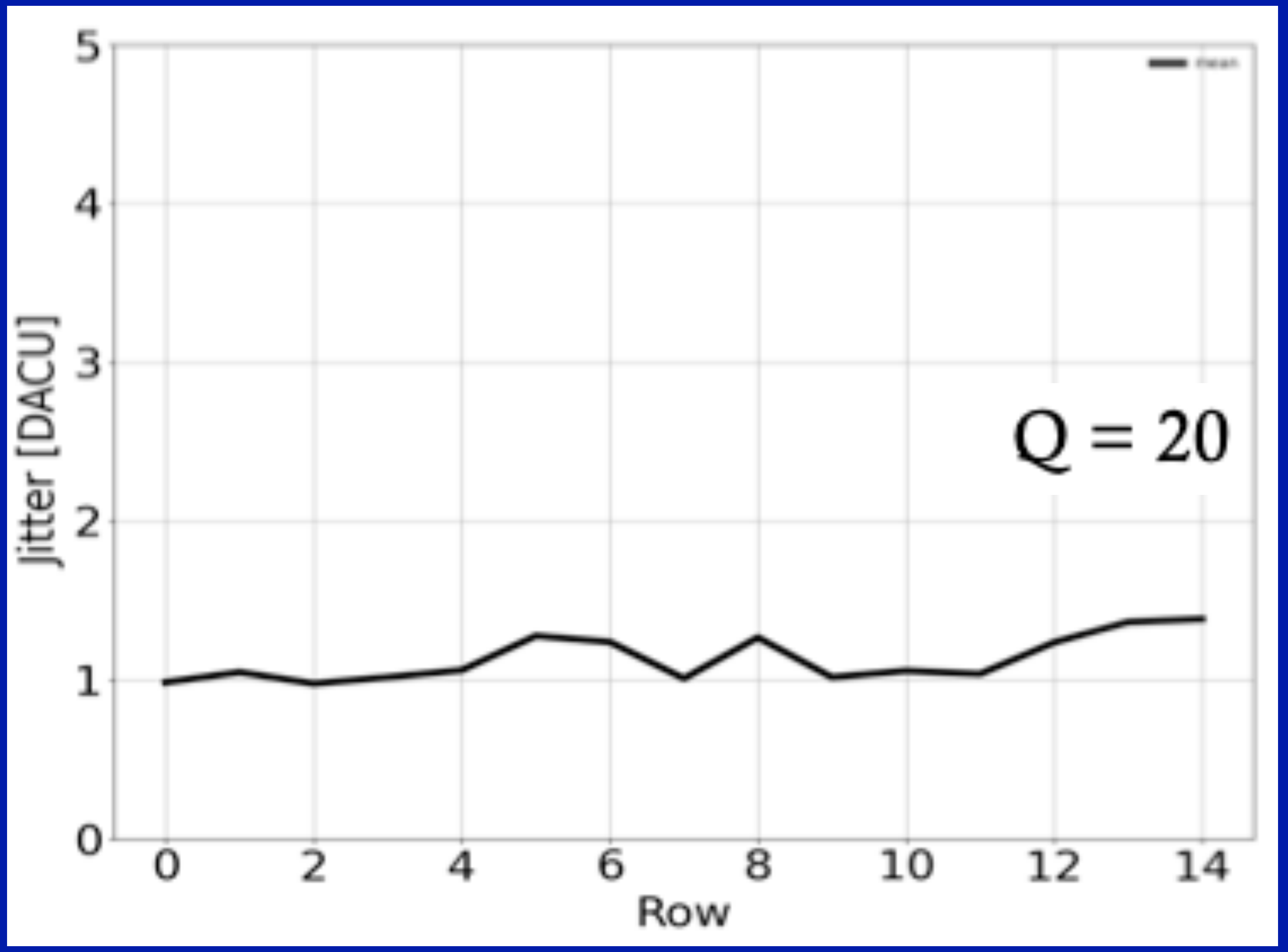
Setup for irradiation tests

minimum detectable charge



Qmin and jitter tests





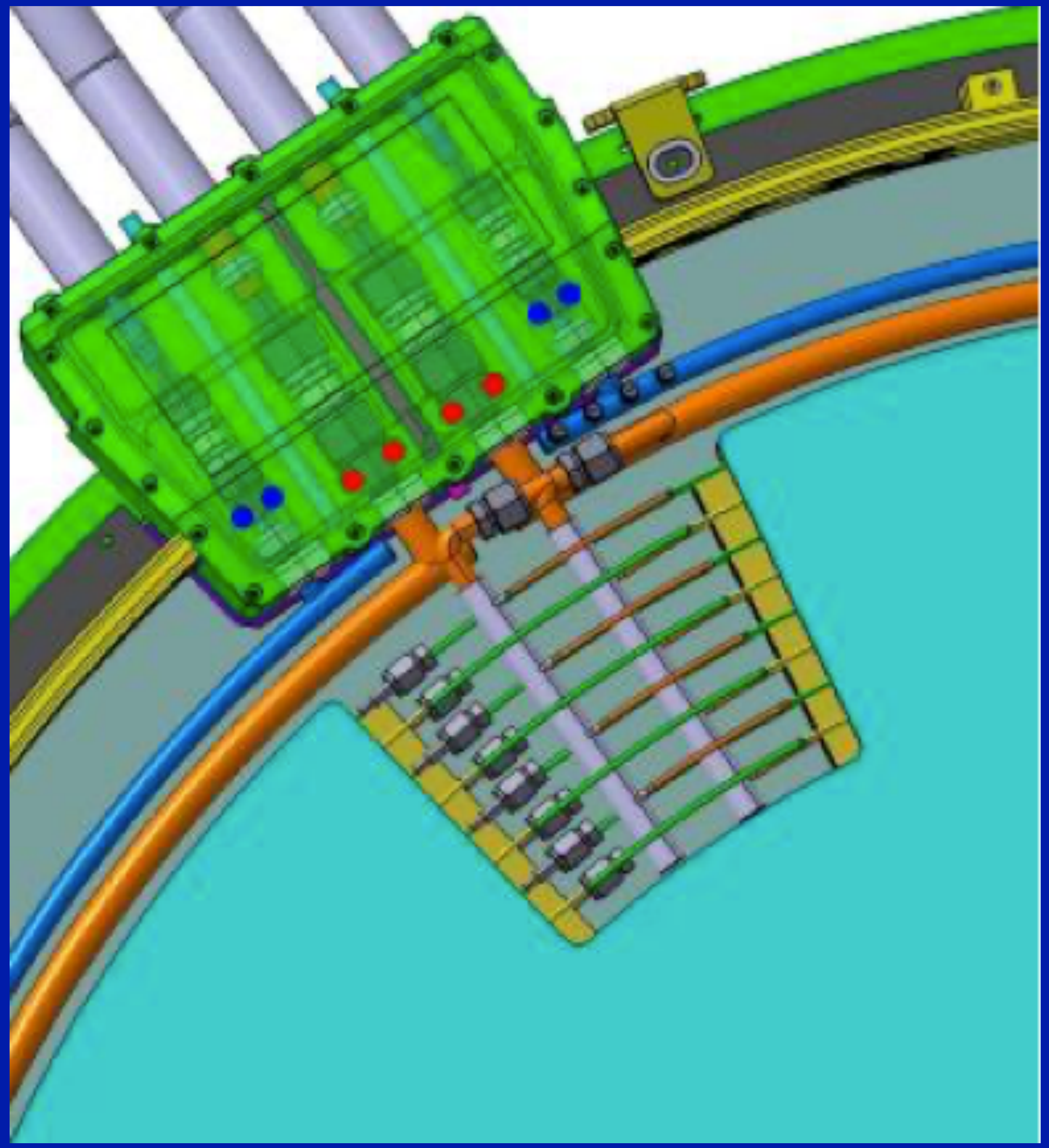
HGTD - DCS and Interlock

Detector Control System (DCS)

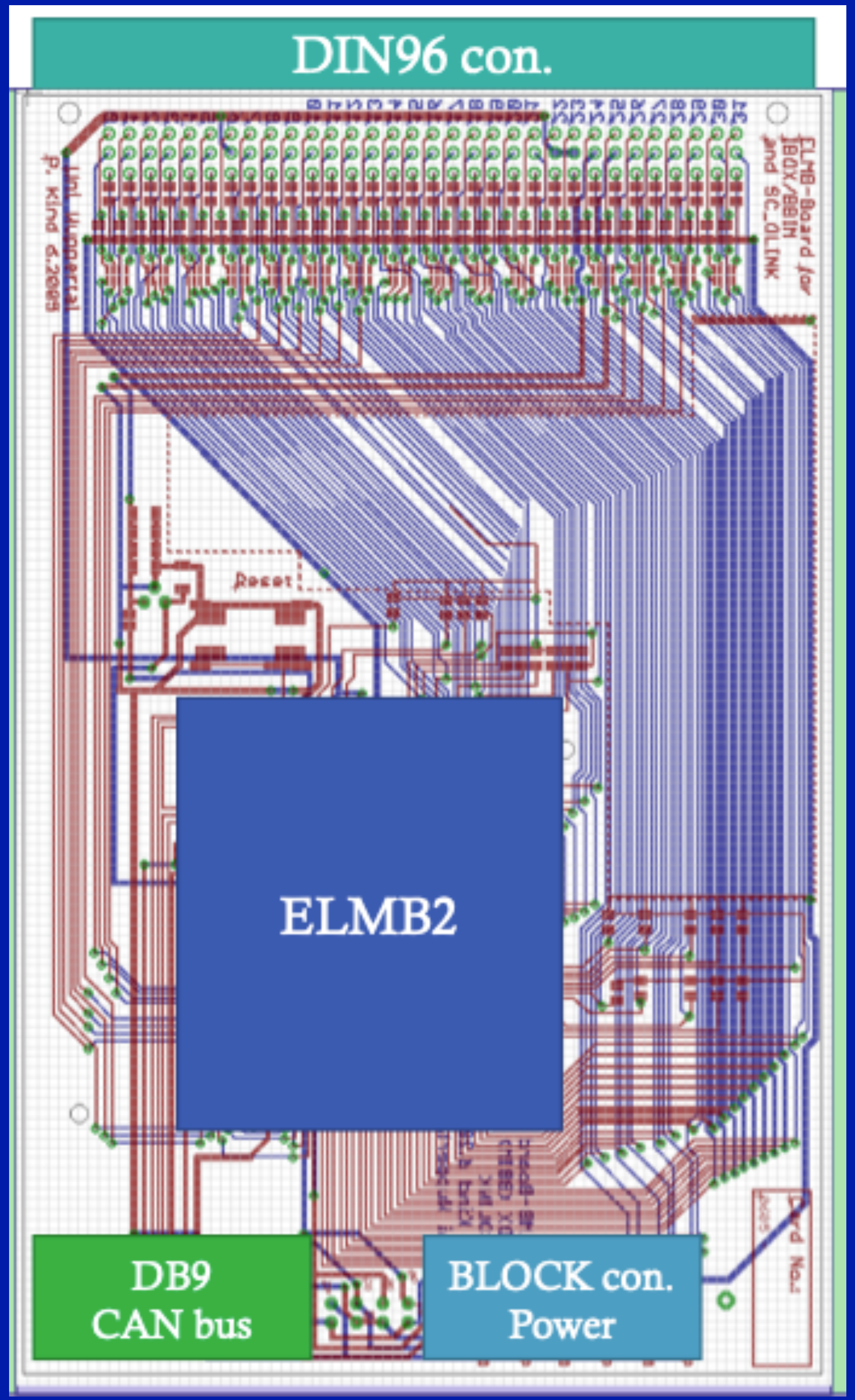
– Contributing to DCS architecture definition

– Readout of DCS environment data through ELMB2 communication board

monitoring of the CO_2 cooling system via Pt10k sensors

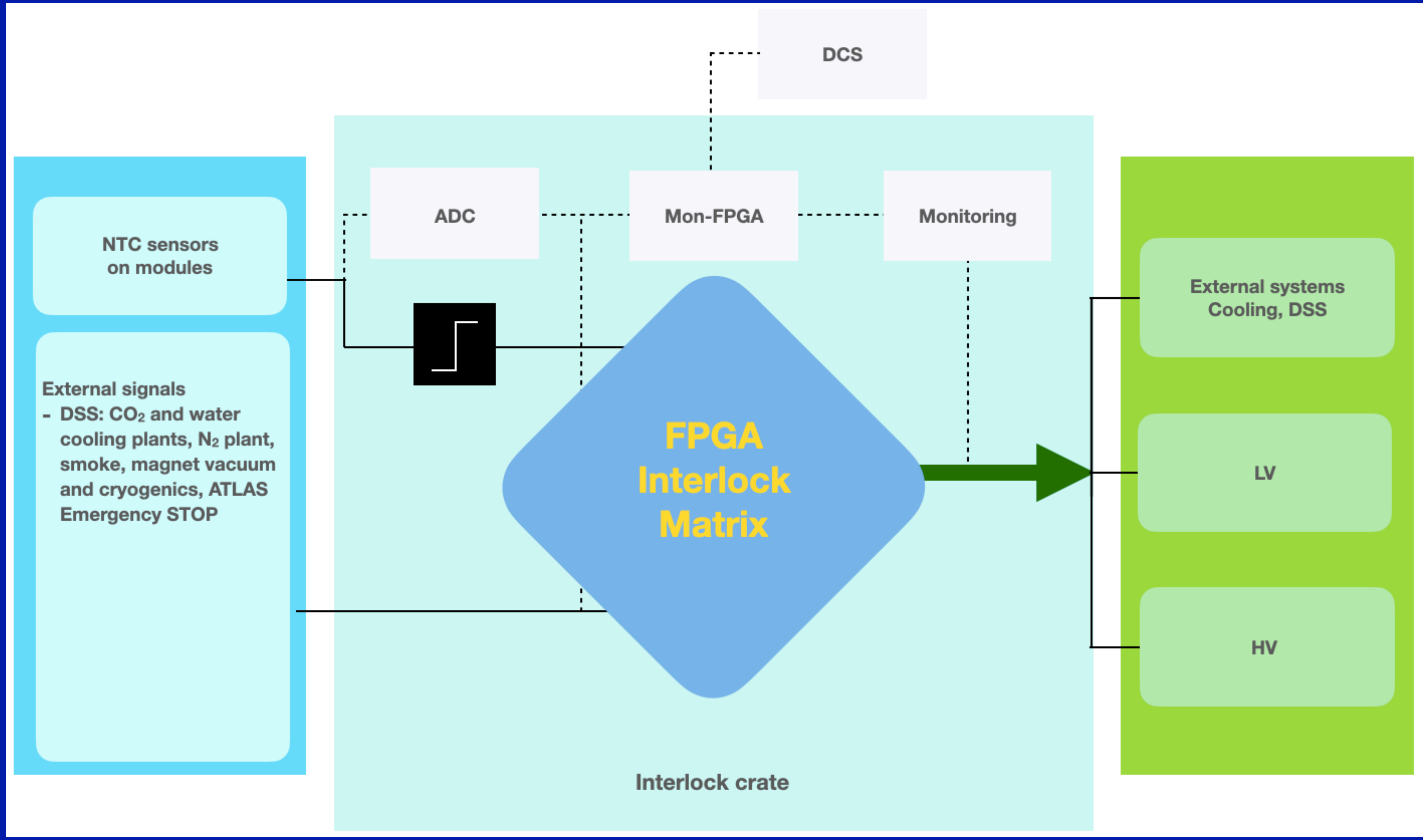


- Temperature range: from −45○C to +20○C
- Maximal tolerable offset (accuracy) of sensor: ±0.2○C
- Precision of sensor: ±0.5○C



- same ELMB board as ITk
- Signal Conditioning board, backplane of both boards and power supply to be designed

HGTD - DCS and Interlock



Interlock

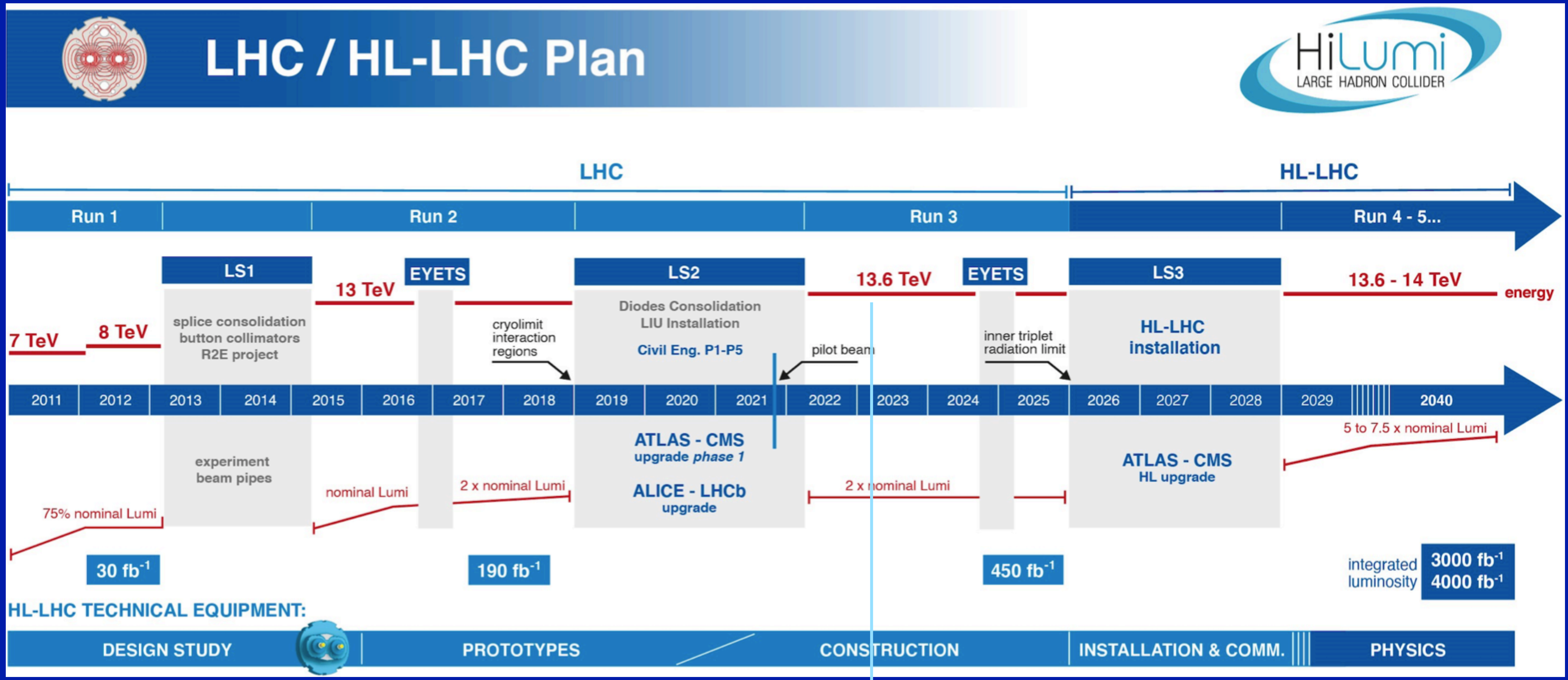
- Mostly re-use the ITk one
- Contributing to module production
- Safety algorithms to be built
- Passed PDR (Preliminary Design Review)
- LIP responsability

- On the left are detectors that recognize threats from which protection is necessary.
- On the right are the devices that should be switched off.
- The central part is the interlock crate, which contains FPGA to define interlock matrix.

Summary and Outlook

HL-LHC —> a harsher radiation environment and higher pileup, luminosity, read-out rates

- New era for trigger and tracking reconstruction algorithms facing 1 MHz first level trigger rate
- TileCal upgrade project is well on track: New mechanics and electronics more radiation hard, more reliable and easier to service
- The HGTD will improve many physics analysis by associating time to tracking, diminishing the impact of pileup and decreasing the luminosity uncertainty
- LIP is deeply committed with ATLAS-Upgrade contributing significantly to TileCal, HGTD and Trigger projects



today

backup

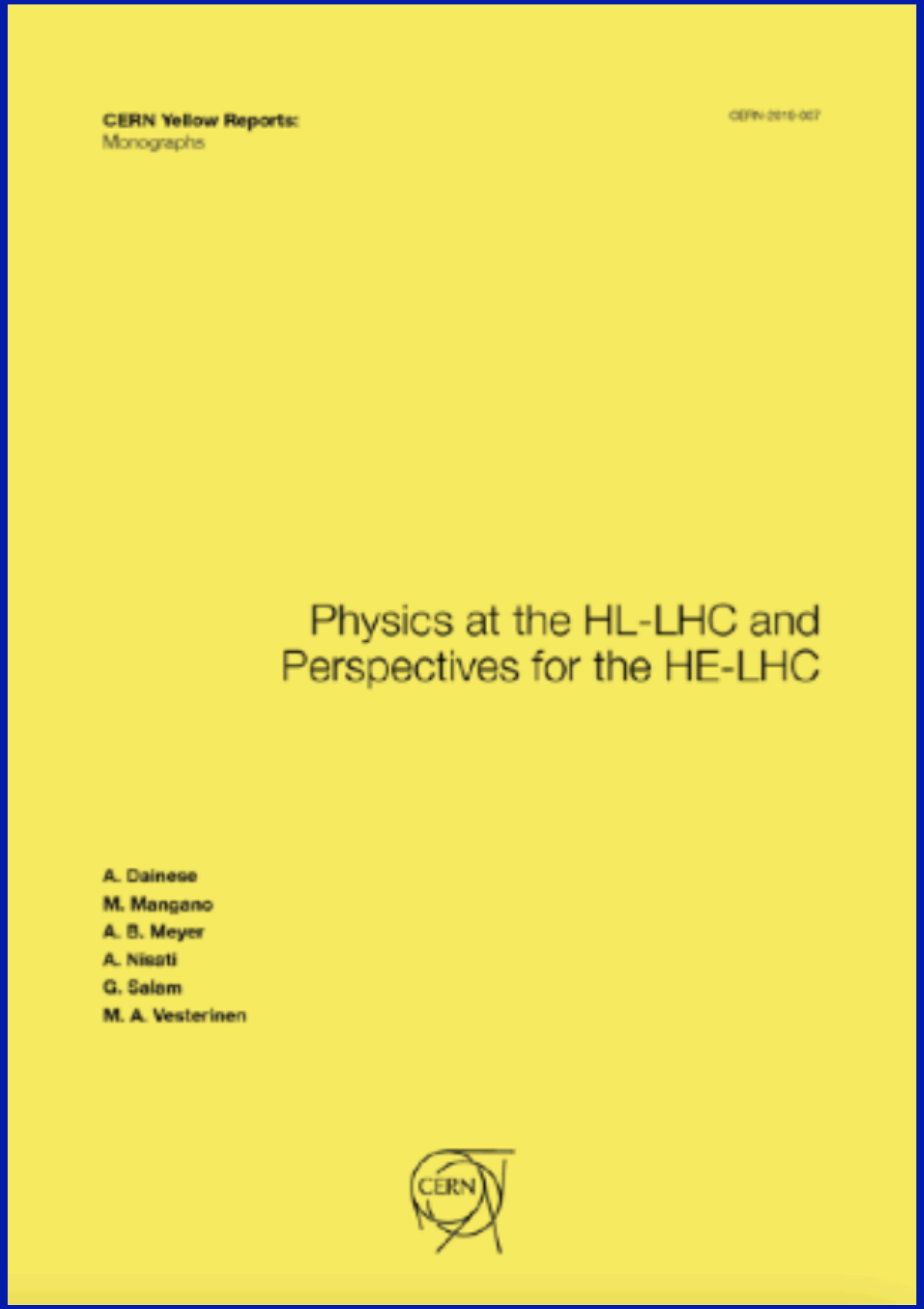
The High Luminosity LHC (HL-LHC)

HL-LHC approved by CERN council in June 2016:

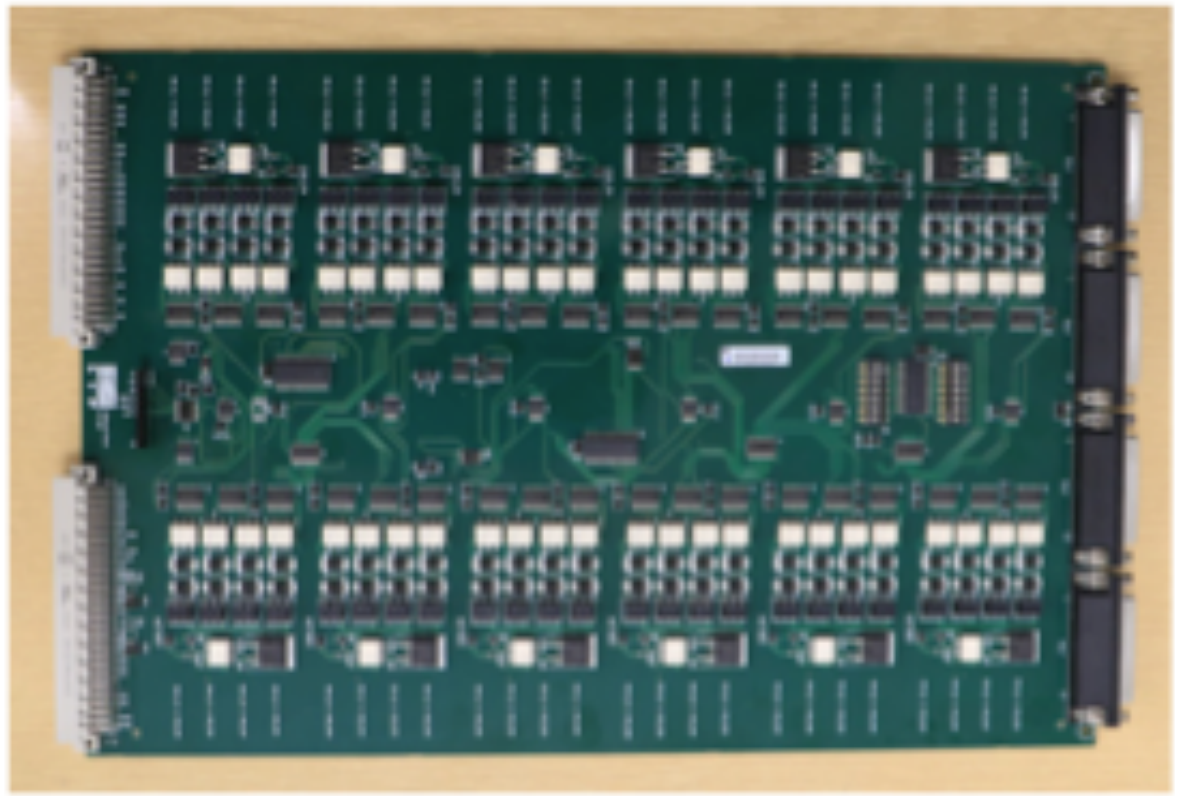
“Europe’s top priority should be the exploitation of the full potential of the LHC, including the high-luminosity upgrade of the machine and detectors with a view to collecting ten times more data than in the initial design, by around 2030. This upgrade programme will also provide further exciting opportunities for the study of flavour physics and the quark-gluon plasma.” (European Strategy 2013)

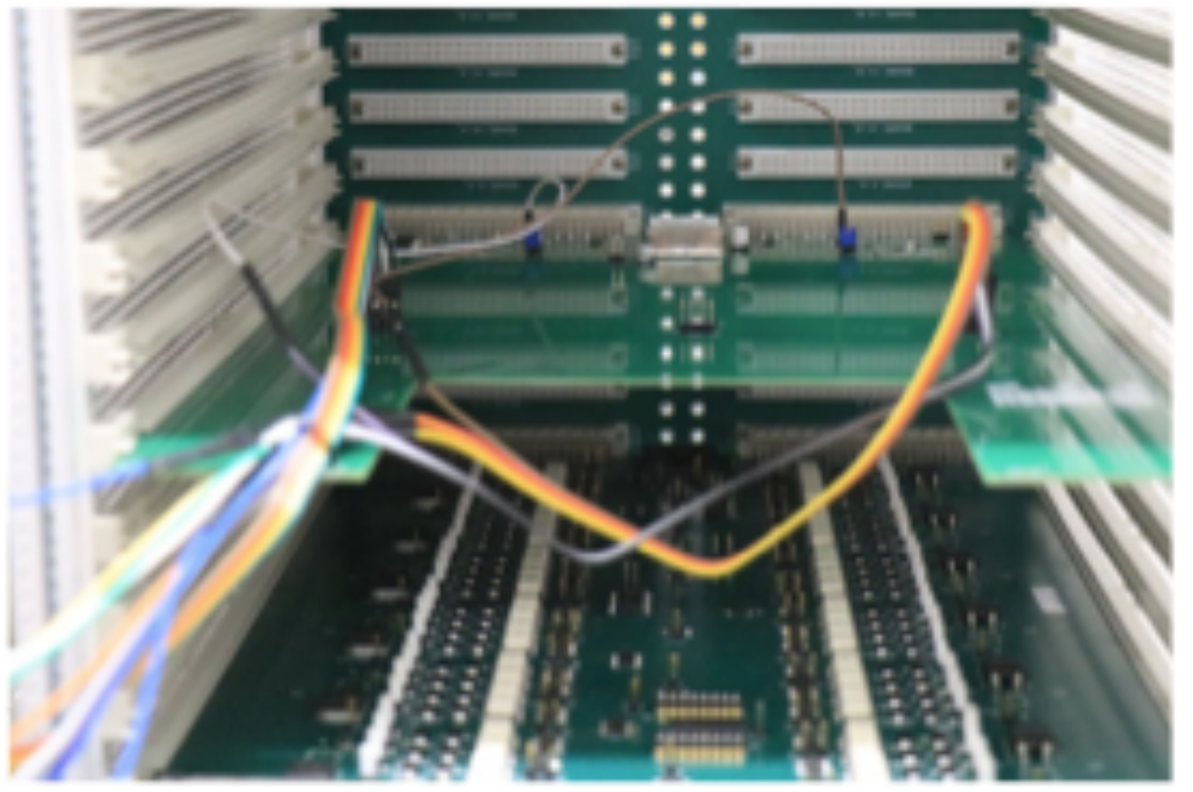
“Detector R&D programmes should be supported strongly at CERN, national institutes, laboratories and universities. Infrastructure and engineering capabilities for the R&D programme and construction of large detectors, as well as infrastructures for data
analysis, data preservation and distributed data-intensive
computing should be maintained and further developed.” (European Strategy 2013)

There is a very wide physics program defined for HL-LHC:
https://cds.cern.ch/record/2703572/files/94-87-PB.pdf



High Voltage System Components





HVSupplies:

- DC-DC converters to produce primary HV
- Connects with the ATLAS Detector Safety System
- First prototypes successfully tested and a new design finished for production
- Designed by eCRLab

HVRemote:

- Receives 2 primary HV inputs from HVSupplies
- Sends 32 or 48 individually regulated HV outputs to HVBus
    - DACs to set the individual voltages
    - Regulation loops based on optocouplers

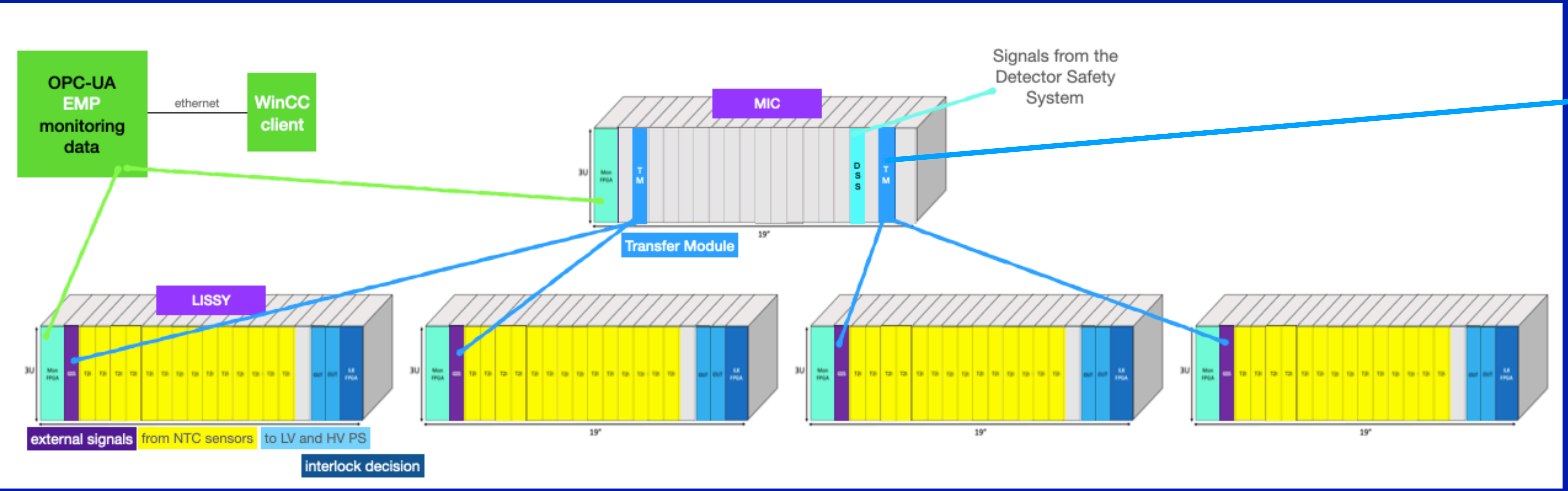
HV Control Board:

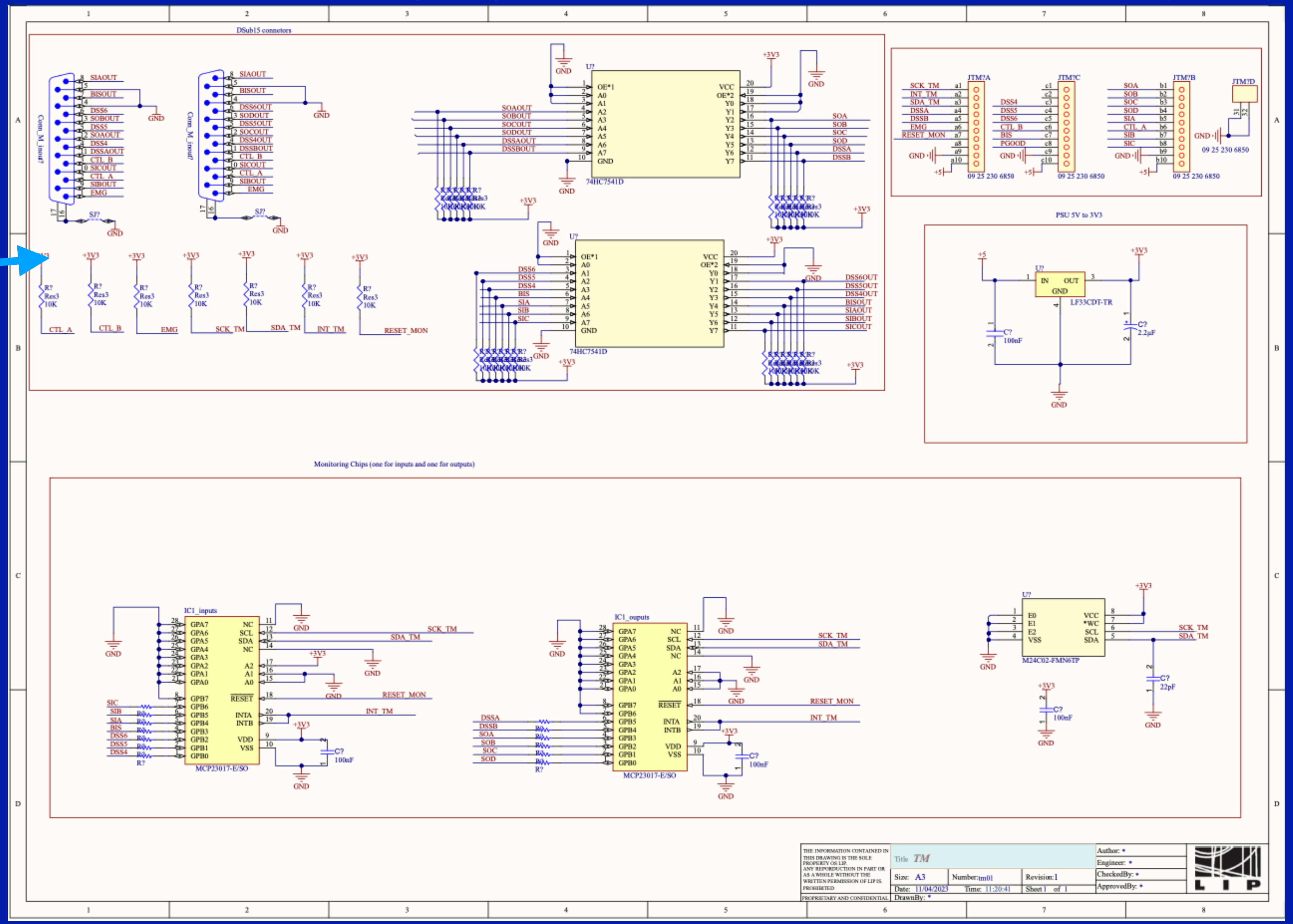
- One Zybo Z7 Zynq System-on-Chip (SoC) interface board per crate
- Two SPI buses (one to the HVRemote and other to the power supply boards);

HGTD - DCS and Interlock

Transfer Module (TM) in the Main interlock Crate (MIC)

Conceptual design of the HGTD interlock system





- Four Local Interlock & Safety SYstem (LISSY) crates.
- One Main Interlock Crate (MIC), responsible for the distribution of global (external) signals to the individual LISSY crates.
- The MON-FPGA module in both crates collects monitoring data and provides an interface for DCS via the Embedded Monitoring Processor (EMP) and OPC server.
- Producing the TM

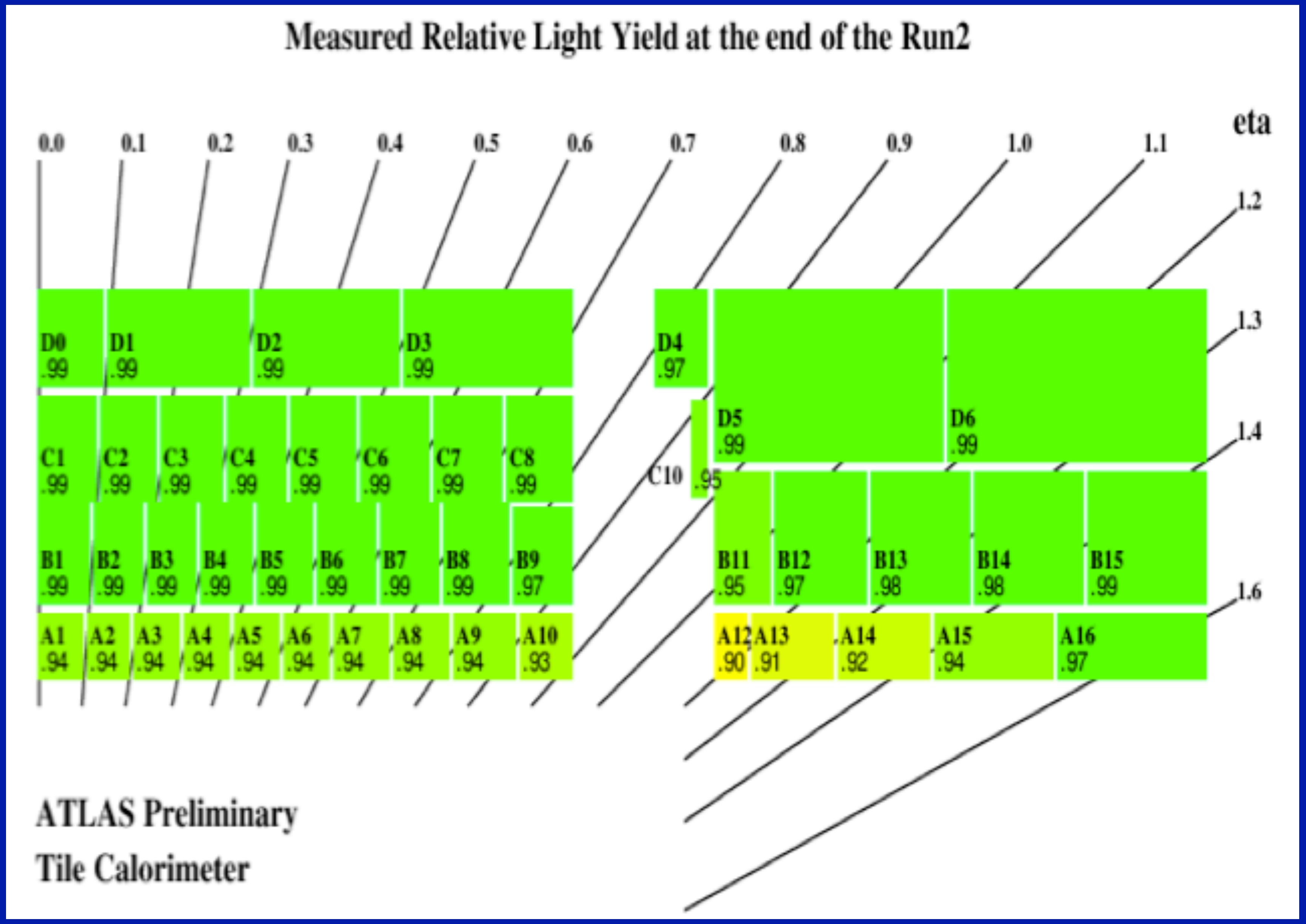
TileCal Optics Robustness for HL-LHC

The HL-LHC will bring additional radiation exposure and damage to the TileCal scintillators and fibres

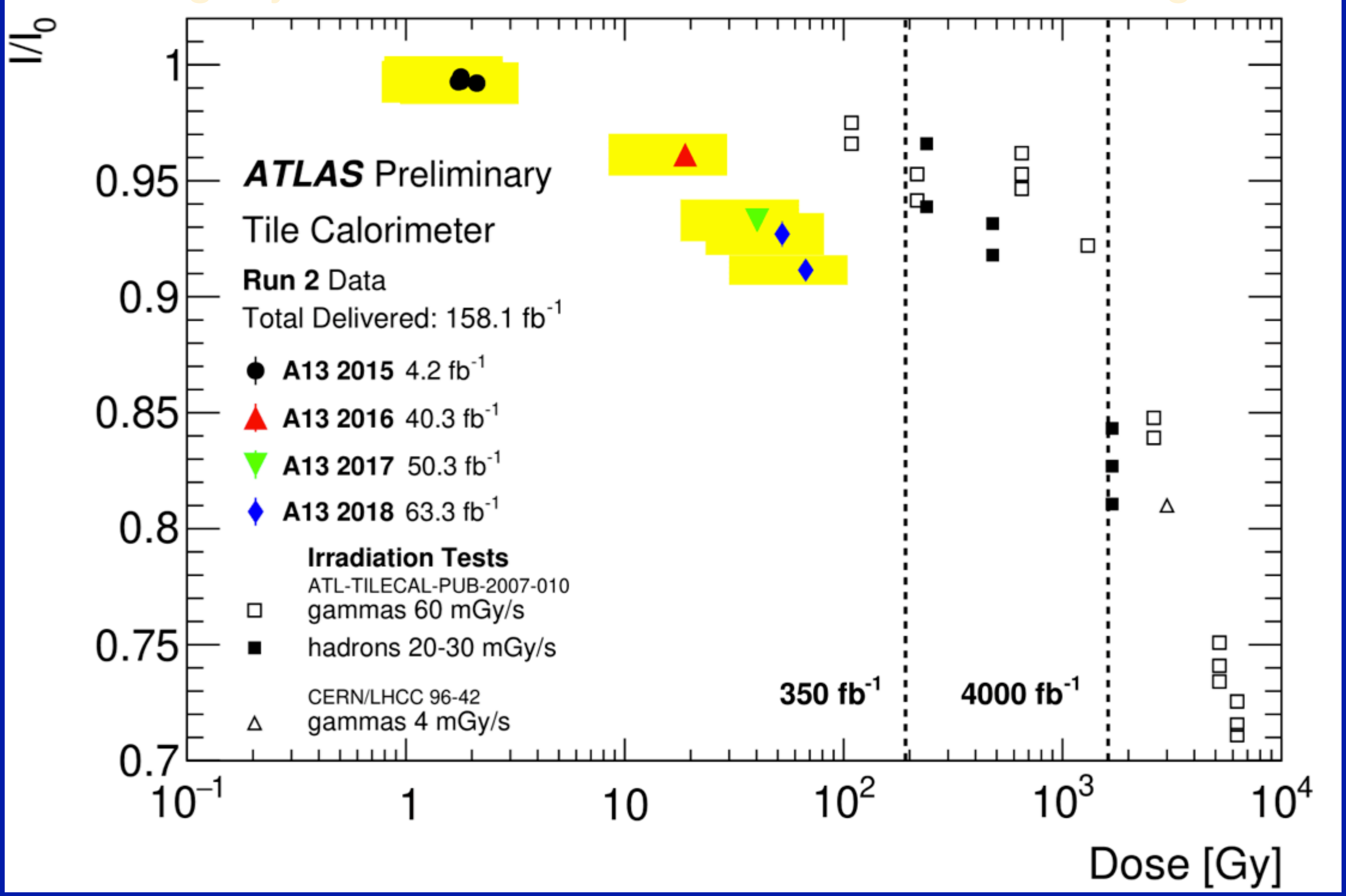
- Measured Run 2 light yield from 137Cs and laser data

$$I/I_0 = 1 + \frac{\Delta x^{Cs} - \Delta x^{Las}}{100\%}$$

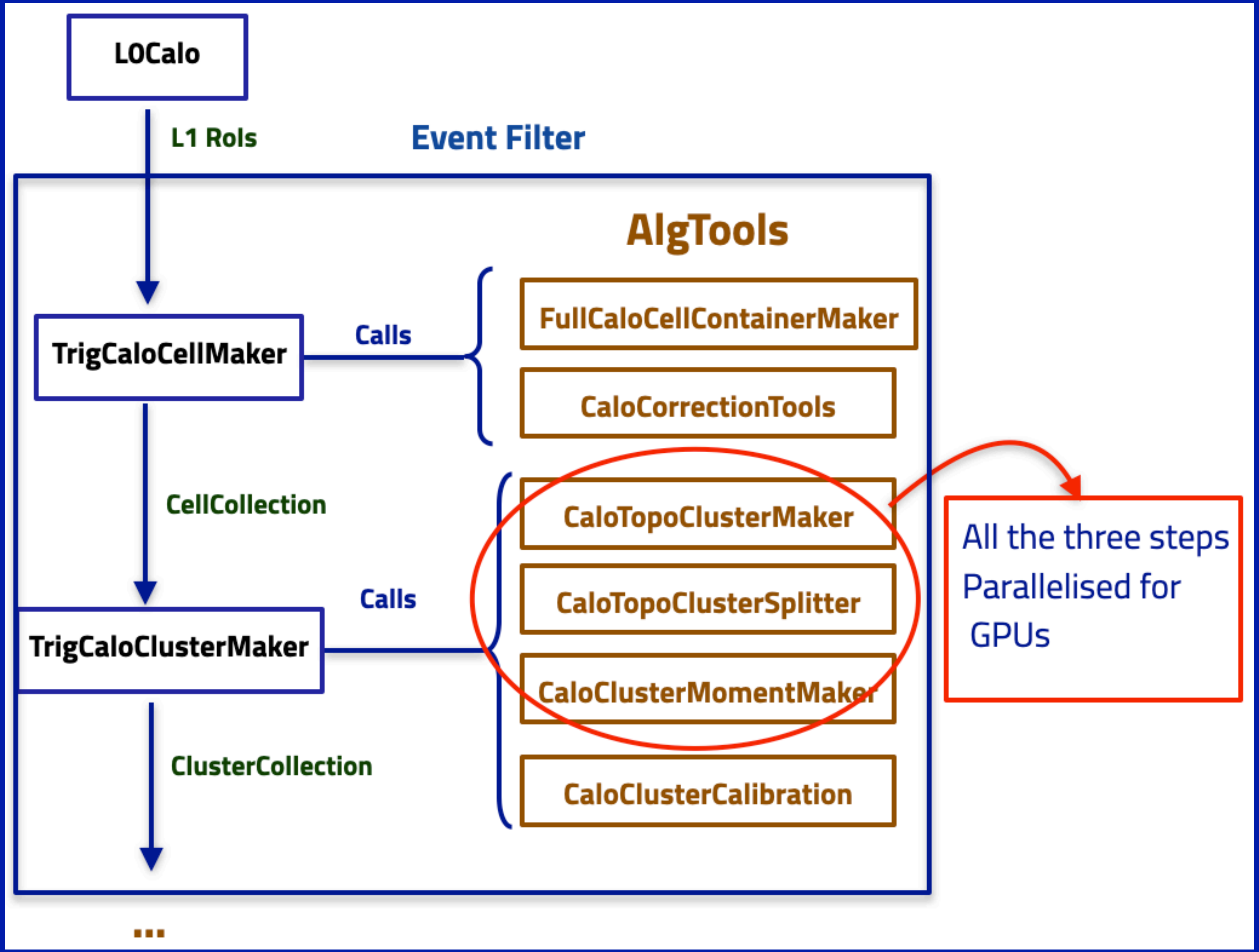
Δx is the cell's deviation to the reference scan.
The difference between Cs and Laser response corresponds to a variation of the scintillators and fibres response;



relative light yield of scintillators as a function of ionising dose



HLT calorimeter reconstruction



Use the same structure for GPU algorithms

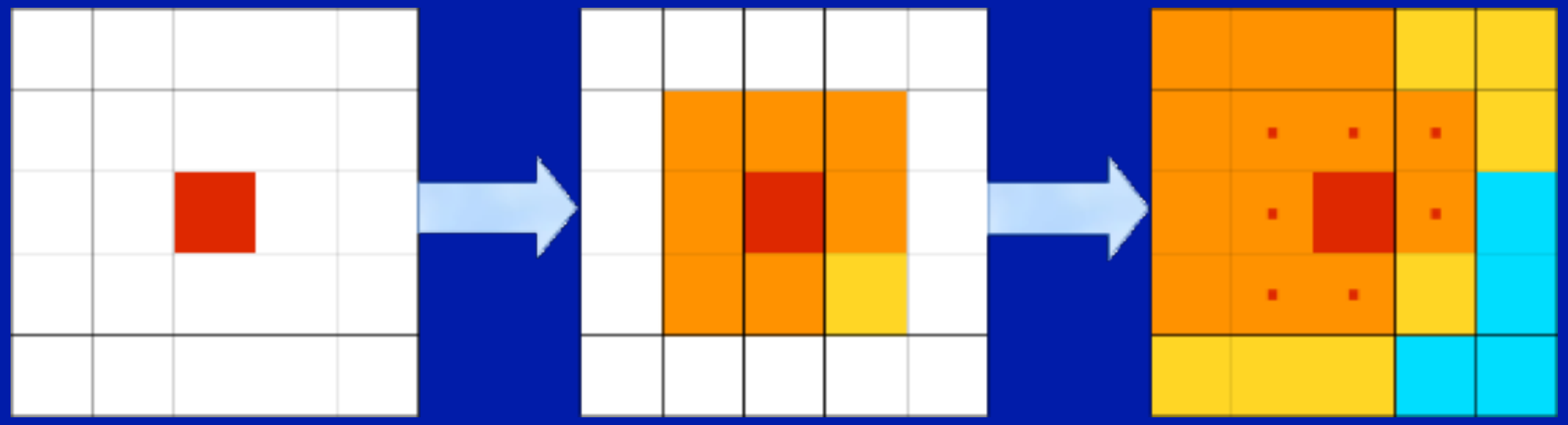
- Flexibility with respect to which algorithms to run on the GPU

Each algorithm accesses the GPU directly

Calo cluster growing phase

TopoCluster reconstruction on CPU (~8% of total time)

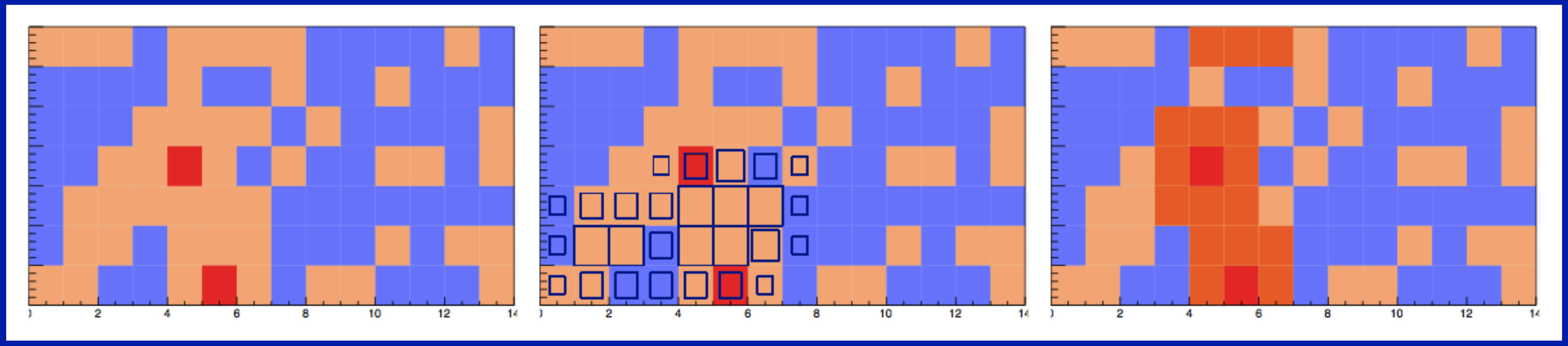
- Group cells in 3-dimensions according to their signal/noise ratio



TAC: Topo-Automaton Clustering

- Use a cellular automaton for the GPU (maximize parallelism)
- Propagate tag on a grid of elements (cell pair)

Cells get the largest tag on each iteration



Test results

- Calorimeter clusters compared one by one
- Timing measurements obtained by running the full sample and subtracting the cell making and Athena execution times
- GPU times include cluster growing, cluster splitting, data conversions and data transfers from CPU to GPU and back
- Very preliminary single thread speed-up factors:
4 for di-jet events (average) and 3.5 for ttbar events
- Fraction of time dedicated to the algorithms: 5-20% (depending on the algorithm)
- Rest of the time: data conversion/transfer overhead