Development of monolithic sensors for high energy physics in TPSCo 65nm ISC technology

CERN EP R&D

WP1.2 Monolithic Pixel Detectors

Many contributors, see next page

Strong synergy with ALICE ITS3 upgrade

Development of monolithic sensors for high energy physics in TPSCo 65nm ISC technology

University and INFN Torino: F. Benotto, S. Beole, C. Ferrero U. Savino, S. Perciballi, F. Prino, A. Turcato
University and INFN Bari: G. De Robertis, F. Loddo
University and INFN Catania: P. La Rocca, A. Triffiro
University and INFN Cagliari: D. Marras, , V. Sarritzu, G. Usai
University of Salerno and Bologna: R. Ricci
University and INFN Trieste: M. Antonelli, R. Baccomi, M. Buckland, P. Camerini, G. Contin, S. Rashevski A. Villani
CPPM: P. Barrillon, M. Barbero, D. Fougeron, A. Habib, P. Pangaud
IPHC: J. Baudot, G. Bertolone, A. Besson, S. Bugiel, C. Colledani, A. Dorokhov, Z. El Bitar, X. Fang, M. Goffe, C. Hu, K. Jaaskelainen, F. Morel, H. Pham, S. Senyukov, J. Soudier, I. Valin, Y. Wu (also with USTC)
NIKHEF: R. Russo, V. Gromov, D. Gajanana, A. Yelkenci, A. Grelli, R. Kluit, J. Sonneveld, A. Vitkovskiy
Heidelberg University: P. Becht, S. Masciocchi, M.W. Menzel, H.K. Soltveit, A. Yuncu, J. Stachel
Munster University: A. Andronic, N. Tiltmann
Prague University: A. Isakov, A. Kotliarov, F. Krizek
STFC (RAL): S. Matthew, I. Sedgwick
Birmingham University: L. Gonella
Technical University Munich: L. Lautner, I. Sanna (also with CERN), L. Fabiette
Technical University Vienna: J. Hasenbichler (also with CERN)
DESY: K. Hansen, C. Reckleben, S. Spannagel

Yonsei University: Y. Kwon, G.H. Hong
CCNU: Wenjing Deng (also with CERN)
EPFL: E. Charbon, F.Piro (also with CERN)
SLAC & Stanford U: M.D. Vassilev, C. Vernieri

CERN:, G. Aglieri Rinella, W. Bialas, G. Borghello, R. Ballabriga, J. Braach, E. Buschmann, M. Campbell, F. Carnesecchi, L. Cecconi, D. Dannheim, K. Dort, Joao de Melo, W. Deng (also with CCNU), A. Di Mauro, A. Dorda Martin, P. Dorosz, J. Hasenbichler (also with TU Vienna), H. Hillemans, A. Junique, I. Kremastiotis, A. Kluge, G. Kucharska, T. Kugathasan, P. Leitao, M. Mager, P. Martinengo, M. Munker, L. Musa, F. Piro, K. Rebane, F. Reidt, I. Sanna (also with TU Munich), W. Snoeys, P. Svihra, M. Suljic, G. Termo, J. B. Van Beelen

Foundry support: TPSCo: M. Suzuki**, Tower Semiconductor:** A.Fenigstein, and **Etesian Semiconductor:** A. Haim, E. Toledano

CMOS Monolithic Active Pixel Sensors revolutionized the imaging world

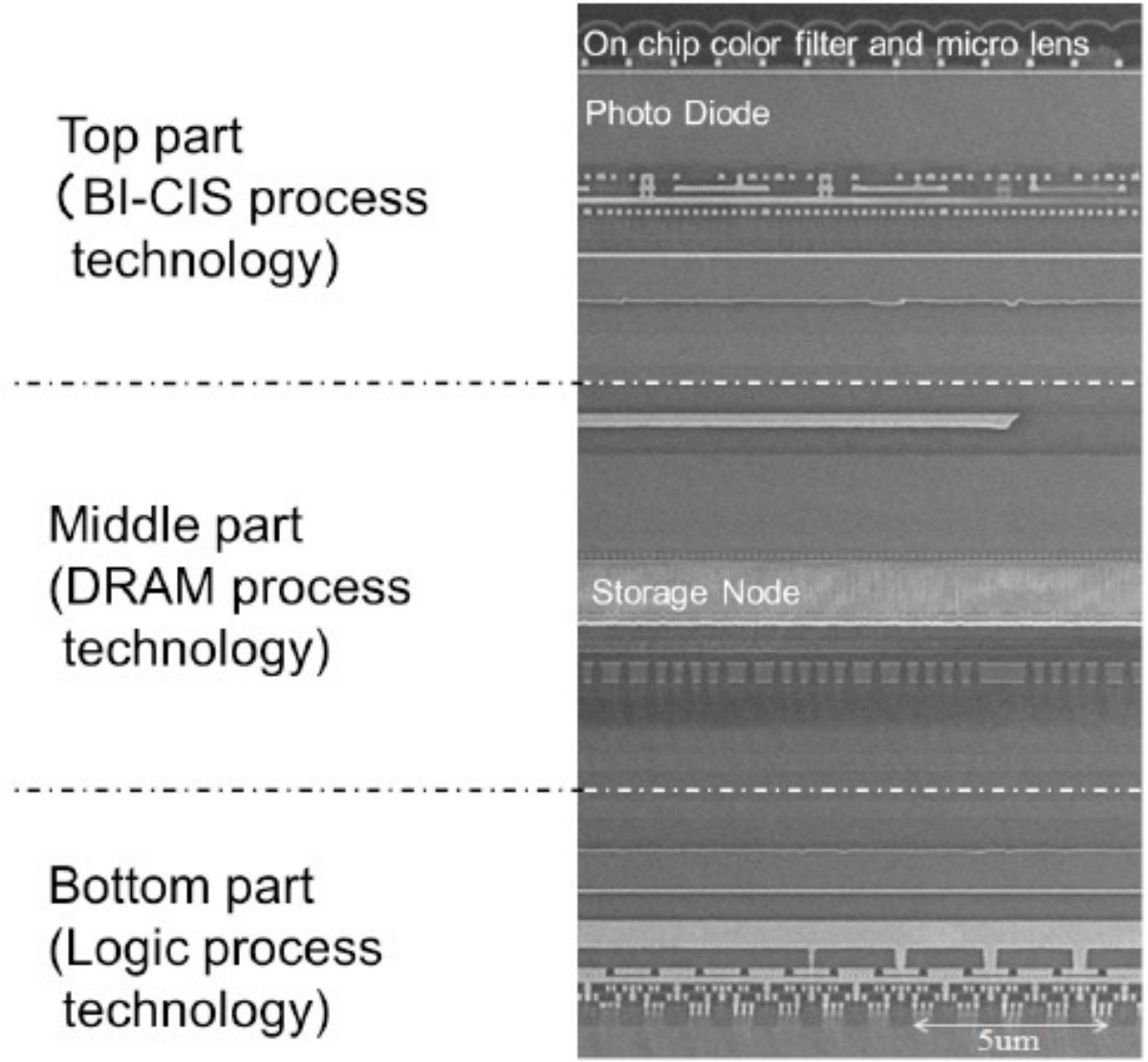
reaching:

- less than 1 e^- noise
- > 40 Mpixels
- Wafer scale integration
- Wafer stacking (now offered by foundries)
- …

Silicon has become the standard in tracking applications both for sensor and readout

… and now CMOS MAPS make their way in High Energy Physics !

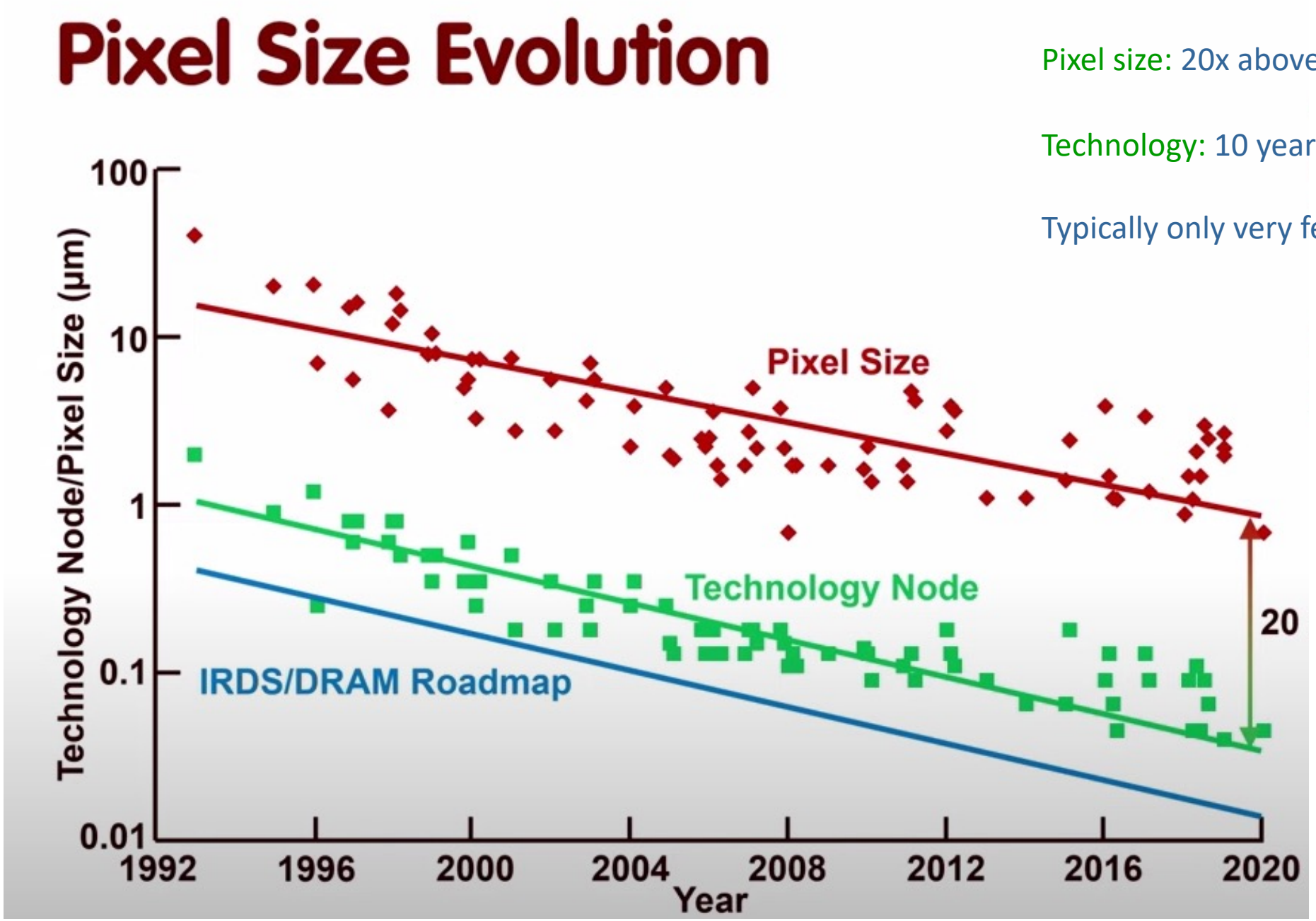
Hybrid still in majority in presently installed systems



Sony, ISSCC 2017

New technologies (TSV's, microbumps, wafer stacking…) make the distinction between hybrid and monolithic more vague.

Evolution of pixel size and technology node for visible:



Pixel size: 20x above technology feature size

Technology: 10 years behind DRAM technology

Typically only very few (1-4) transistors per pixel

Many more transistors per pixel for HEP !

Albert Theuwissen, ISSCC 2021

Requirements for High Energy Physics

	Dose (Mgy)	Fluence (10^{16} 1MeVn_{eq}/cm^2)
ALICE ITS	**0.01**	**10^{-3}**
LHC	**1**	**0.1…0.3**
HL-LHC 3ab^{-1}	**5**	**1.5**
FCC	**10-350**	**3-100**

Radiation tolerance

- CMOS circuit typically more sensitive to ionizing radiation
- Sensor to non-ionizing radiation (displacement damage)

Single particle hits instead of continuously collected signal in visible imaging

- Sparse images < or << 1% pixels hit per event
- Near 100% efficiency, full CMOS in-pixel needed, often circuit (much) more complex

Position resolution (~µm)

Low power consumption is the key for low mass

- Now tens of mW/cm^2 for silicon trackers and hundreds of mW/cm^2 for pixels
- Despite enhanced detector functionality for upgrades, material penalty limits power consumption increase

More bandwidth

Time resolution

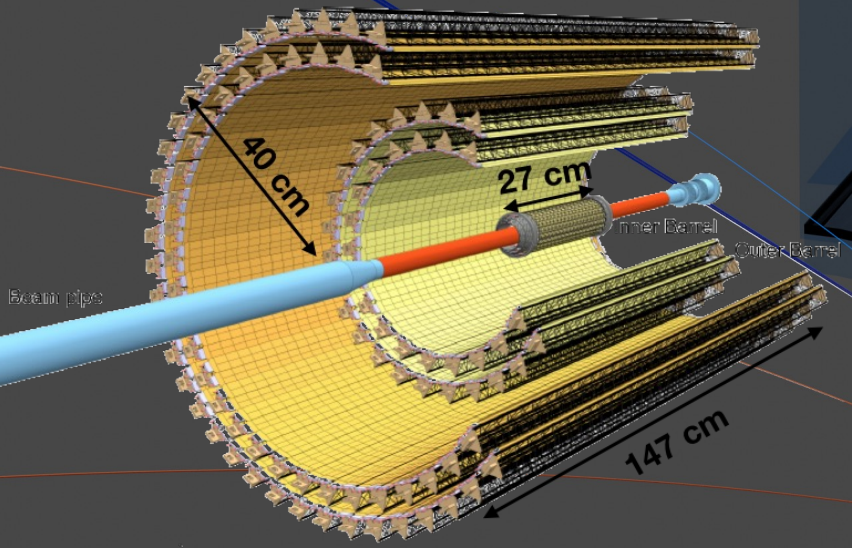
- Time stamping ~ 25 ns or even lower, ... much lower (10s of ps)

Larger and larger areas

- ALICE ITS2 10 m^2, discussions on hundreds to even thousands square m^2,
- Interest for versatile sensors programmable for different applications (P. Allport CERN EP seminar 2020)

ALICE Inner Tracker System 2 (ITS2) taking data

10 m^2 covered with ALPIDE CMOS sensors in TJ 180 nm



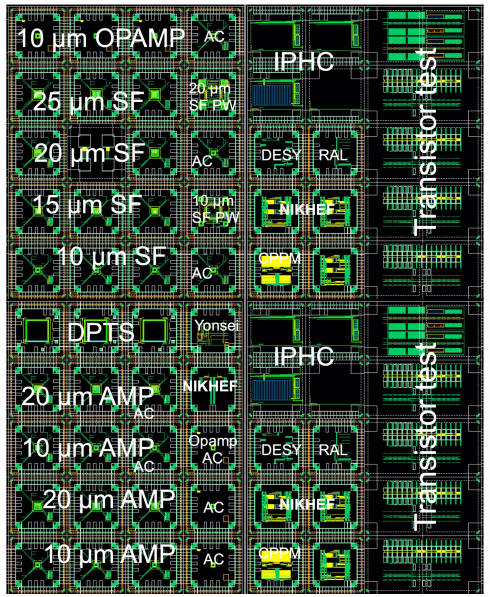
ITS 3 upgrade: replace 3 inner layers with wafer scale stitched sensors[1]

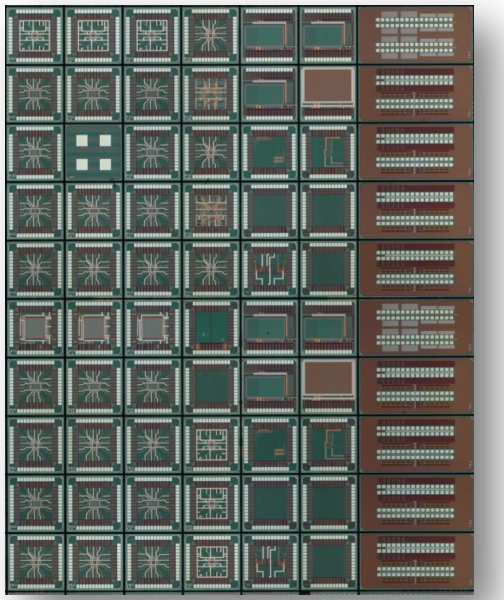
(1) https://indico.cern.ch/event/1071914, *ALICE ITS3 – a next generation vertex detector based on bent, wafer-scale CMOS* sensors, Magnus Mager (CERN)
(1) https://cds.cern.ch/record/2703140/files/LHCC-I-034.pdf - *Letter of Intent for an ALICE ITS Upgrade in LS3*

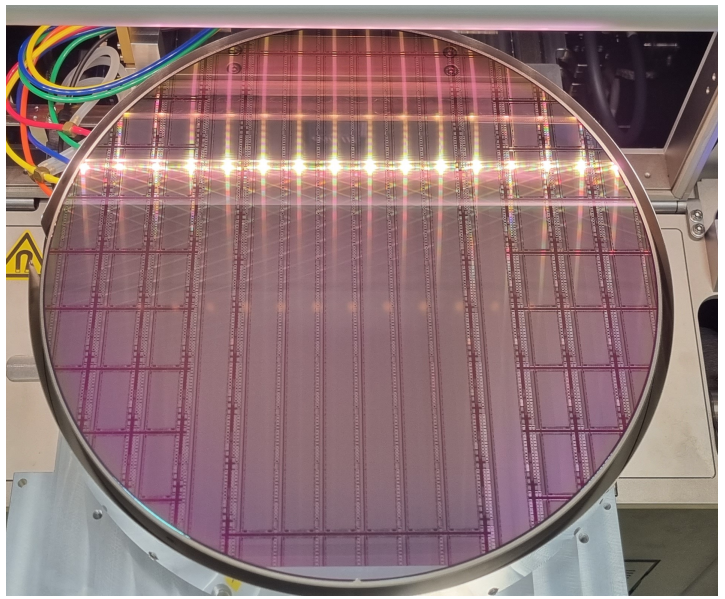
ALICE

EP RD WP1.2 on monolithic CMOS sensors

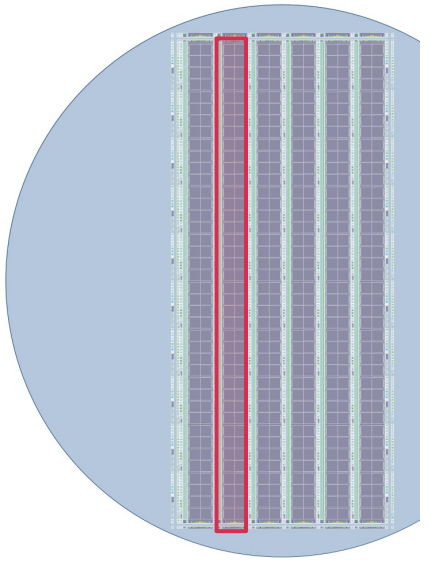
- CERN EP R&D (WP1.2 Monolithic Pixel Detectors) investigating sub 100 nm technologies for HEP
- Many contributors, strong synergy with ALICE ITS3 upgrade, very large measurement team (40-50 people)
- First technology selected is the TPSCo 65 nm ISC. Two submissions so far:







26cm long single silicon object



MLR1 (December 2020): 1.5 x 1.5 mm^2 test chips

Learn about the technology, characterize pixels, transistors and building blocks

ER1 (December 2022):

Prove we can design wafer-scale stitched sensors

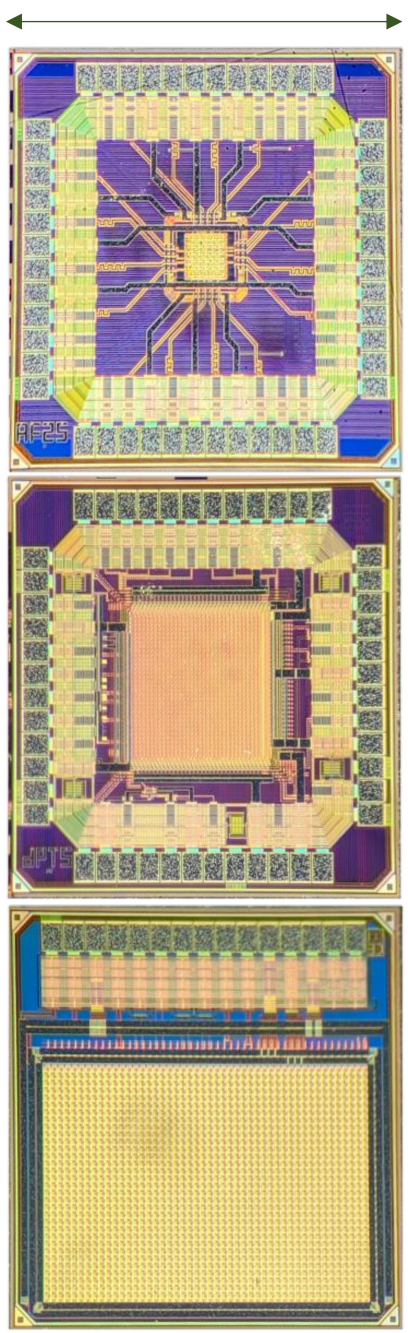
Profited significantly from the 10 years of experience in the TowerJazz 180 nm CMOS technology.

Similar process modifications as in 180 nm, but more needed in 65 nm doi.org/10.22323/1.420.0001

Summary of WP1.2: https://indico.cern.ch/event/1233482/contributions/5264293/attachments/2596131/4482445/EP_RandD_Days_WP1.2_2023_02_20.pdf

MLR1 Chips and Features

- Transistor Test Structures
- Building blocks
  - Bandgap, DACs, Temperature sensor, VCO, drivers …
  - NIKHEF, IPHC, STFC, DESY, CPPM
- Pixel Prototypes APTS, DPTS, CE65
  - Other pixel prototypes from DESY, Yonsei
- Process Optimisation
  - Increase margins on sensing performance



APTS

4x4 pixel matrix
10, 15, 20, 25 µm pitches
Pixel variants
Direct analogue readout

DPTS

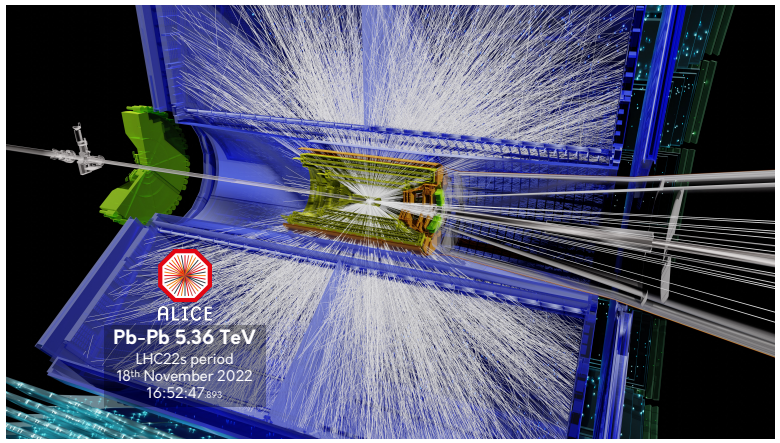
32 × 32 pixels
15 µm pitch
Asynchronous digital readout
ToT information

CE65

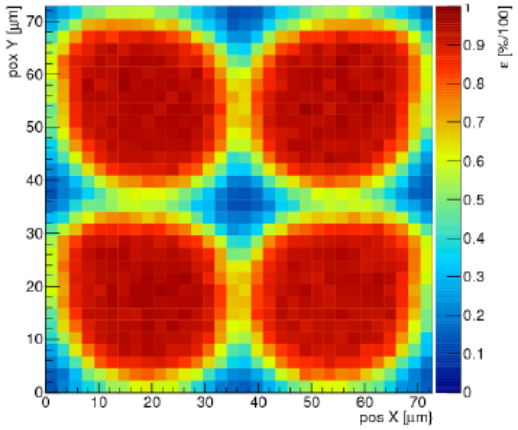
64 × 32 pixels
15 µm pitch
Rolling shutter analog readout
3 pixel architectures

Pixel optimization in 180 nm (started in 2012)

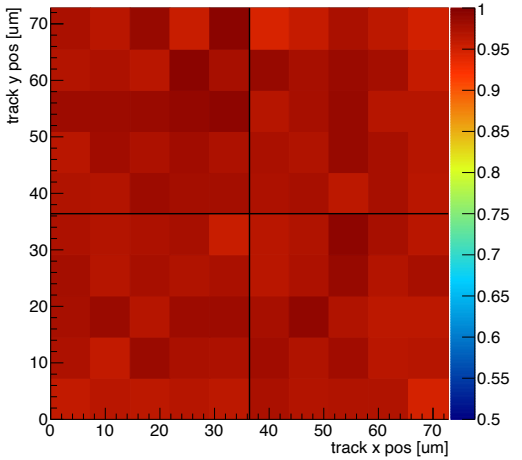
efficiency loss at ~ 10^{15} 1 MeV n_{eq}/cm^2



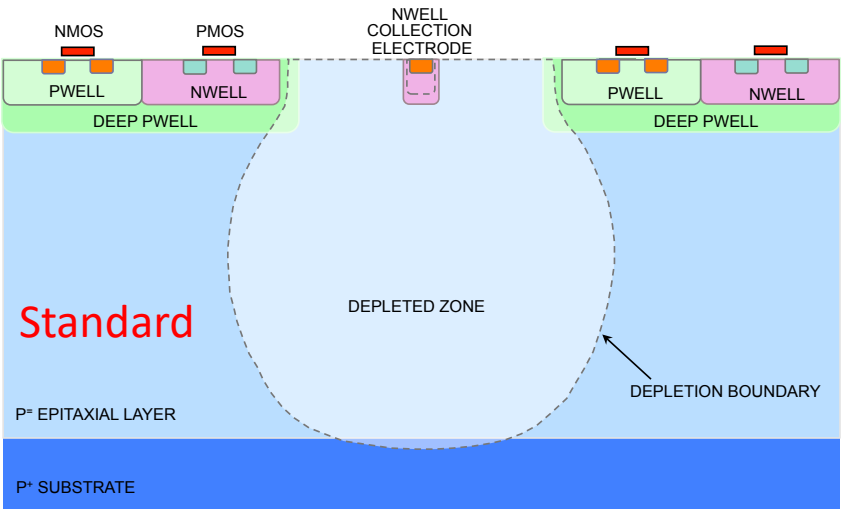
ALPIDE and ITS2 in ALICE (10 m^2)

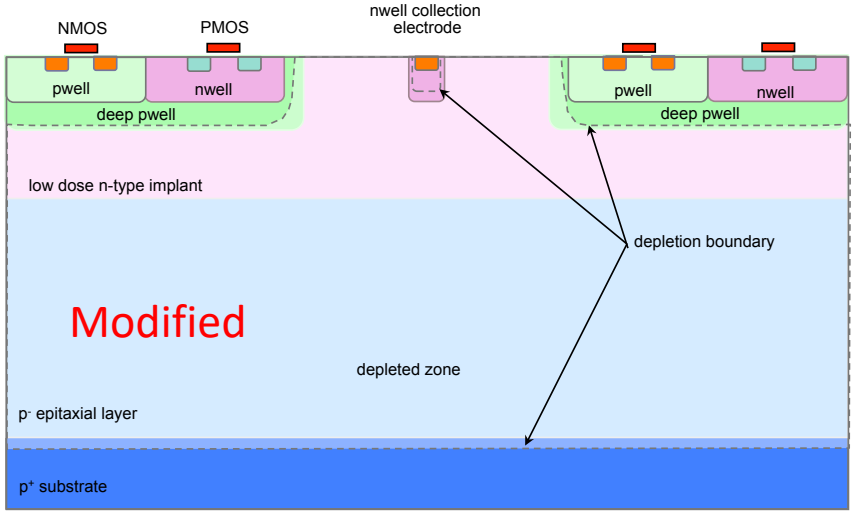


E. Schioppa et al, VCI 2019

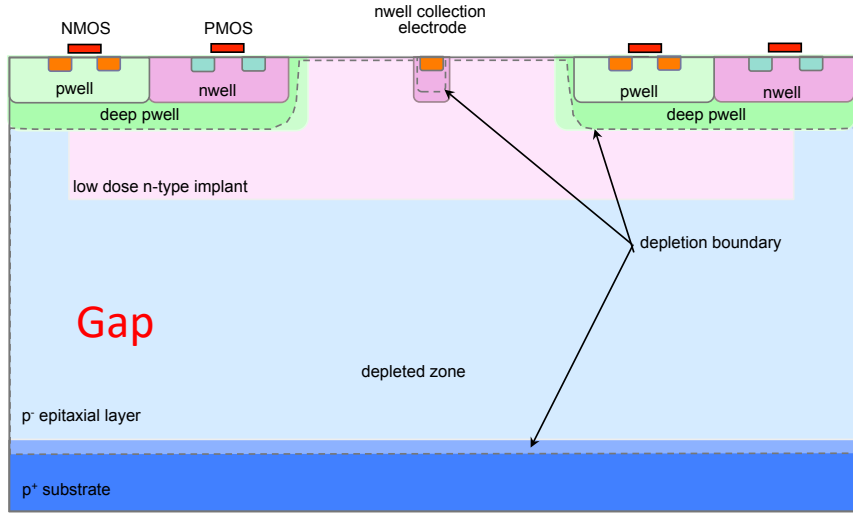


H. Pernegger et al., Hiroshima 2019, M. Dyndal *et al* 2020 *JINST* **15** P0200





https://doi.org/10.1016/j.nima.2017.07.046 (180nm)

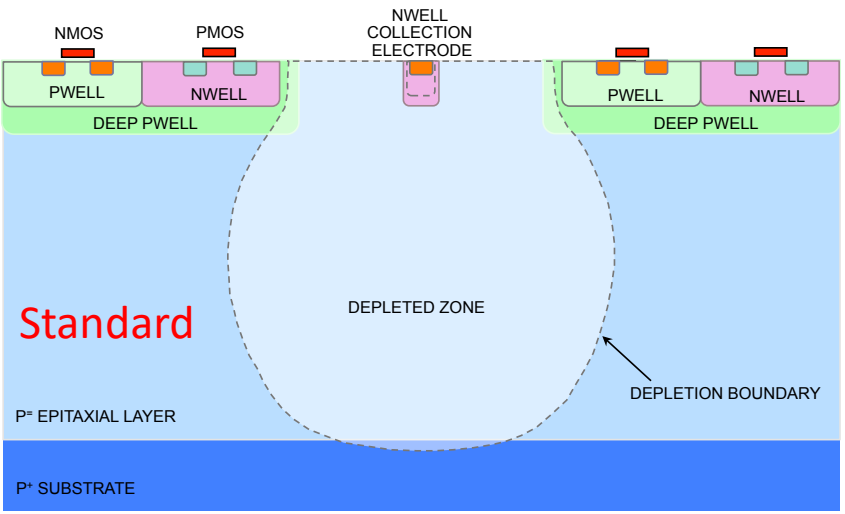


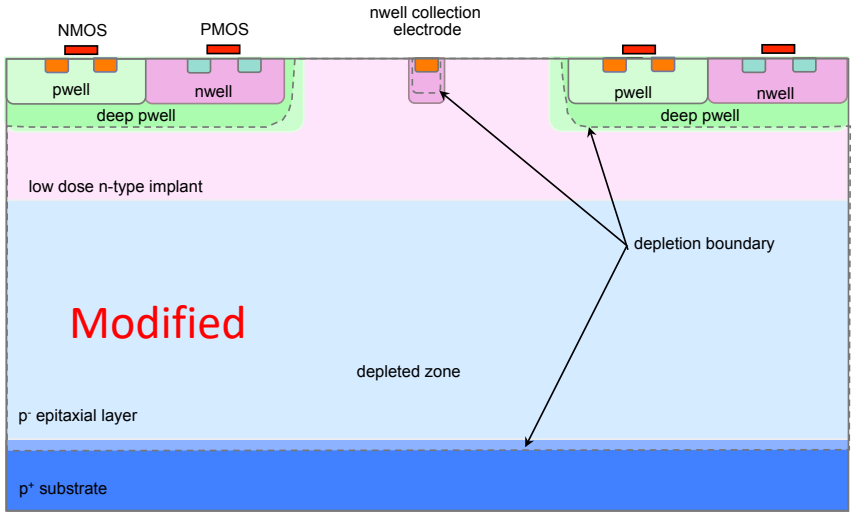
https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013 (180nm)

Charge collection speed

Charge sharing

Process optimization: 65 nm very similar





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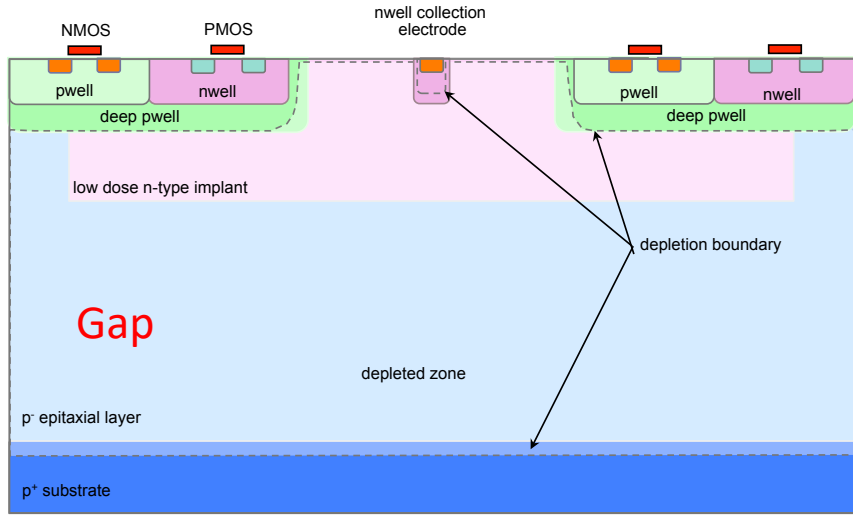


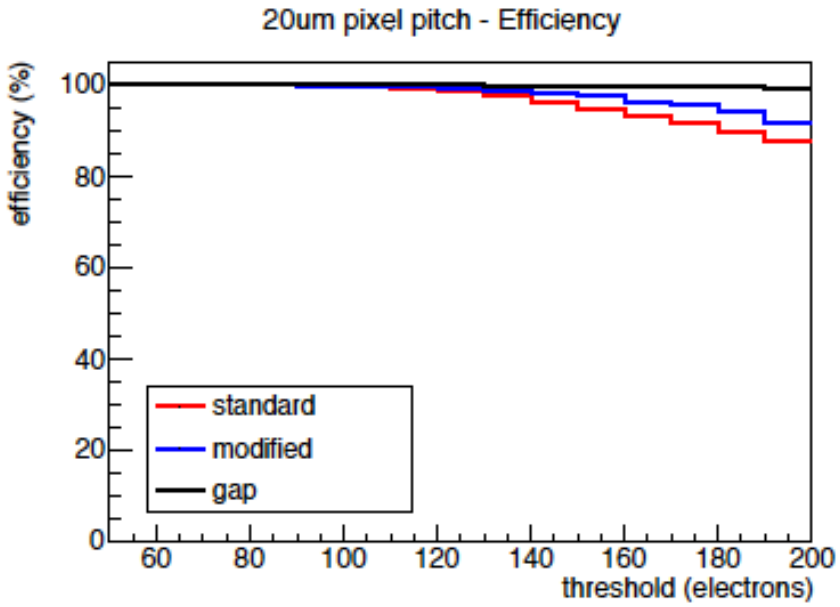
https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013 (180nm)

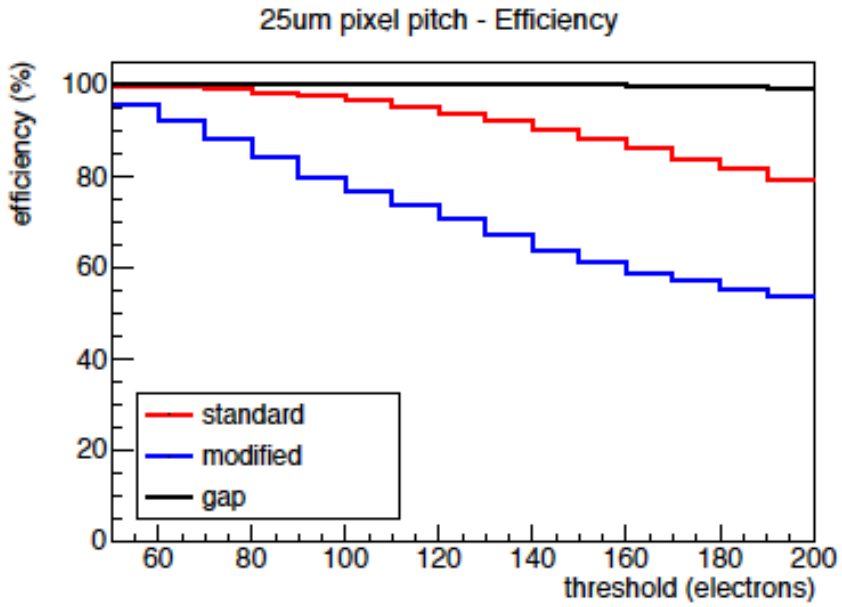
Charge collection speed

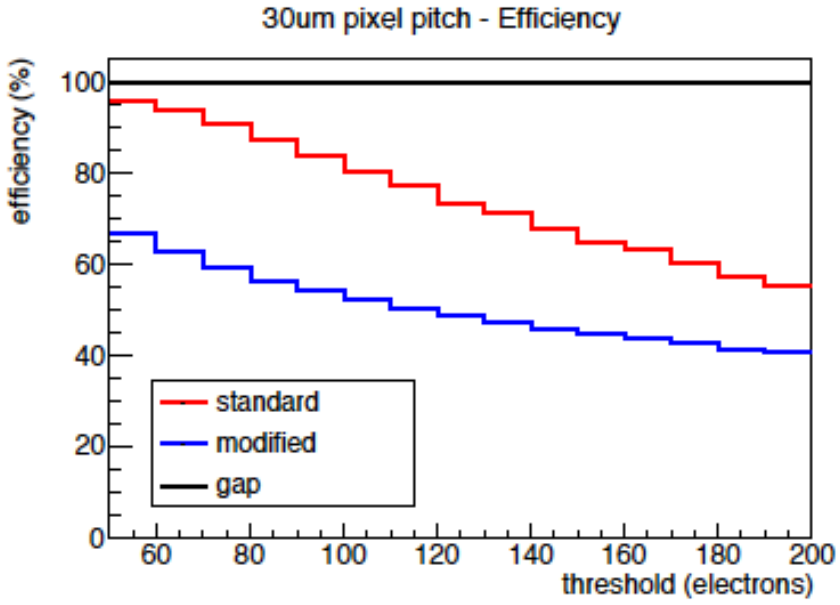
Charge sharing

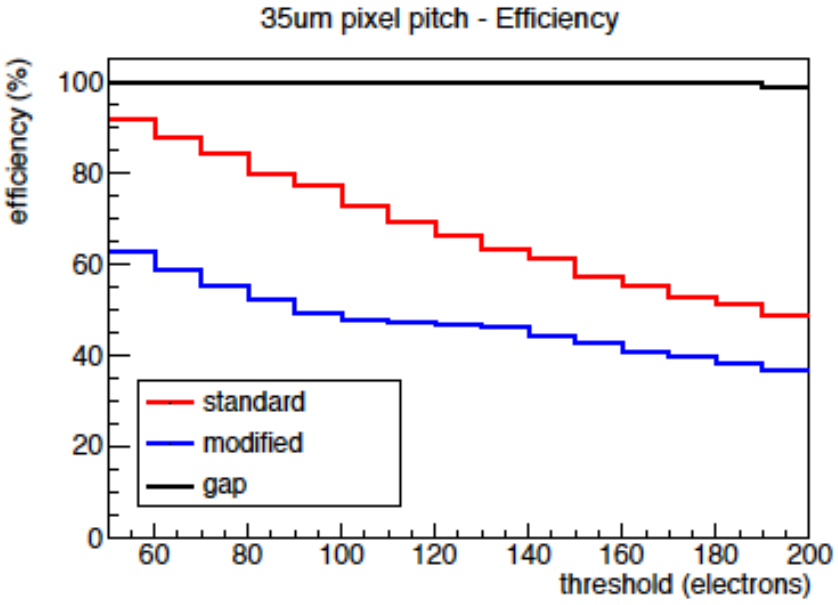
"10th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging" PoS(Pixel2022)001, DOI: https://doi.org/10.22323/1.420.0001

Different pixel flavors at larger pixel pitches









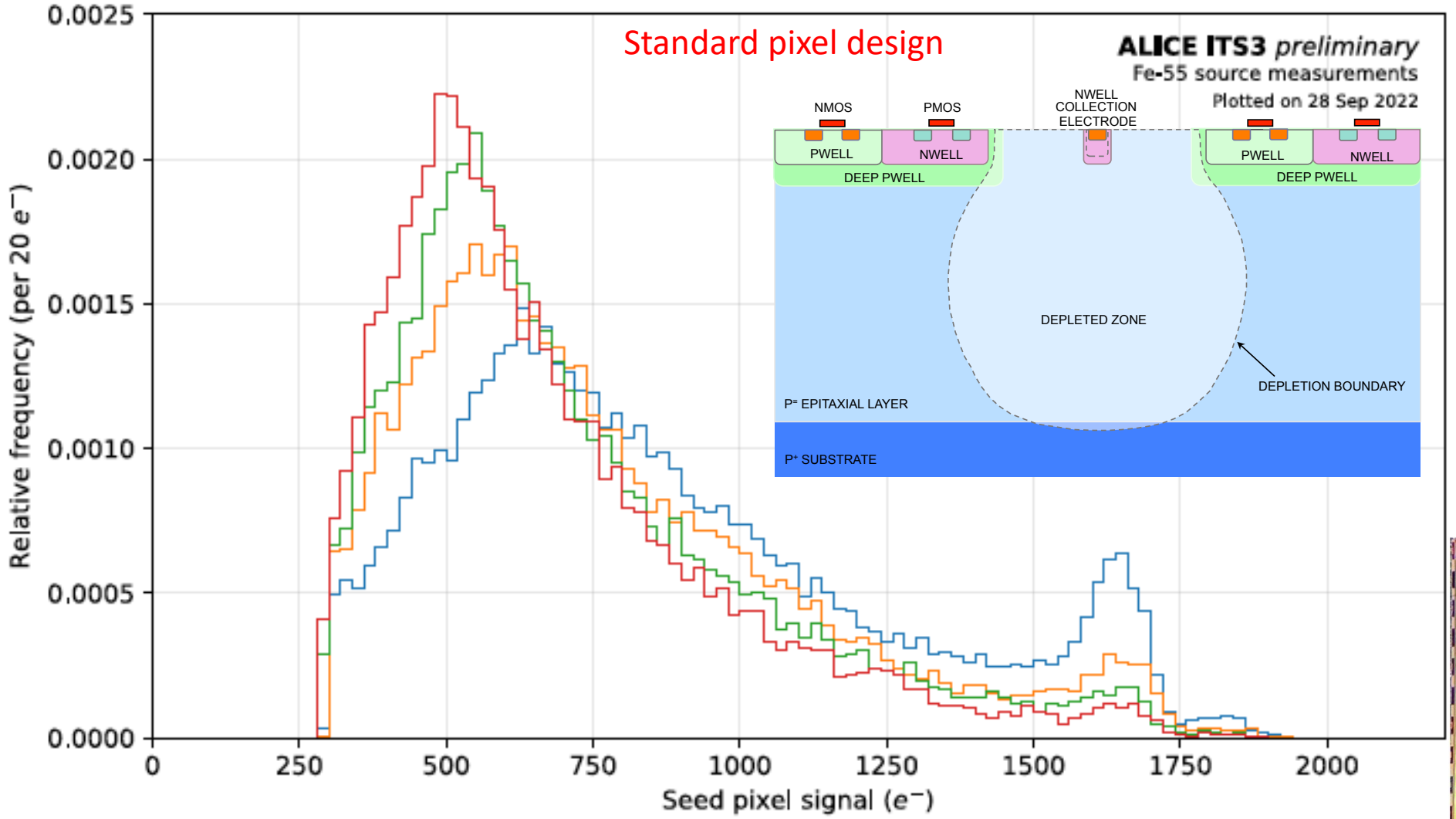
Simulations by J. Hasenbichler for MIPS

Charge sharing reduces the signal in a single pixel and reduces efficiency especially for larger thresholds.

Only the gap concentrates charge sufficiently to remain efficient for large pixel pitches

Pitch dependence for different variants ^{55}Fe

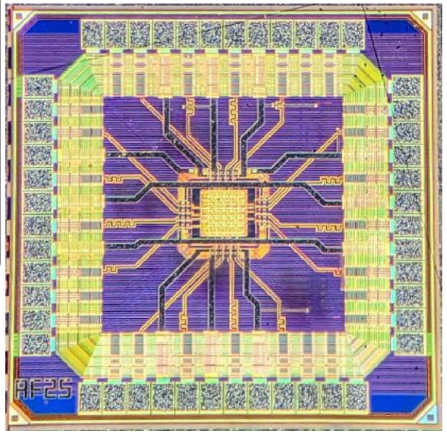
See also: I. Sanna IEEE NSS 2022



APTS SF
type: standard
split: 4
$V_{sub} = V_{pwell} = -1.2$ V
$I_{reset} = 100$ pA
$I_{biasn} = 5$ µA
$I_{biasp} = 0.5$ µA
$I_{bias4} = 150$ µA
$I_{bias3} = 200$ µA
$V_{reset} = 500$ mV

pitch = 10 µm
pitch = 15 µm
pitch = 20 µm
pitch = 25 µm

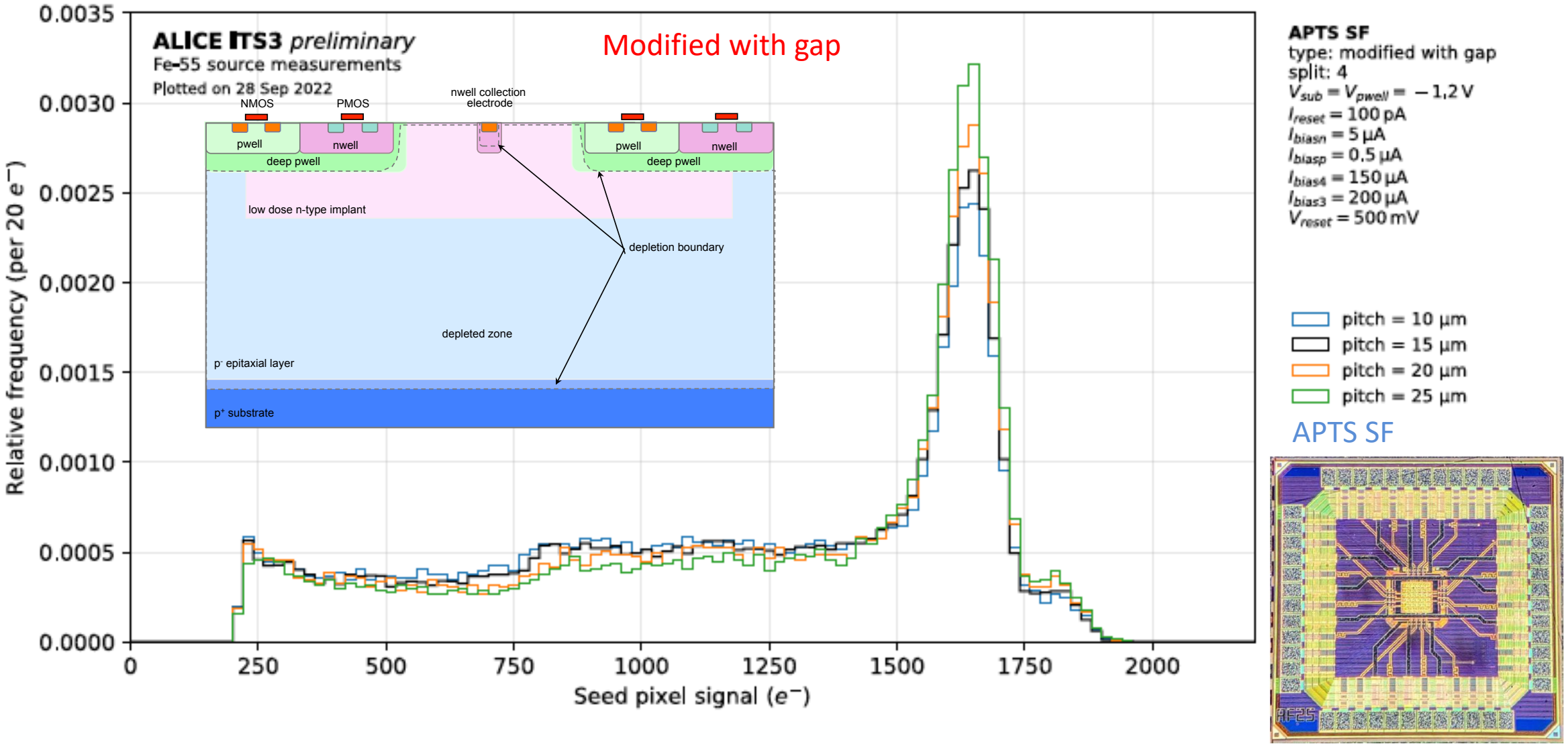
APTS SF



Pitch dependence for different variants ^{55}Fe

See also: I. Sanna IEEE NSS 2022

Remarkable result !



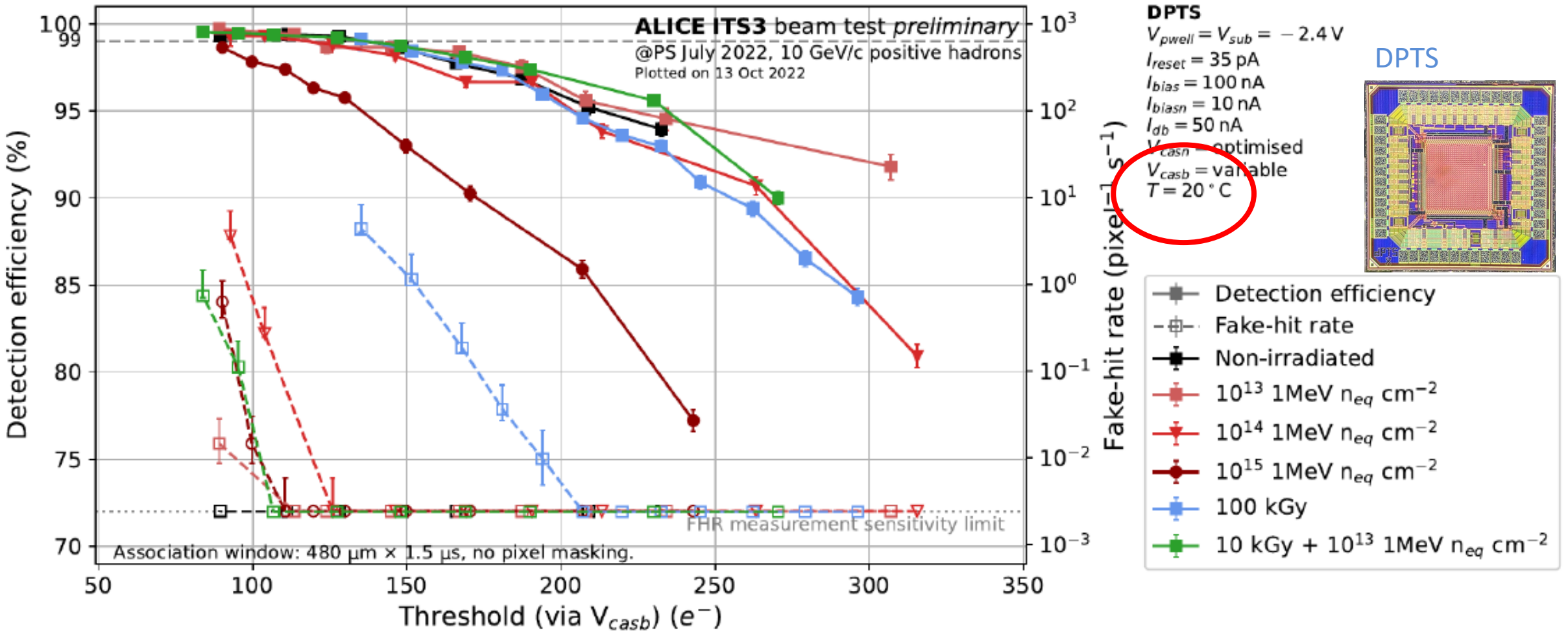
APTS SF
type: modified with gap
split: 4
$V_{sub} = V_{pwell} = -1.2\,V$
$I_{reset} = 100\,pA$
$I_{biasn} = 5\,\mu A$
$I_{biasp} = 0.5\,\mu A$
$I_{bias4} = 150\,\mu A$
$I_{bias3} = 200\,\mu A$
$V_{reset} = 500\,mV$

pitch = 10 µm
pitch = 15 µm
pitch = 20 µm
pitch = 25 µm

APTS SF

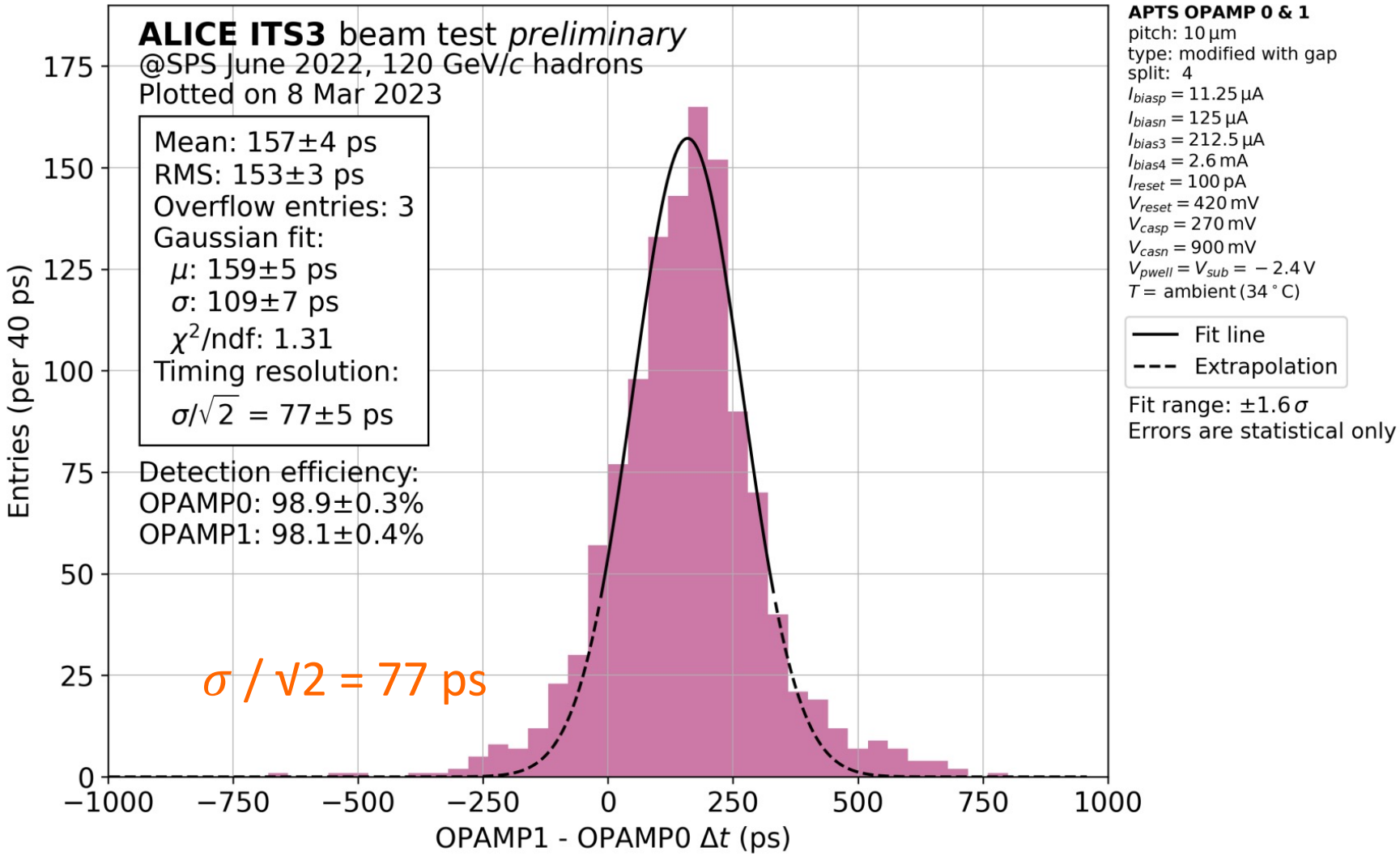
~ 99 % efficiency at 10^{15} n_{eq}/cm^2 … at room temperature

doi: 10.1016/j.nima.2023.168589

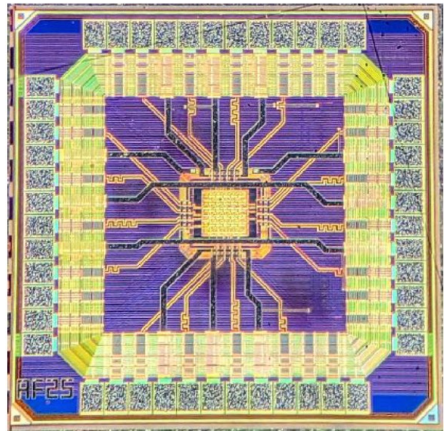


- Fully efficient sensor, analog front end, digital readout chain in 15 x 15 µm² pixel (DPTS) including sensor optimization
- Transistor total ionizing dose tolerance doi: 10.1088/1748-0221/18/02/C02036 and SEU in line with other 65 nm technologies
- KEY ACHIEVEMENT: 65nm ISC qualified for HEP, many features not yet explored (wafer stacking, special imaging devices…)

Sensor timing



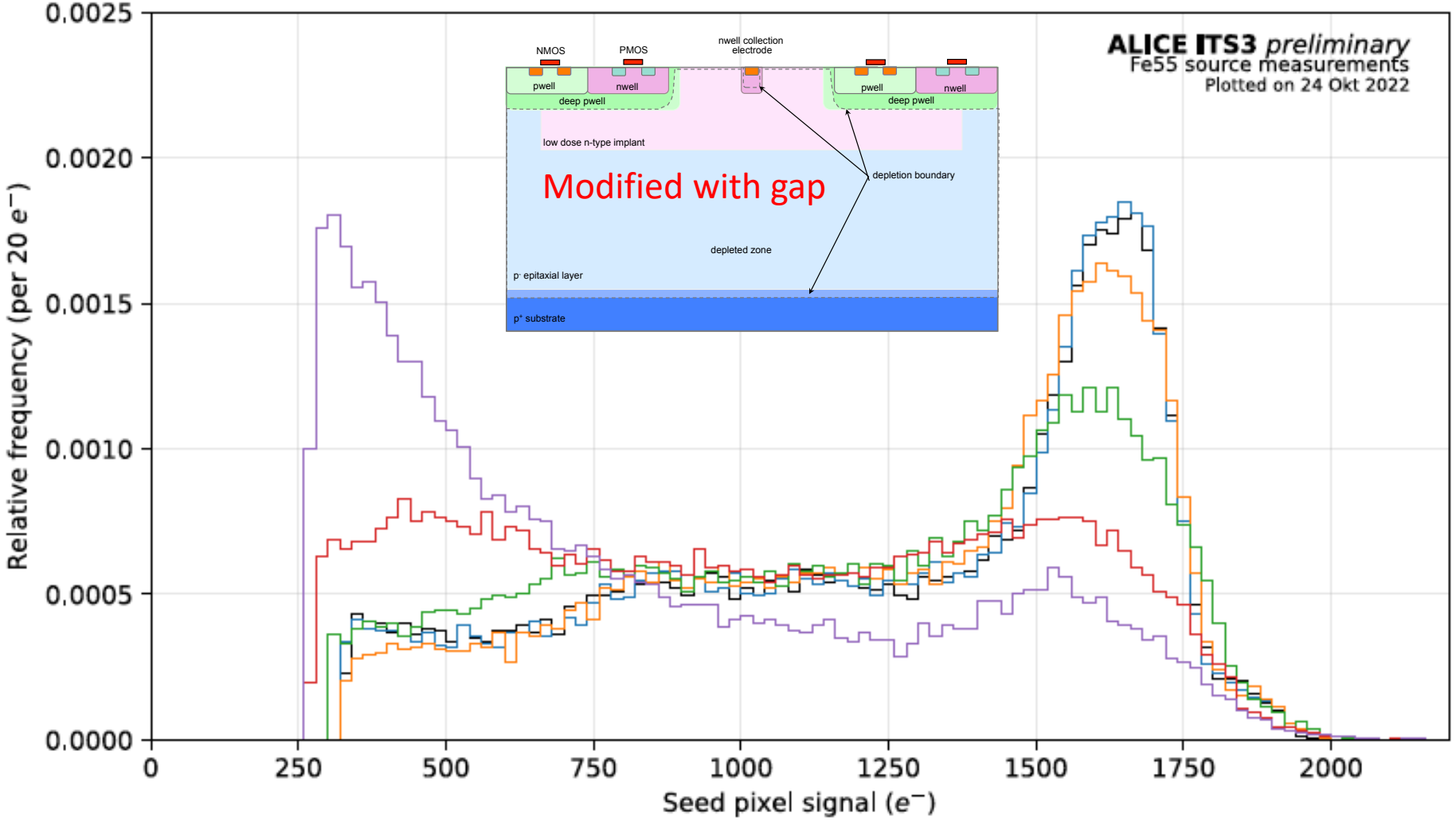
APTS OPAMP



Bong-Hwi, U. Savino et al. ULITIMA 2023

(180nm FASTPIX about 100 ps with time walk and cluster size correction, J. Braach et al. doi:10.48550/arXiv.2306.05938)

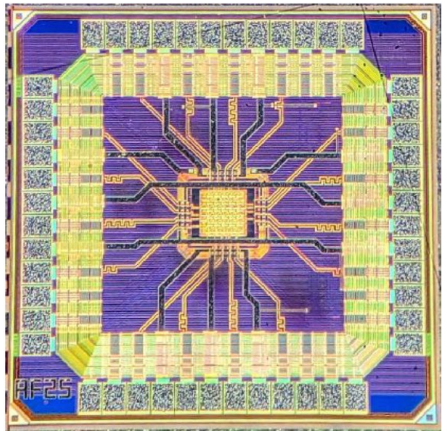
Irradiation results: exploring paths to higher fluences



APTS SF
pitch: 15 µm
type: modified with gap
split: 4
$V_{sub} = V_{pwell} = -1.2\,V$
$I_{reset} = 250\,pA$
$I_{biasn} = 5\,\mu A$
$I_{biasp} = 0{,}5\,\mu A$
$I_{bias4} = 150\,\mu A$
$I_{bias3} = 200\,\mu A$
$V_{reset} = 500\,mV$
temperature = 14 °C

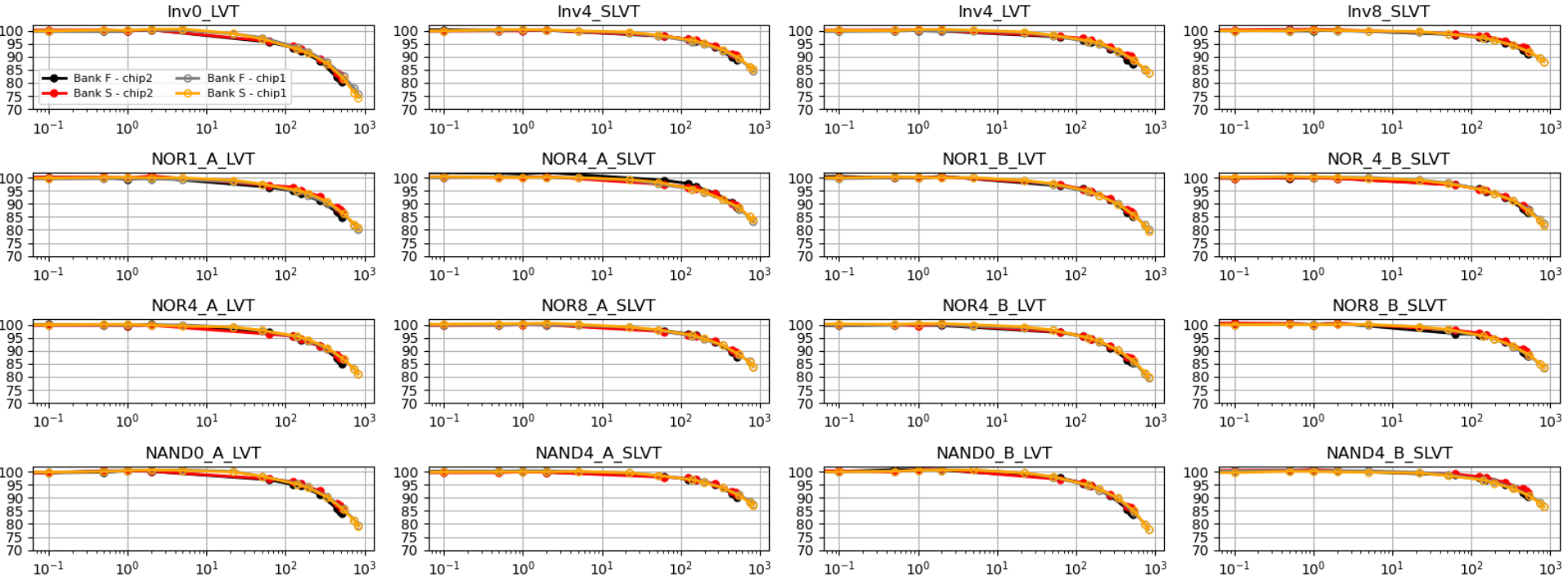
Not irradiated
1e13
1e14
1e15
2e15
1e16

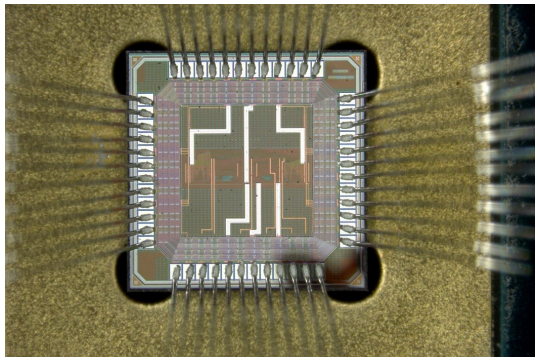
DPTS still efficient at RT



Ringoscillator test chip

CPPM: Pierre Barrillon, Marlon Barbero, Denis Fougeron, Alexandre Habib and Patrick Pangaud (TWEPP 2022)

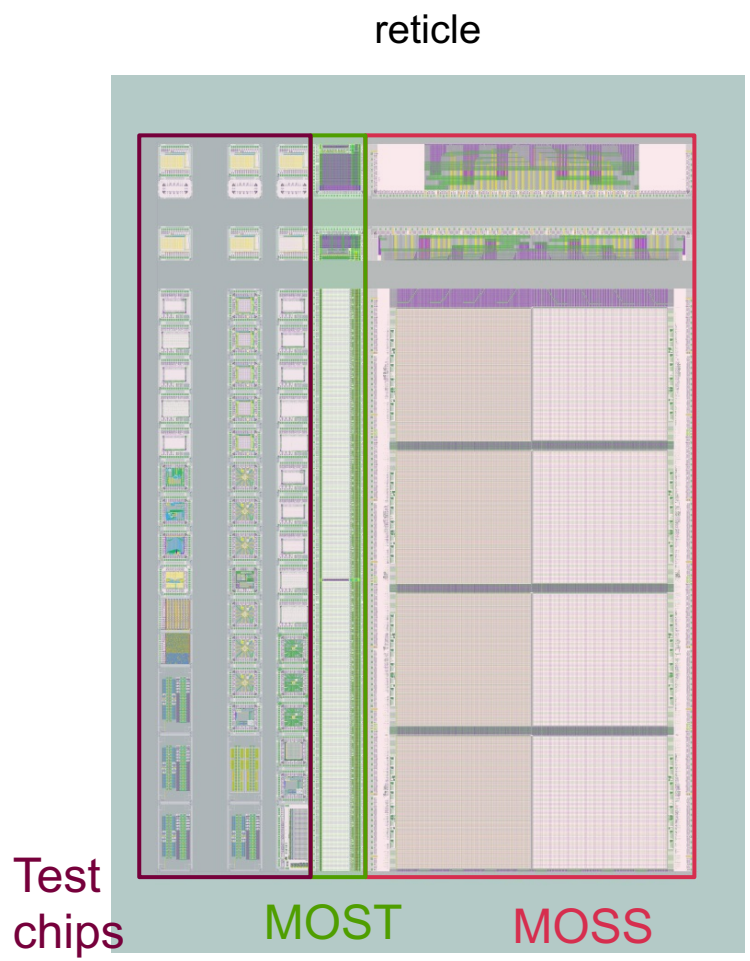


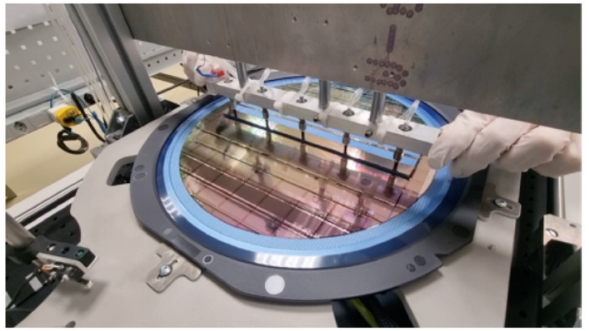


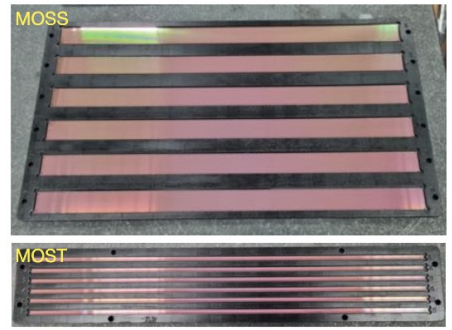
- CPPM contributed to MLR1 with a Ring Oscillator test chip to characterize the standard cells of the TJ 65 nm technology.
- The chip contains 48 ring oscillator based on different standard cells.
- 2 banks of 24 Rows each with the purpose of testing two approaches while irradiating:
  - Functional: the oscillation is enabled
  - Static: the oscillation is disabled
- Oscillation frequency drops by 12-25 % after 830 Mrad. Degradation more pronounced for smaller cells.
- Also several analog designs radiation tolerant up to several 100 Mrad, eg DACs (IPHC) , VCO, bandgap (NIKHEF)…

ER1 submission

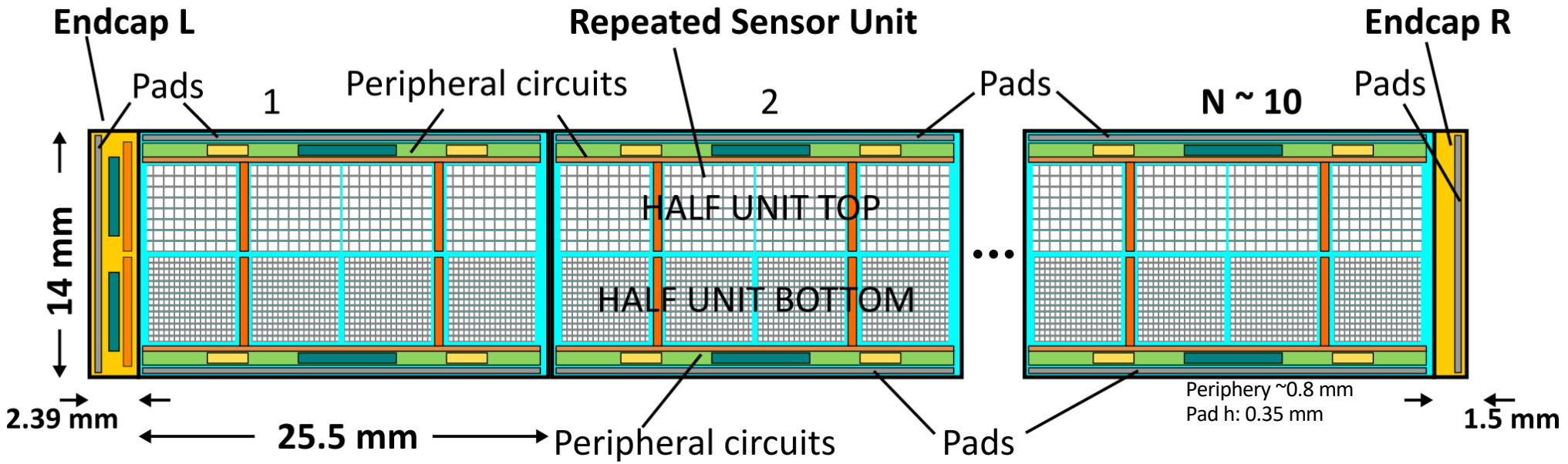
- Two stitched sensor chips, 6 of each per wafer, digital on top design
  - MOSS chip (1.4 x 26 cm)
    - Conservative layout (DFM rules), Alpide-like readout scheme and 1/20 power segmentation
  - MOST chip (0.25 x 26 cm)
    - High local density with high granularity of power gating to mitigate faults, async hit driven readout
- 51 chiplets for prototyping blocks and pixel chips
  - PLL, pixel prototypes, fast serial links, SEU test chips, …
  - IPHC, NIKHEF, STFC, DESY, SLAC, INFN, CERN…
- Learn stitching methodology, wafer assembly and automated signoff (P.. Leitao et al.)
- Learn about yield, design for manufacturing (DFM) and defects masking
- Study power schemes, leakage, spread, noise and speed
  - Practical application: Alice ITS3 upgrade
- Technology and support development
  - New metal stack: new I/Os, PDK, DDK, DRC rules
  - Custom DRC and LVS rule check, custom DFM standard library
  - Legal framework, nda …







MOSS Monolithic Stitched Sensor Prototype



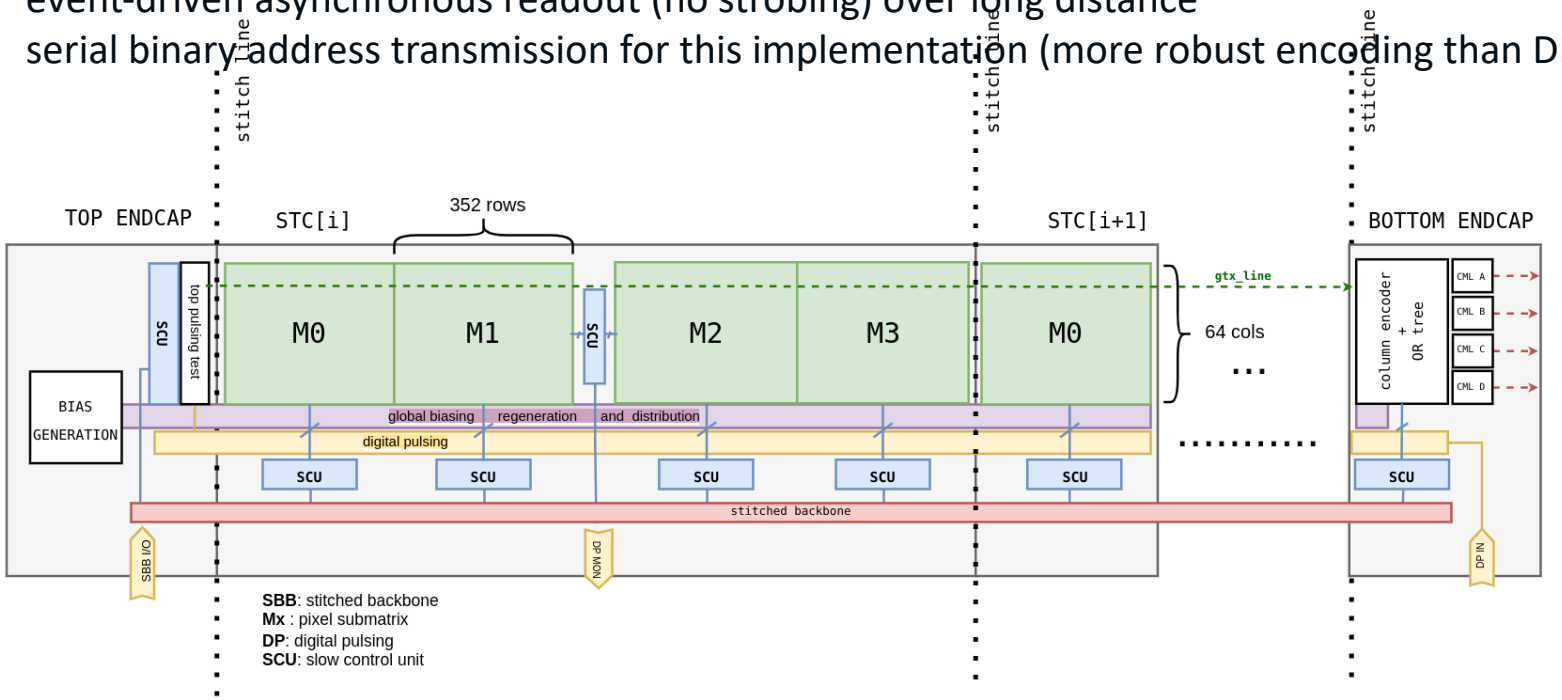
Primary Goals
Learn Stitching technique to make a particle detector
Interconnect power and signals on wafer scale chip
Learn about yield and DFM
Study power, leakage, spread, noise, speed

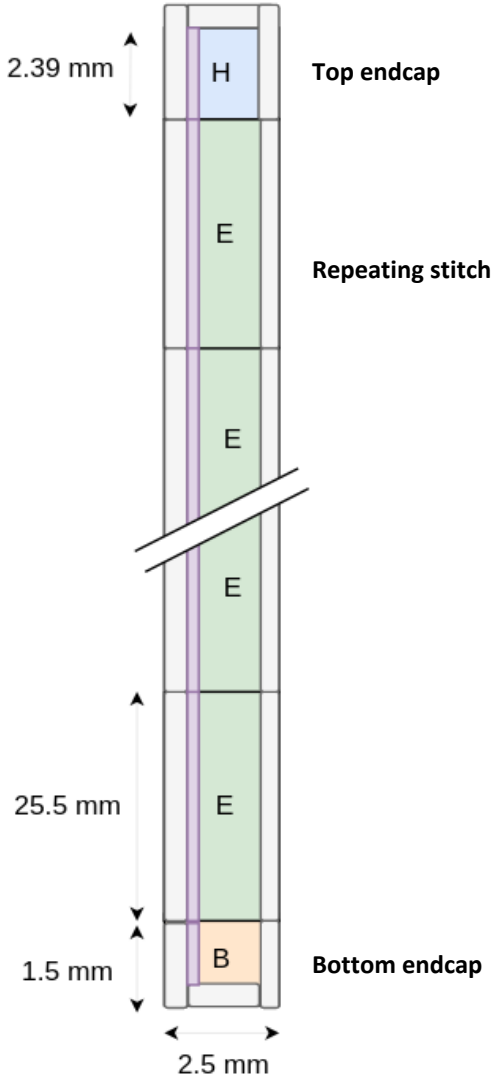
Repeated units abutting on short edges

- Repeated Sensor Unit, Endcap Left, Endcap Right
- Functionally independent
- Stitching used to connect metal traces for **power distribution** and **long range on-chip interconnect busses for control and data readout**

MOST Chip

- Investigate **yield** when local density is preserved
  - Global power domains over full chip (Digital/Analog)
  - Higher granularity in power gating in case of a defect of
    - analog (rows of 4 pixels)
    - digital (half columns)
  - PWELL tied to ground
    - reverse sensor biasing achieved by higher power supply
- Immediate transfer of hit data to the periphery (bottom endcap, 4 CML outputs)
  - event-driven asynchronous readout (no strobing) over long distance
  - serial binary address transmission for this implementation (more robust encoding than DPTS)





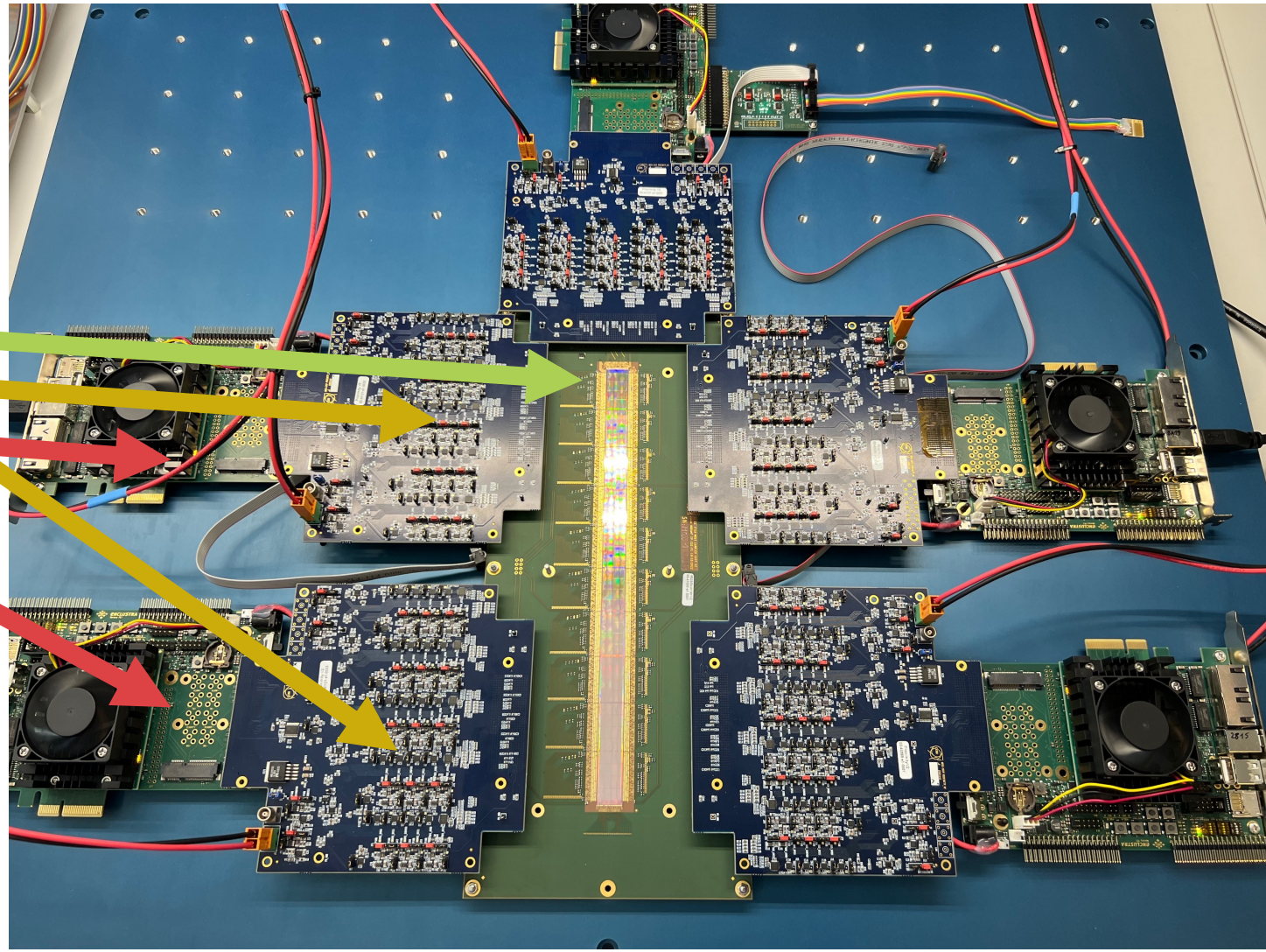
ER1 (MOSS) test system

Gregor Eberwein, Valerio Sarritzu, Antoine Junique, Magnus Mager …

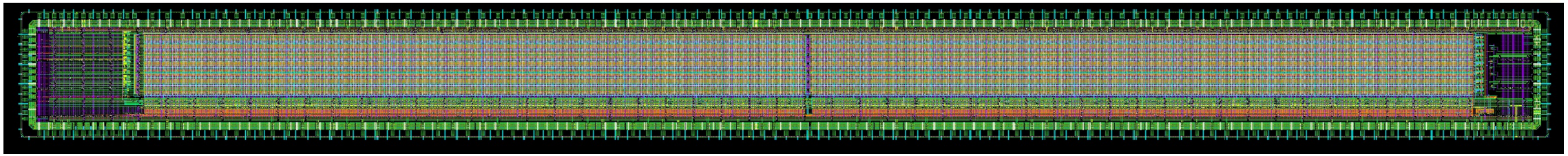
Based on:

- Carrier card (passive)
- 5x proximity card (active, custom made)
- 5x FPGA card (commercial)

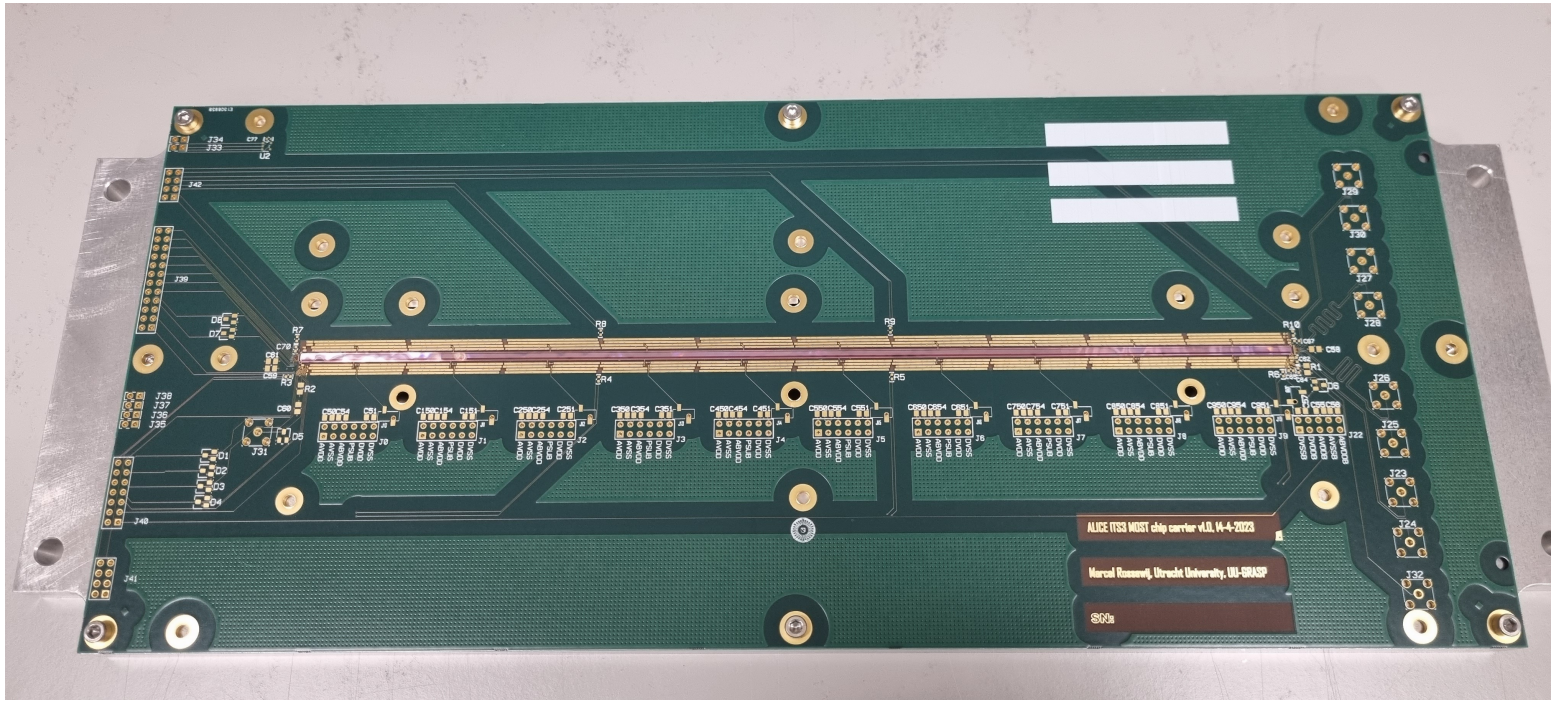
- First successful contact in May
- First operation in beam in August
  (D. Colella TIPP2023)



MOST



Single stitch assembly: (1 middle stitch + endcaps)



First mounting of (dummy from pad wafer) MOST on test card

SUMMARY and OUTLOOK

After MLR1: 65 nm ISC qualified for HEP:

- Building knowledge about this technology for general interest
- Results fully in line with ECFA roadmap
- Very significant effort with **synergy with the ALICE ITS3 upgrade project without which this progress could not have been made.**

ER1: exploration of stitched sensors

- Back from foundry, first results becoming available but significant testing effort ahead

ER2: focused on large stitched sensor MOSS2 for ITS3 upgrade

- MOSS2 will need to satisfy ITS3 requirements
- Less chiplets
- Tapeout spring 2024

MLR2…4: Organizing access for wider HEP community and continuing R&D for experiments (ALICE 3, ….)

- See next page

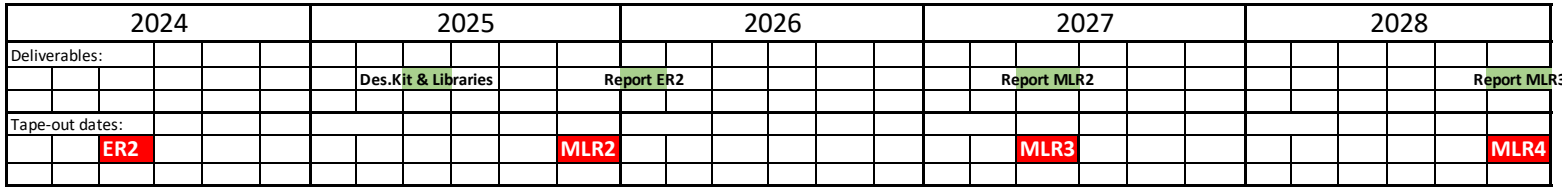
SUMMARY and OUTLOOK

Organize access for HEP community, and continue R&D, coordinate and streamline efforts in the R&D,

also in testing (!), in synergy with the experiments (ALICE3, …) and other R&D projects

As part of CERN EP R&D WP1.2 on monolithic sensors and DRD7. 6 on complex imaging ASICs and technologies, aligned with ECFA roadmap

- Set up joint access for TPSCo 65 nm technology (and possibly others like TJ 180 nm, Lfoundry supported by other institutes, …)
  - Engineering runs MLR2-4 with small chiplets, reticle scale and wafer scale stitched sensors on single wafer
  - Common framework with frame contract, PDK, libraries, …
  - IP blocks (standard pixels, pad rings, ADCs …)
- Shared access to 3 D technologies
- Common QA/ASIC development framework
  - Designer's fora
  - Standardized test setups and readout, MASSIVE testing effort



- DRD7 workshop September 25-26th: https://indico.cern.ch/event/1318635/
- See also last general WP1.2 general reporting meeting: https://indico.cern.ch/event/1280150/

THANK YOU TO ALL CONTRIBUTING PEOPLE, GROUPS AND INSTITUTES

and the conference organizers

SPARE

ECFA Detector R&D in Electronics: DRD7. Call for projects

Dear Colleagues

You receive this message because you registered to the ECFA DRD7 interest group.

In view of drafting its Letter of Intent, DRD7 is now calling for projects in electronics, following the priorities established in the ECFA Detector R&D roadmap document.

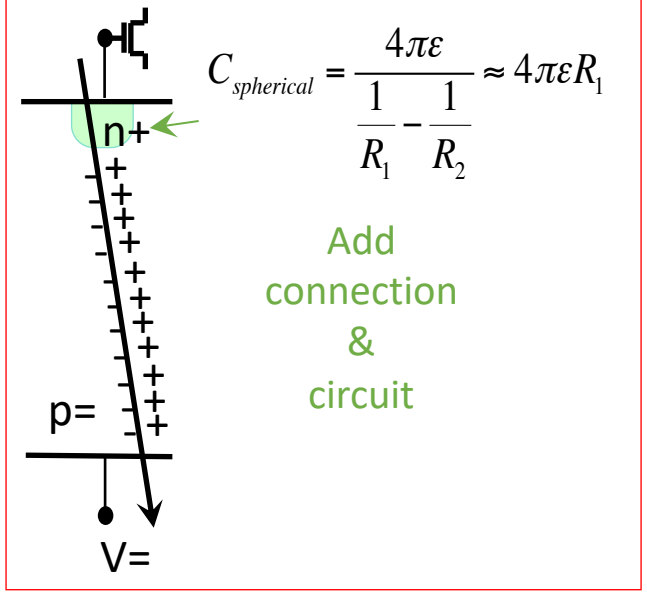
Interested scientists, groups or collaborations are invited to express their interest by contacting the relevant DRD7 WG conveners with their project intentions.
Conveners will collect the community feedback and aggregate it into a portfolio of projects in each WG.
These preliminary project intentions will form the basis of the Letter of Intent, due to be submitted in July 2023.

The two attached documents give all necessary information on the call for projects itself, and on the DRD7 future organization.

Please express your interest before 30 June 2023.

Francois Vasey, on behalf of the steering and technical committees.

The need for sensor optimization to obtain full depletion

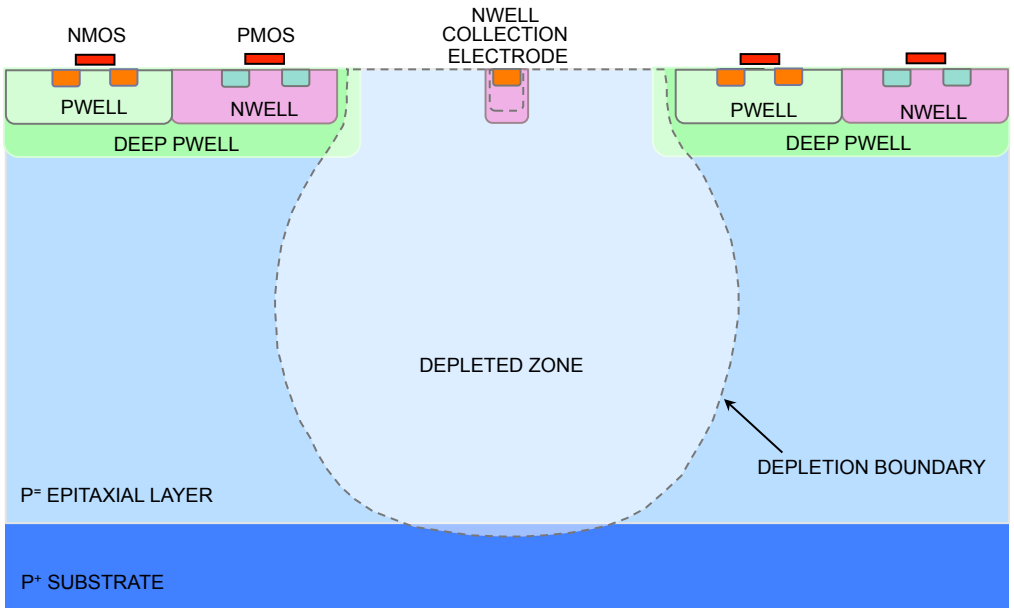


$$C_{spherical} = \frac{4\pi\varepsilon}{\frac{1}{R_1} - \frac{1}{R_2}} \approx 4\pi\varepsilon R_1$$

Add connection & circuit

Planar junction
Depletion width $= \sqrt{\frac{2\varepsilon|V|}{qN_A}}$

Spherical junction
Outer depletion radius $= \sqrt[3]{\frac{2\varepsilon|V|}{qN_A}\frac{3R_1}{2}}$

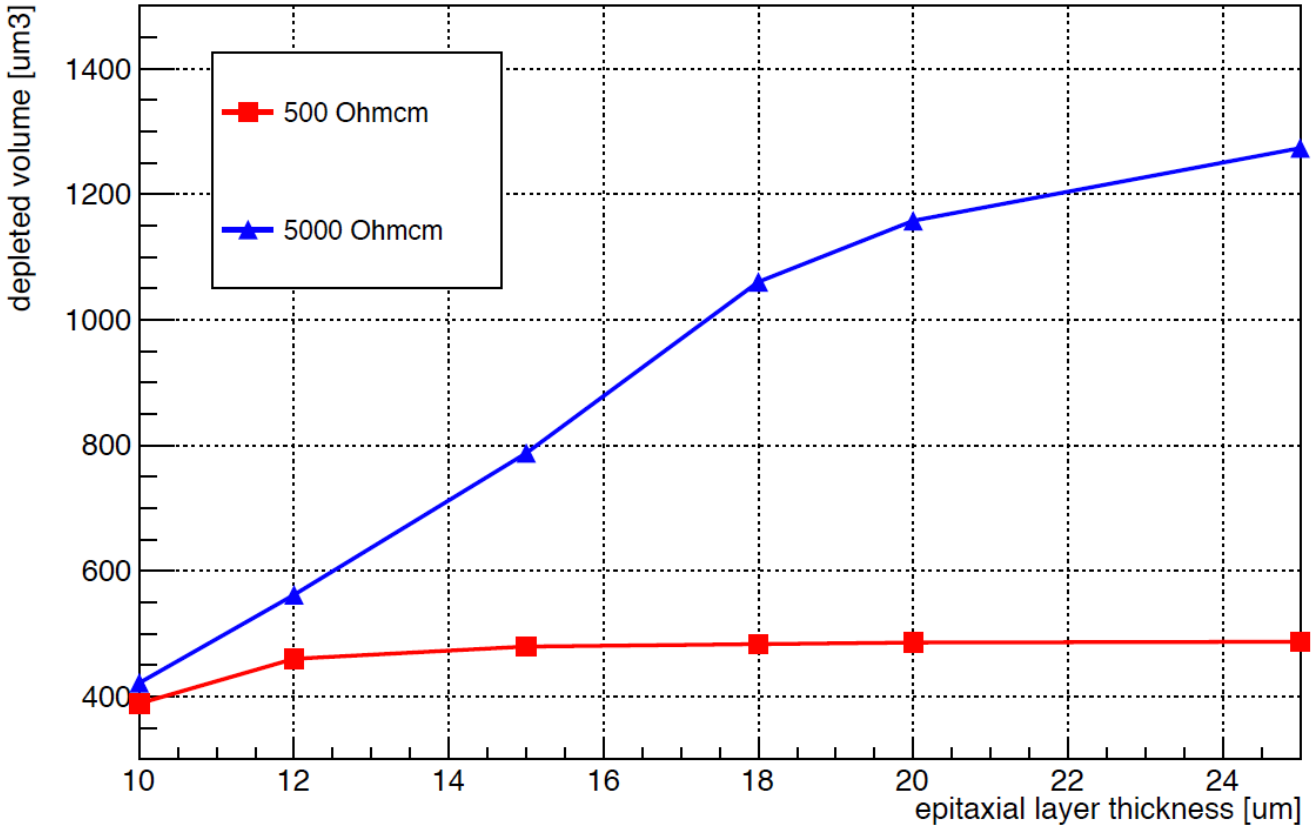


Signal charge is collected from the non-depleted layer, diffusion dominated and prone to trapping after irradiation

Planar vs spherical junction

- Planar junction: depletion thickness proportional to *square root* of reverse bias.
- Spherical junction : depletion thickness proportional only to *cubic root* of reverse bias, inner radius R1 to be kept small for low capacitance
- Deep pwell and substrate limit extension of the depletion layer -> see next slide

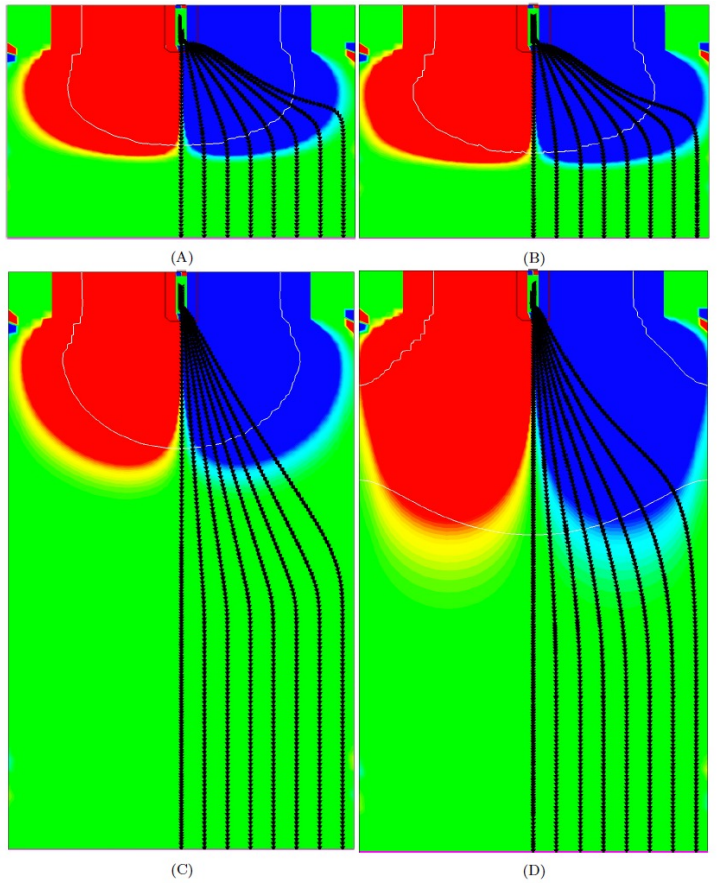
Sensor optimization: influence of the resistivity of the epitaxial layer



Lateral electric field

thin epitaxial layer

thick epitaxial layer



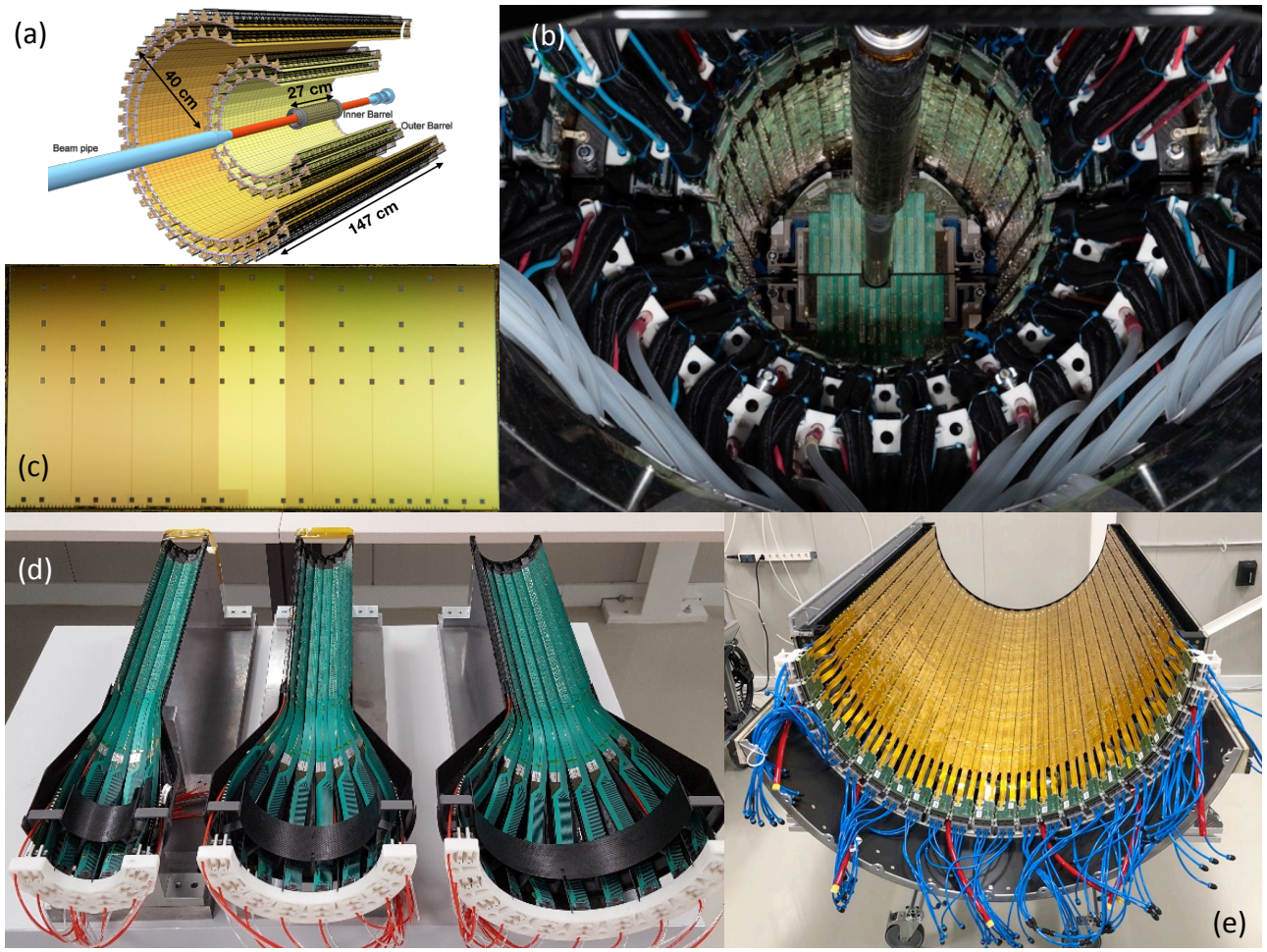
low resistivity high resistivity

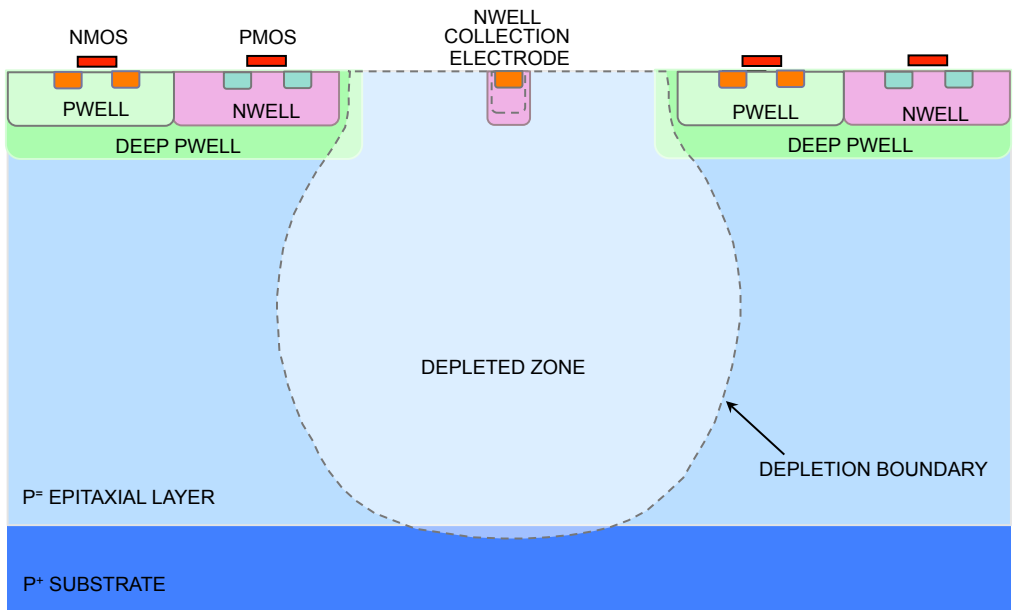
For thinner epitaxial layers, higher resistivity does not help for further depletion due to the proximity of the substrate

Depletion constrained by the substrate and surrounding pwells

State of the art: ALICE Inner Tracking System 2 : 10 m^2 with 3x1.5 cm^2 ALPIDE chips

TowerJazz 180 nm imaging CMOS technology, development 2012-2016





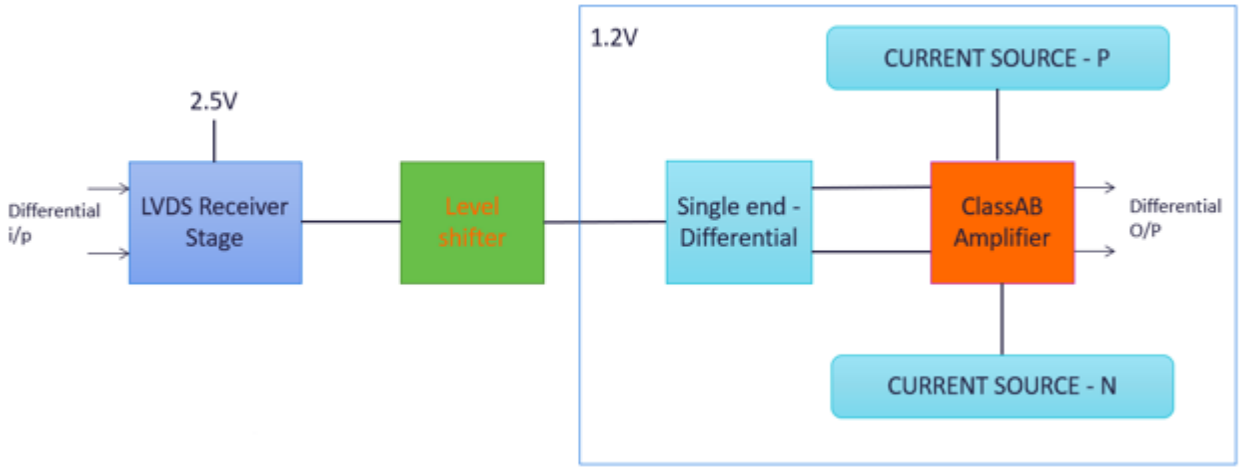
ALPIDE CHIP

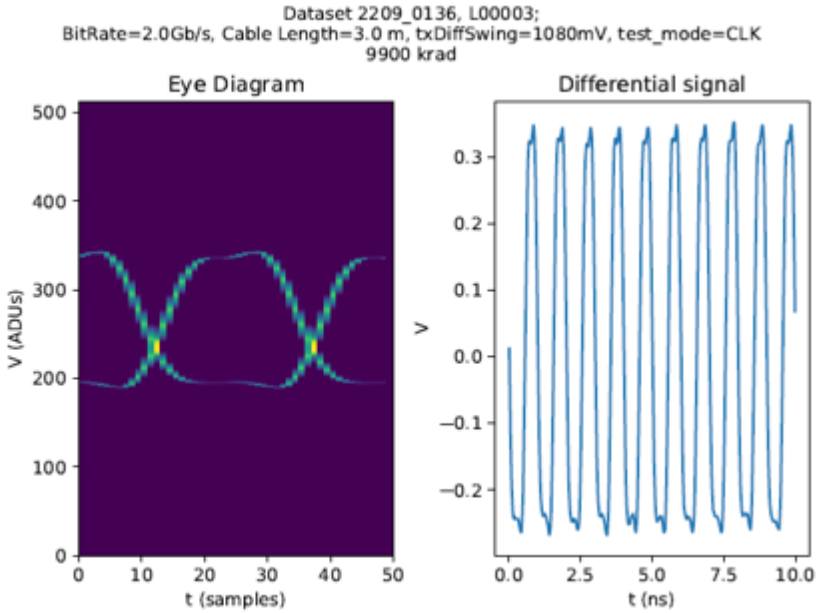
- 512 x 1024 pixels of 28 x 28 μm^2
- Full CMOS in the pixel (deep pwell)
- 40 nW front end, sparse readout
- Matrix 6 mW/cm^2, up to 40 mW/cm^2 including periphery
- Standard process: sensitive epitaxial layer not depleted

STFC

RAL: S. Mathew, Iain Sedgwick

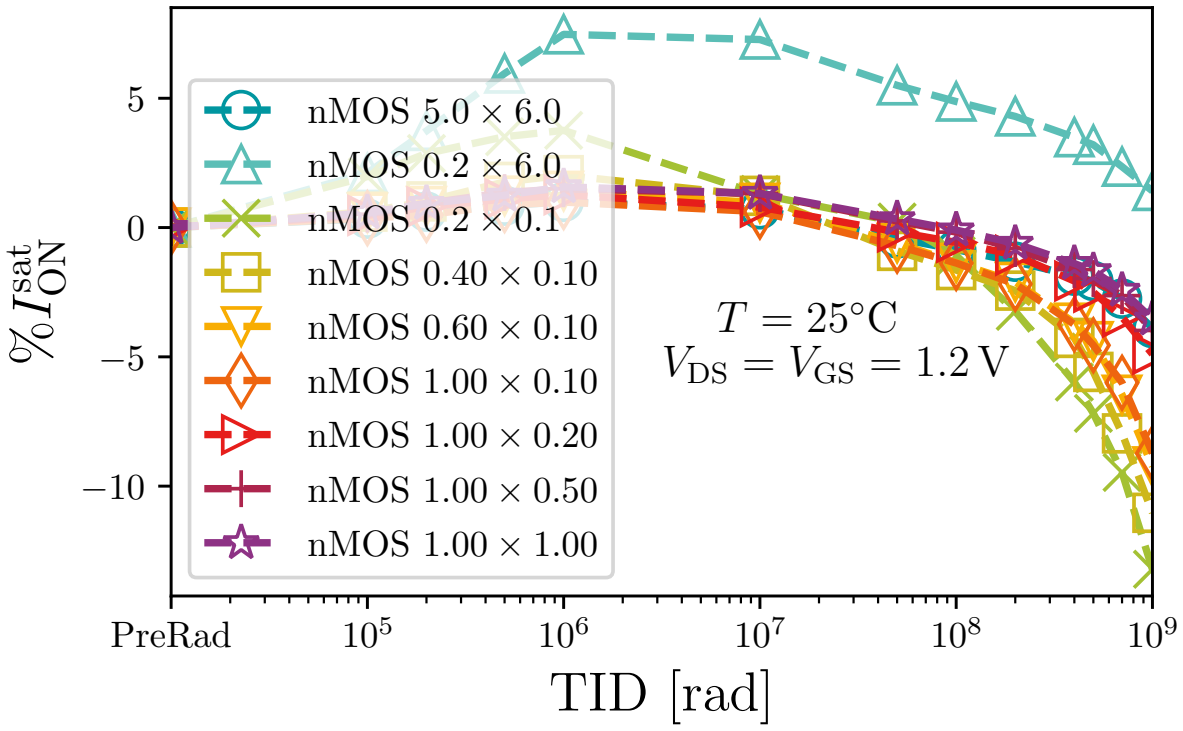
- MLR1 submission with CML driver:

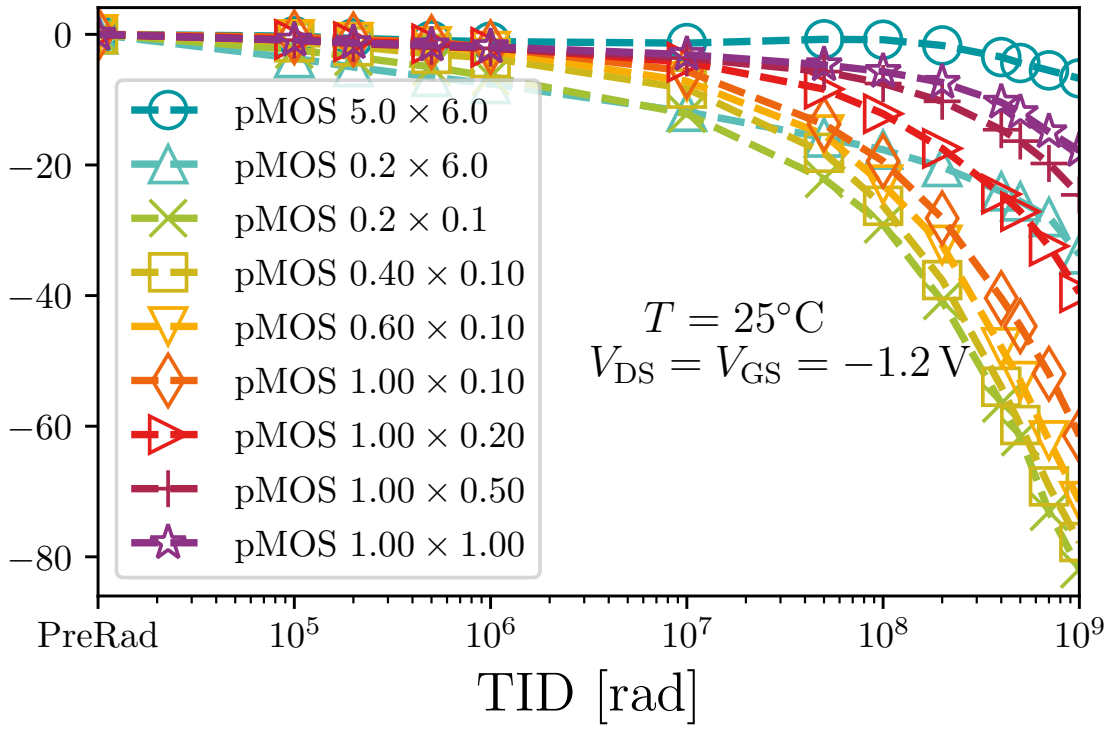




- Several other institutes have submitted test chips: Yonsei and SLAC (pixel test matrix), DESY (test pixels and Krummenacher feedback amplifier)

Transistor radiation tolerance

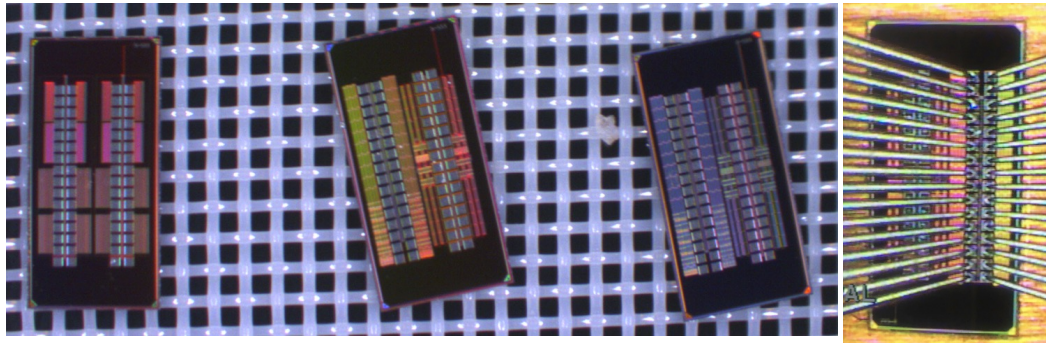




In line with other 65 nm technologies, no showstoppers.

Small size PMOS transistors degrade significantly after several hundred Mrad.

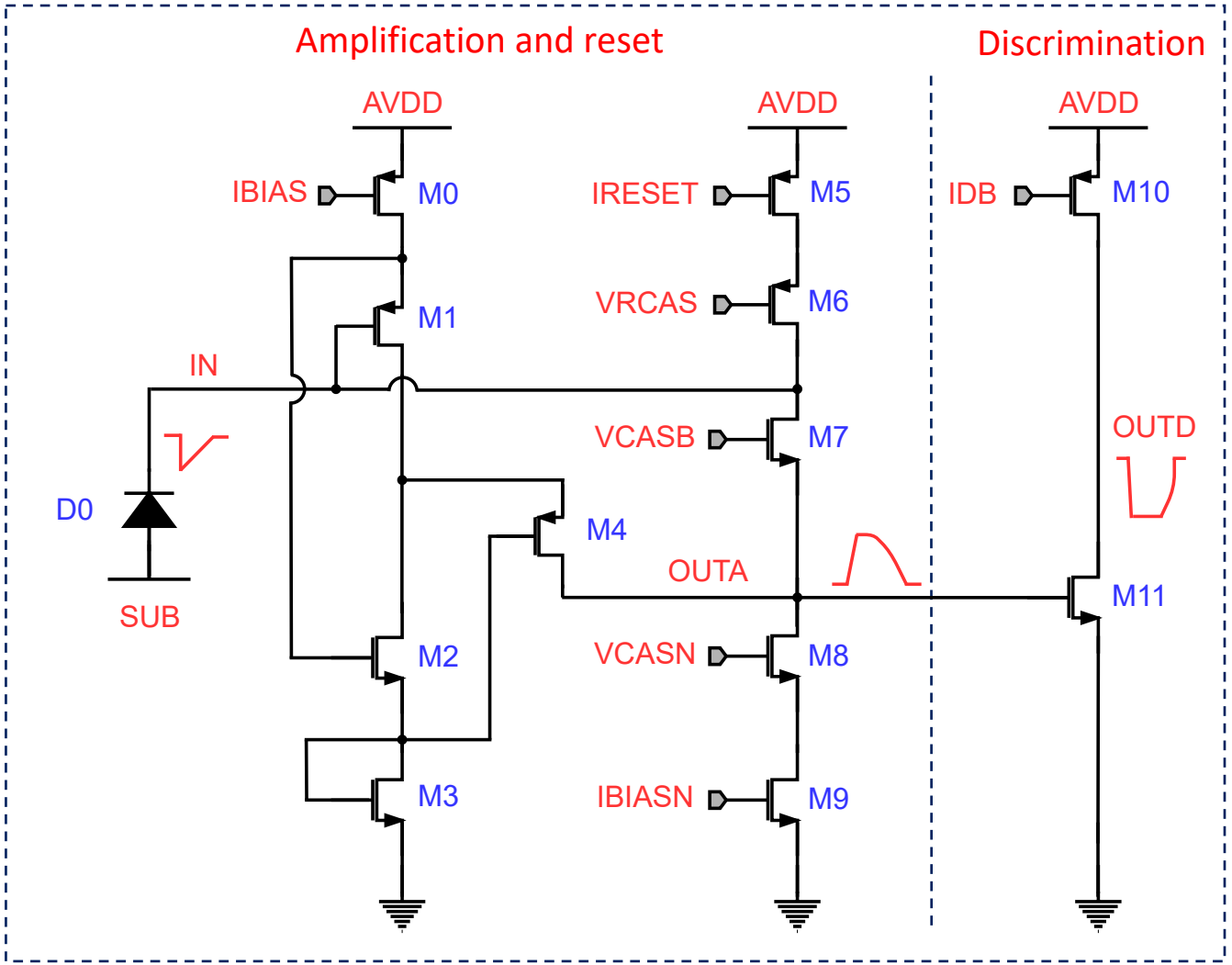
Caveat: modeling of transistors with significant reverse bias



A. Dorda Martin et al. “Measurements of total ionizing dose effects in TPSCo 65 nm and influence of NMOS bulk bias”. doi: 10.1088/1748-0221/18/02/C02036

DPTS Analog front-end

see also: F. Piro IEEE NSS 2022



Benefits from low sensor capacitance (< 5fF).

- Source follower (M1) to compensate C_{GS} capacitance.
- M2, DC coupled to the source of M1, contributes to the gain using the same current.
- Cascode transistors M4 and M8 provide high gain on OUTA.
- DC coupling requires feedback to input through M7. Current provided by M5-M6.
- M10-M11 form a simple discriminator with threshold set by the IDB current source.

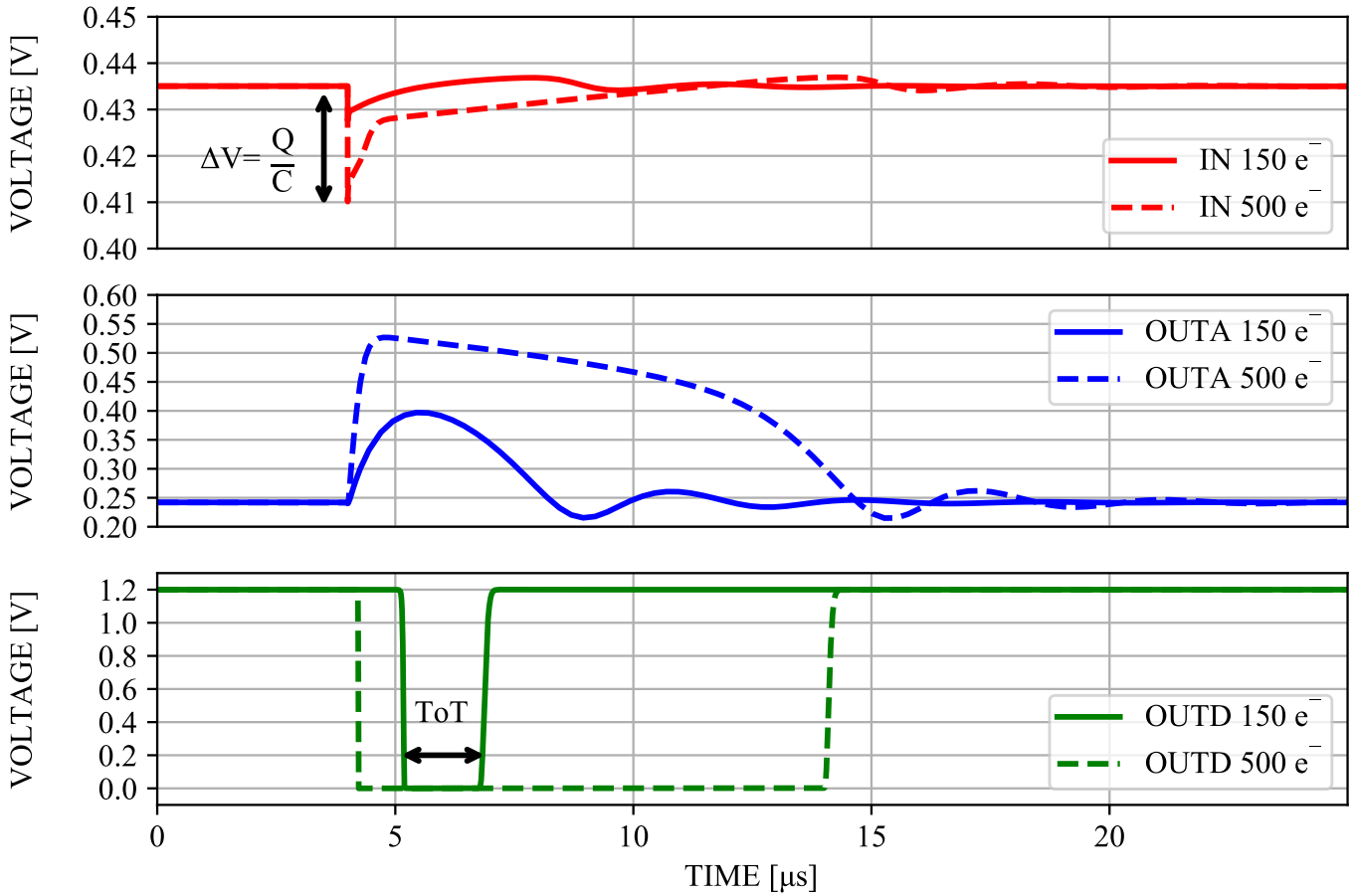
Tunable IBIAS-IBIASN (IBIAS = 10 x IBIASN) currents to set lower power consumption or faster timing response.

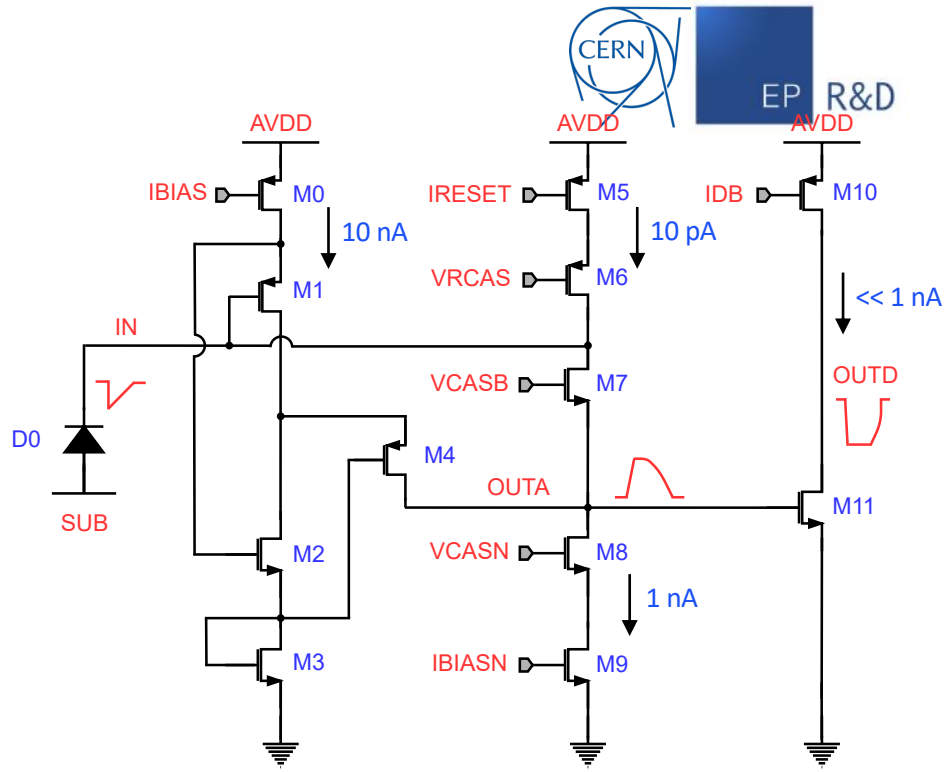
L. Cecconi, et al., “Design and readout architecture of a monolithic binary active pixel sensor in TPSCo 65 nm CMOS imaging technology ”, TWEPP 2022.

DPTS Front-end simulations

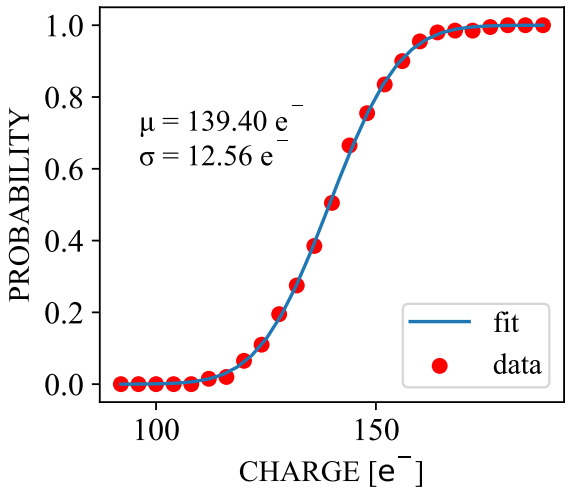
Simulation results with ≈ 12 nW power consumption – lowest power mode.

Gain @ threshold ≈ $1\ \mathrm{mV/e^-}$, 1 µs peaking time.

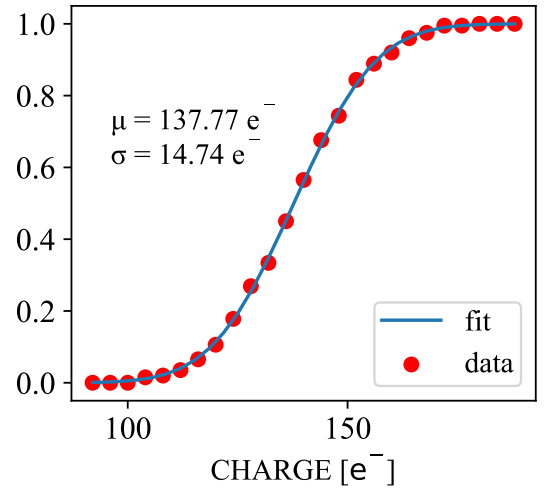




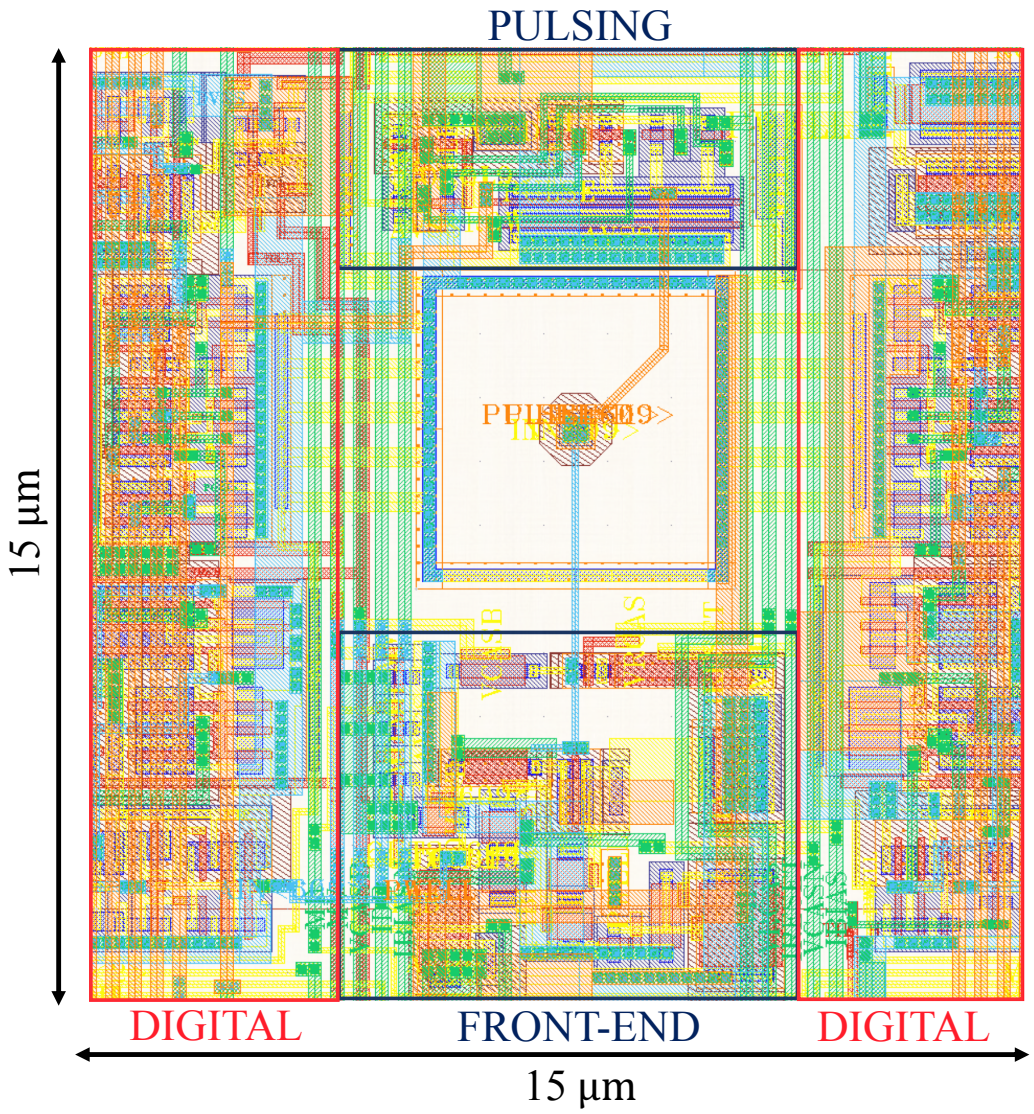
Monte Carlo



Transient noise



DPTS Pixel layout and measurements



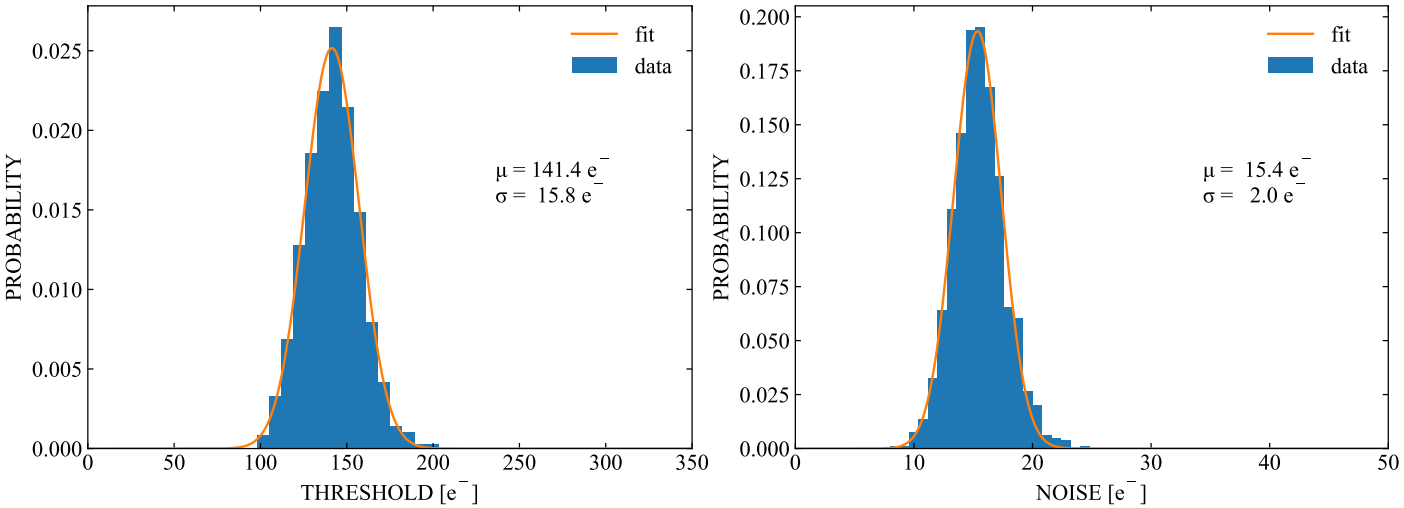
In-pixel circuitry:

- front-end amplifier and discriminator ($42\ \mu m^2$).
- test pulse injection circuitry ($17\ \mu m^2$).
- digital gates for asynchronous transmission of the time-encoded pixel address ($140\ \mu m^2$).

Analog power density over the matrix as low as $\sim$ **5 mWcm^{-2}**.

Good agreement with simulations

threshold dispersion $\approx 15.8\ e^-$ noise $\approx 15.4\ e^-$



Measurements - front-end time walk

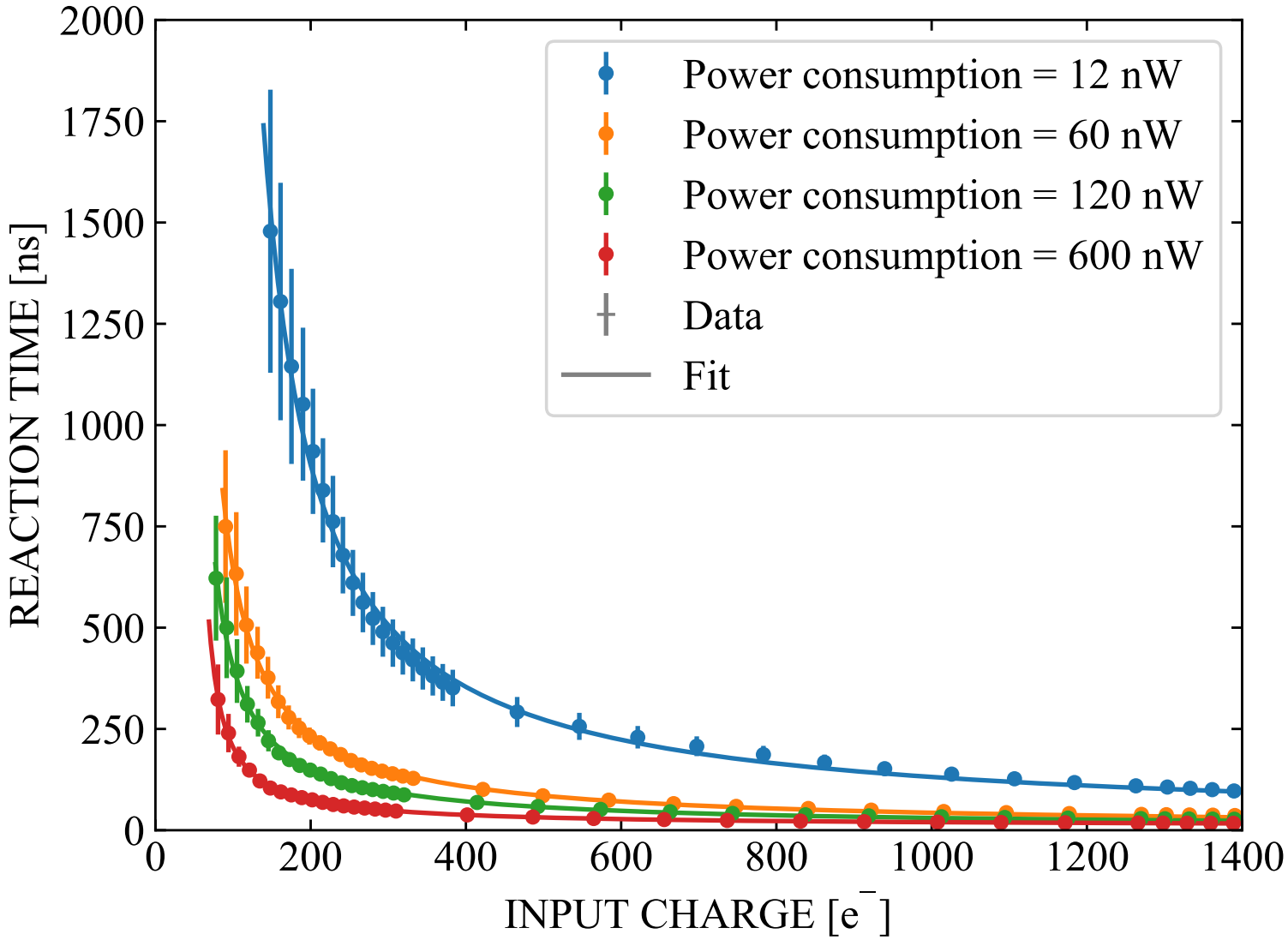
For a power consumption of 12 nW, with charges $> 200\ e^-$ (35% of a MIP charge):

- time response $< 1\ \mu s$
- jitter < 150 ns

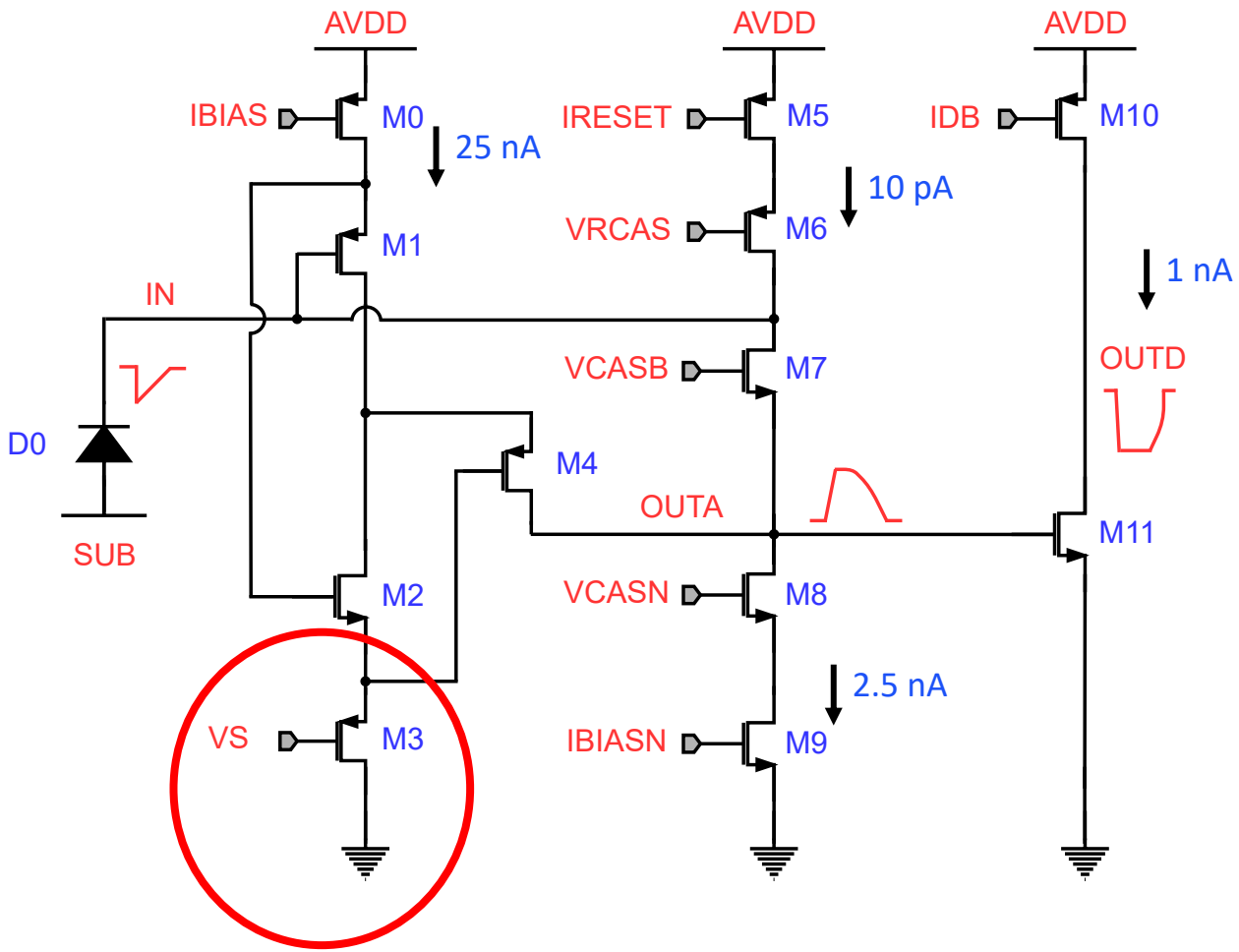
For a power consumption of 600 nW, with charges $> 350\ e^-$:

- time response < 25 ns
- jitter < 1.2 ns

Can go up to a few µW. Power increased by increasing IBIAS = 10 IBIASN.



MOSS front-end



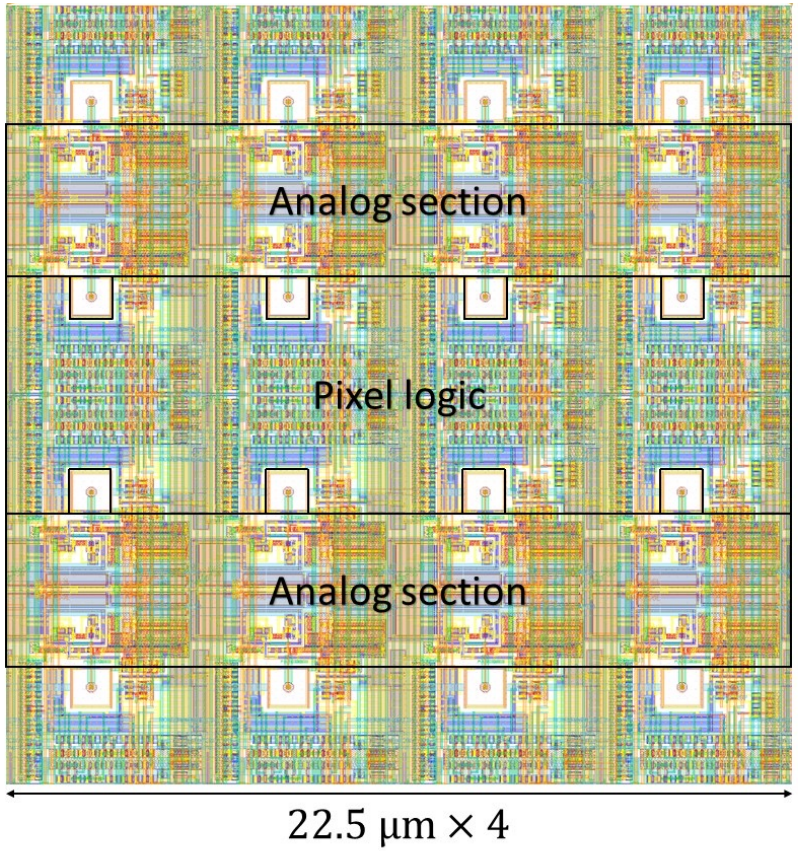
Conservative layout to respect DFM rules.

PWELL/PSUB to be kept at ground for high yield:

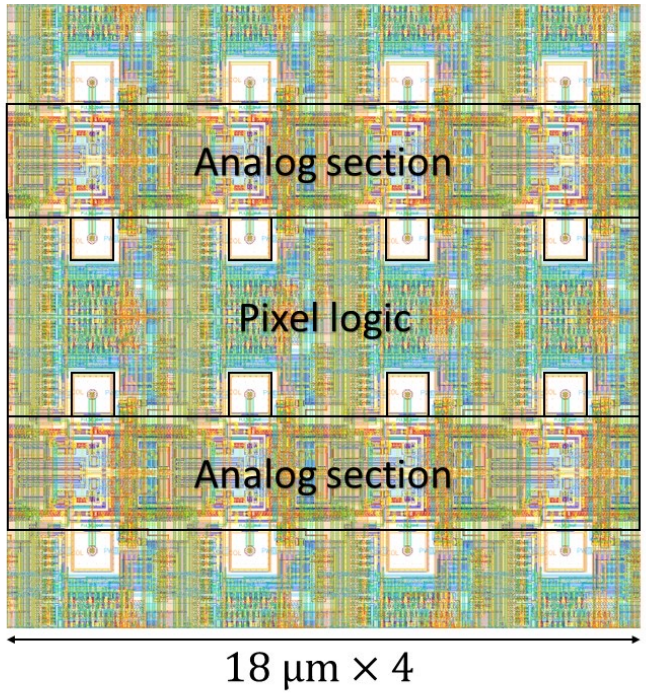
- Transistor M3 converted to a PMOS to be able to shift up the collection electrode voltage through front-end settings and increase sensor reverse bias.

Higher current for more margin

MOSS pixel layout



Power density ≈ 7.11 mWcm^{-2}



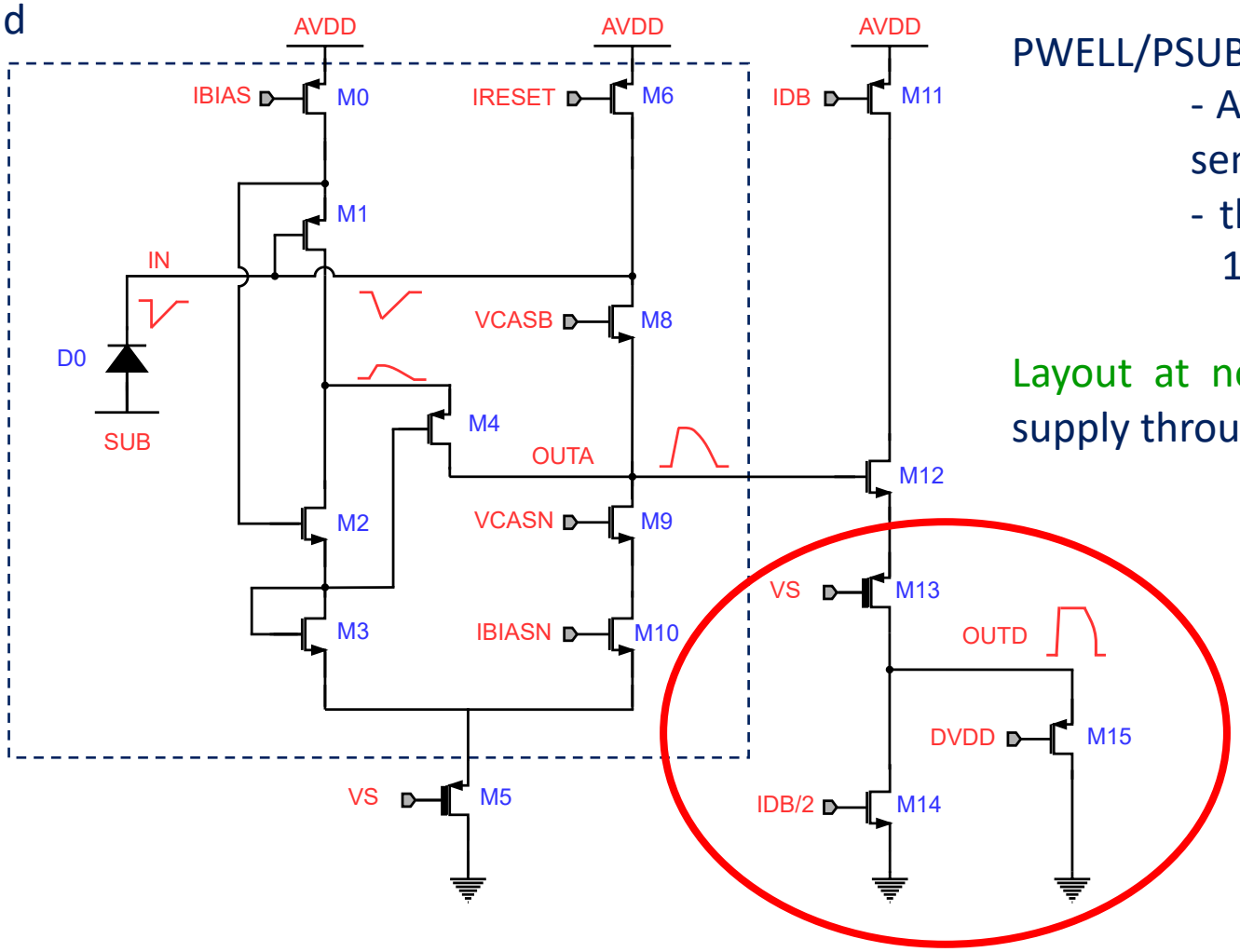
Power density ≈ 11.11 mWcm^{-2}

Performance obtained with PEX simulations

Parameter	Value
Area	60 µm^2
Power	36 nW
Gain	0.5 mV/e$^-$
Threshold	150 e$^-$
Peaking Time	1 µs
Phase Margin	60°
Thr. Dispertion	11.5 e$^-$
ENC	12 e$^-$

MOST front-end

DPTS front-end



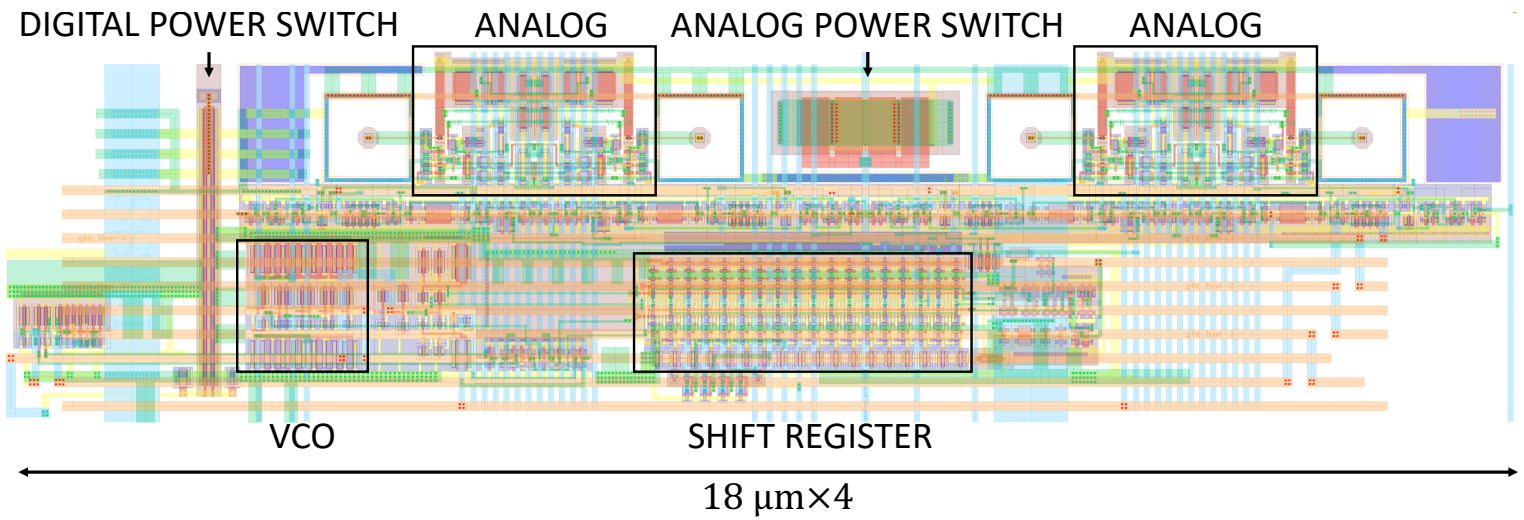
PWELL/PSUB connected to analog ground:

- AVDD to create headroom and accommodate large sensor reverse biases through the front-end settings.
- thick oxide transistors (M5-M13) to allow AVDD > 1.2 V

Layout at normal density -> groups of pixels connected to supply through switches to power gate defect pixels

Adaptation of the interface to the digital domain.

MOST pixel layout



Power density $\approx 11.11\ \mathrm{mWcm^{-2}}$

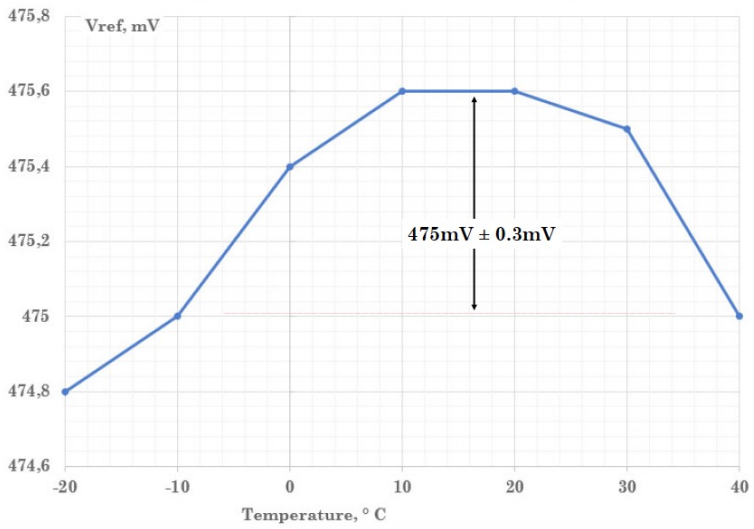
Performance obtained with PEX simulations

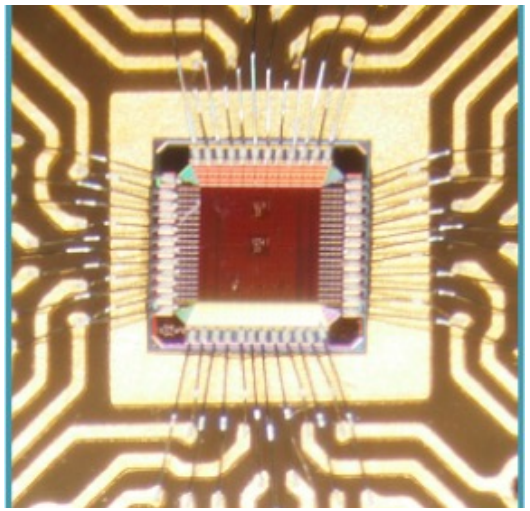
Parameter	Value
Area	$45\ \mu\mathrm{m}^2$
Power	$36\ \mathrm{nW}$
Gain	$1\ \mathrm{mV/e^-}$
Threshold	$150\ \mathrm{e^-}$
Peaking time	$1\ \mu\mathrm{s}$
Phase Margin	$55°$
Thr. Dispertion	$15\ \mathrm{e^-}$
ENC	$10.5\ \mathrm{e^-}$

IP Block measurements bandgap, T-sensor, VCO: all functional and tolerant to 100 Mrad or beyond

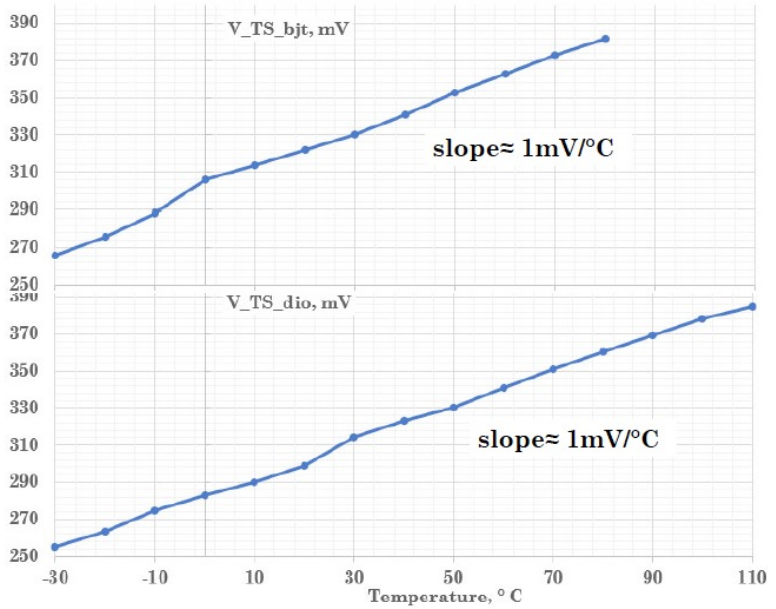
NIKHEF: V. Gromov, D. Gajanana, A. Yelkenci, A. Grelli, R. Kluit, M. Rossewij (TWEPP 2022)

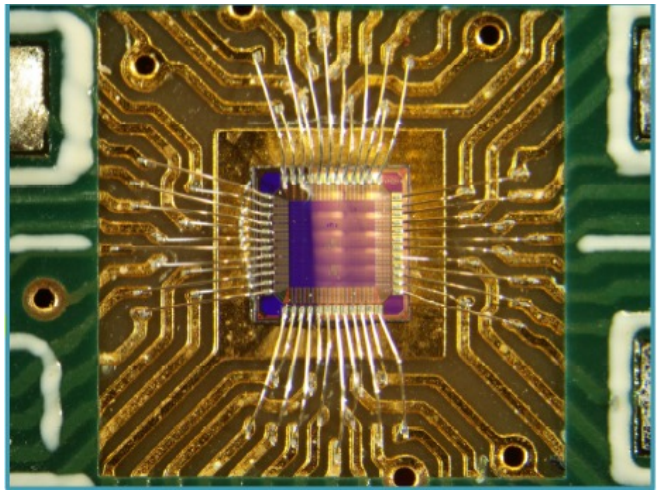
Bandgap



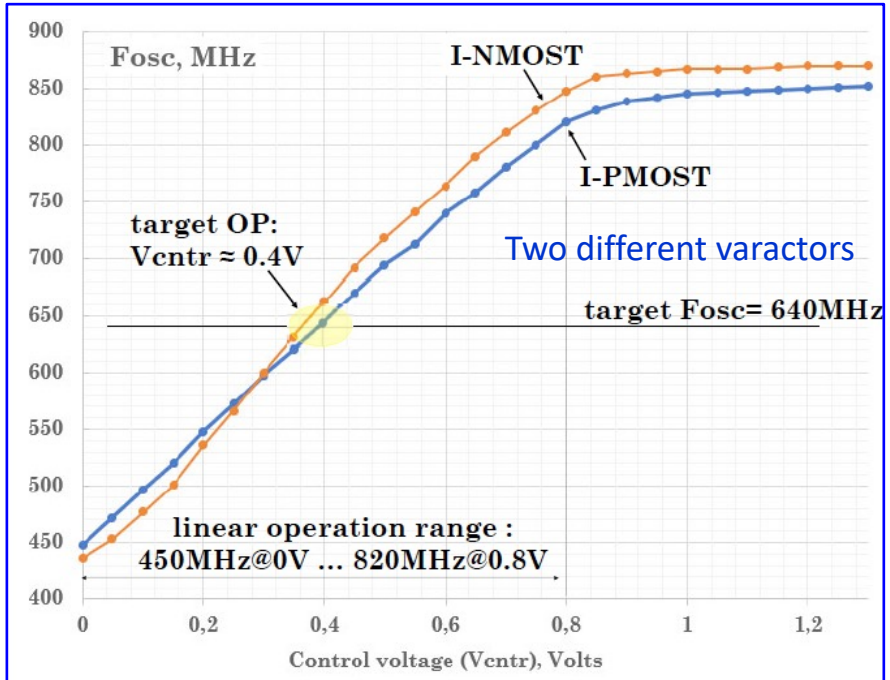


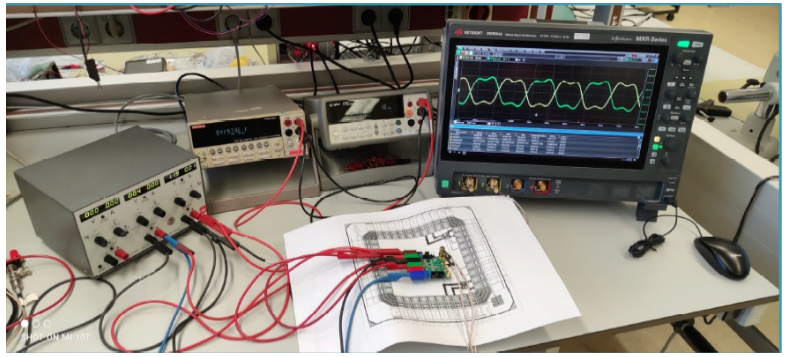
Temperature sensor





Voltage Controlled Oscillator (VCO)





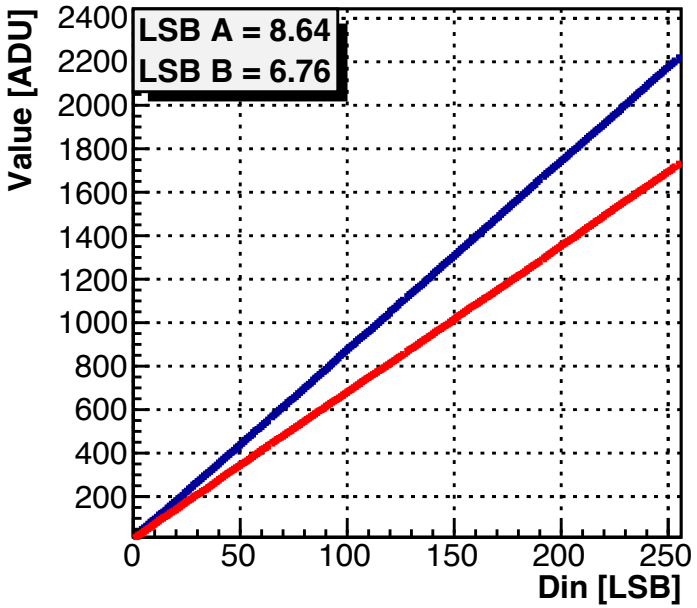
IP Block measurements DAC

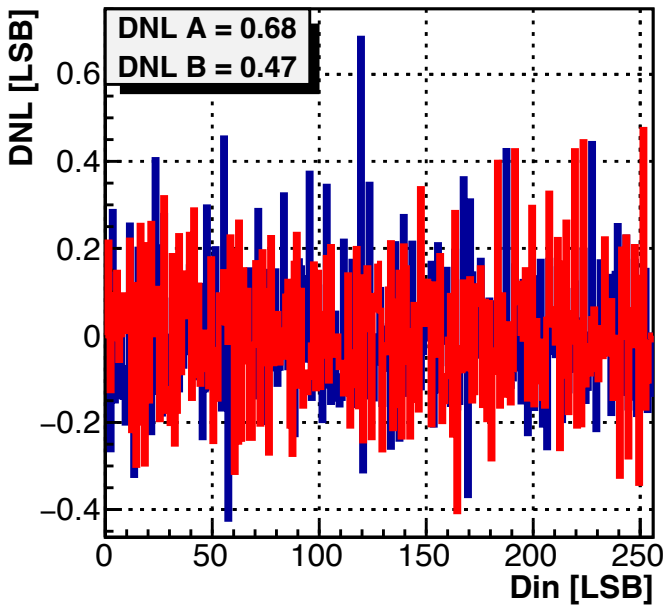
IPHC: I. Valin, S. Bugiel, A. Dorokhov, C. Colledani, C. Hu et al.

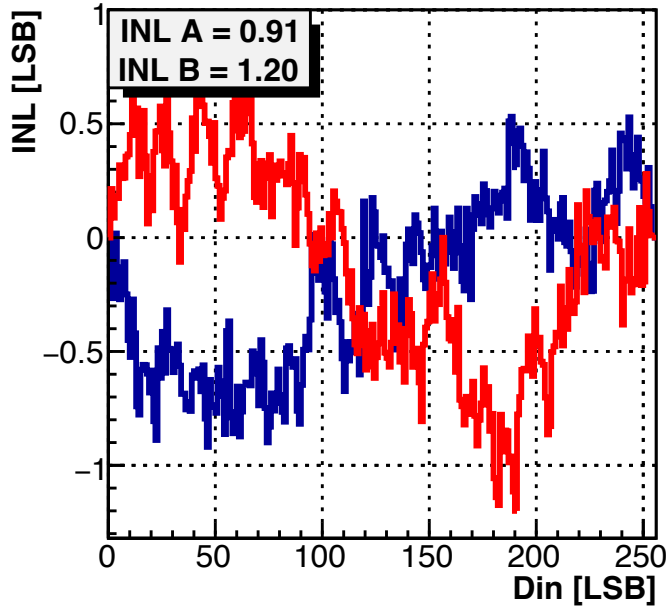
	DAC A	DAC B
Resolution	8 bit	8 bit
LSB [nA]	40	40
Reference current [uA]	-0.8	-10.72
Power [uW] (*)	13	13
Area [um x um]	133x253	143x253

Both DACs remain functional after 500 Mrad irradiation with DNL < 1 LSB, INL < 2 LSB

10 keV X-rays 6.5 Mrad/hour

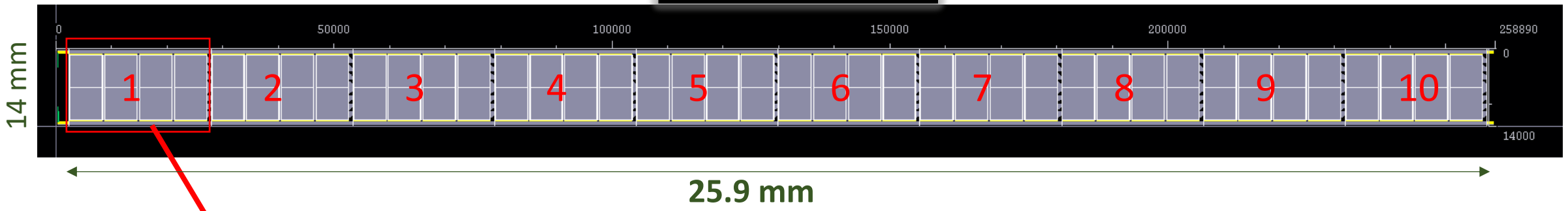




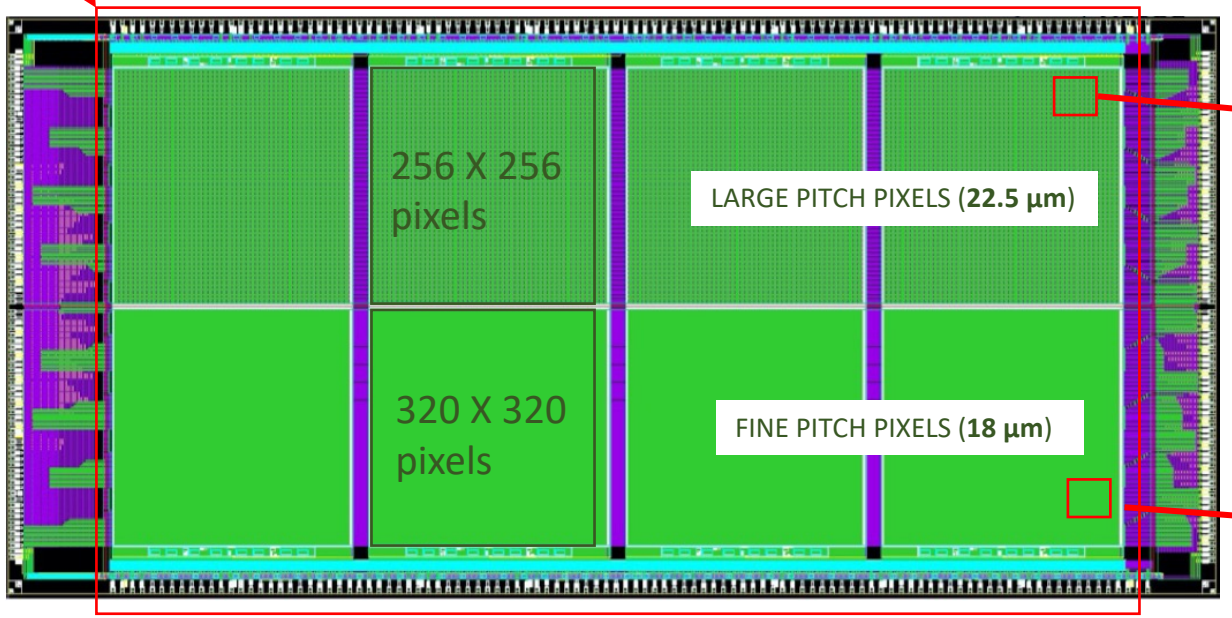


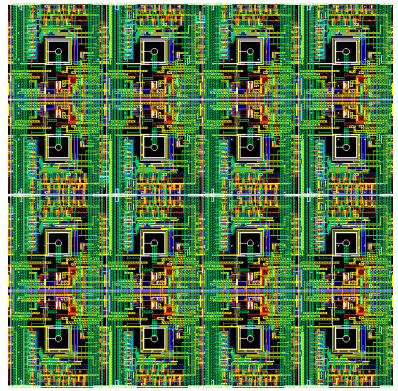
MOSS Layout

6.72 Mpixels

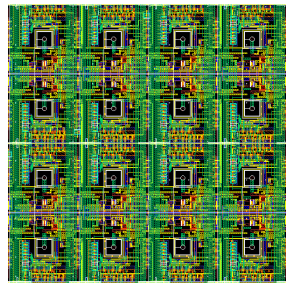


1 of 10



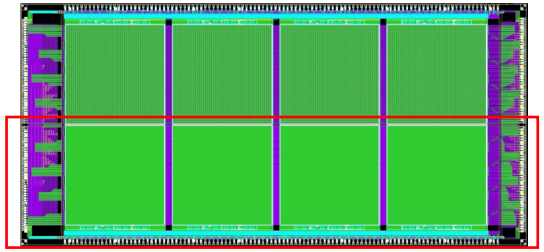


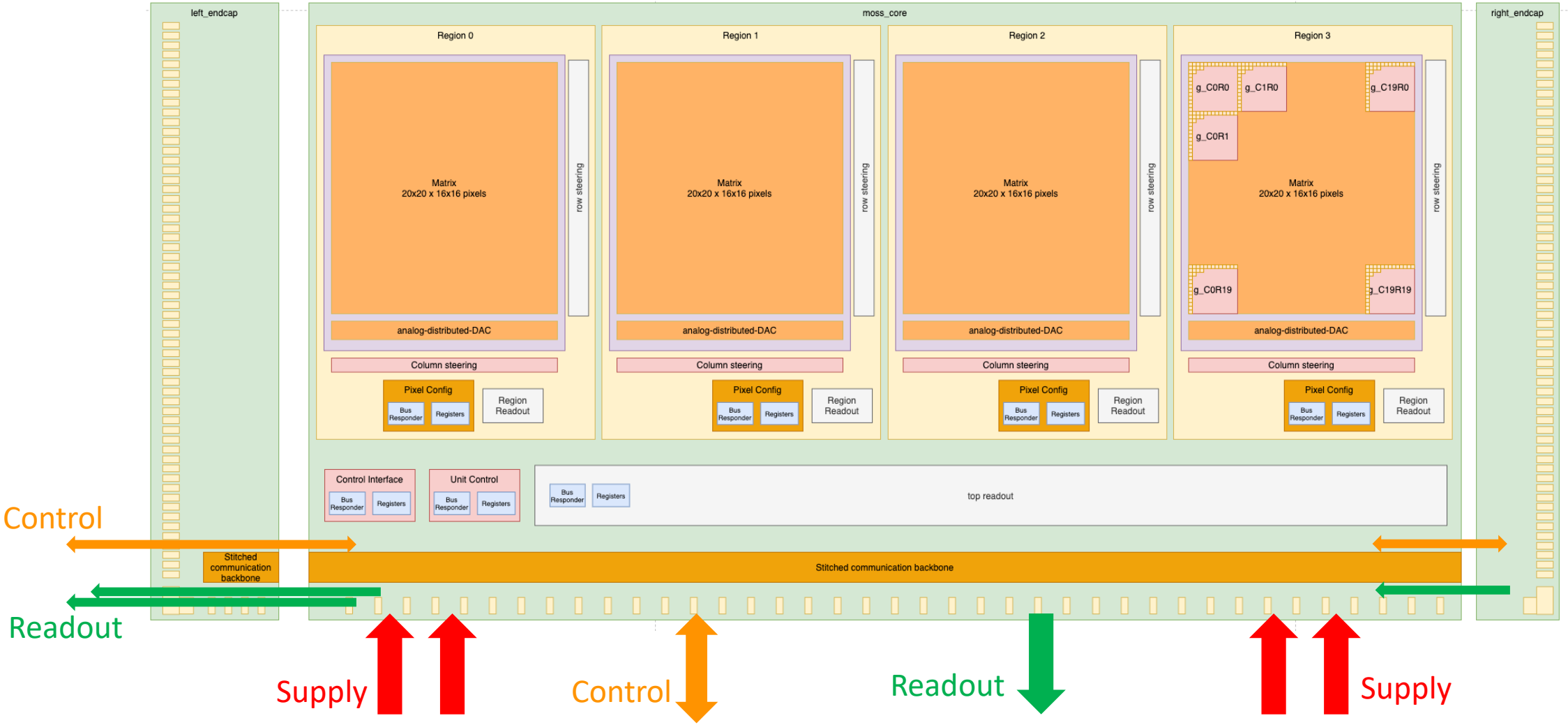
Pitch 22.5 µm



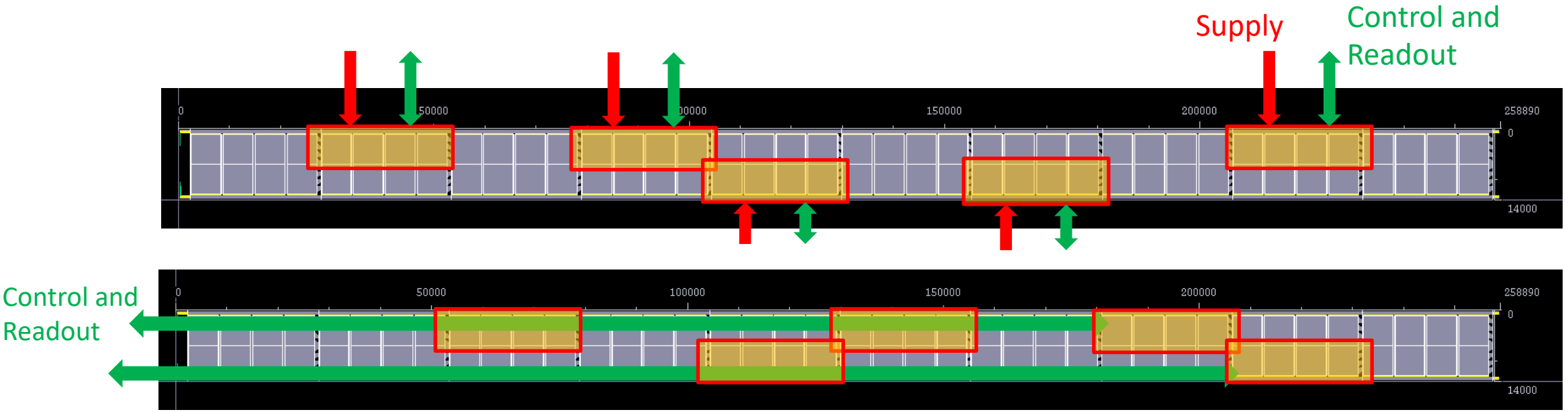
Pitch 18 µm

MOSS - Half Unit





MOSS TESTING SCENARIOS - EXAMPLES



Test the sub-units independently

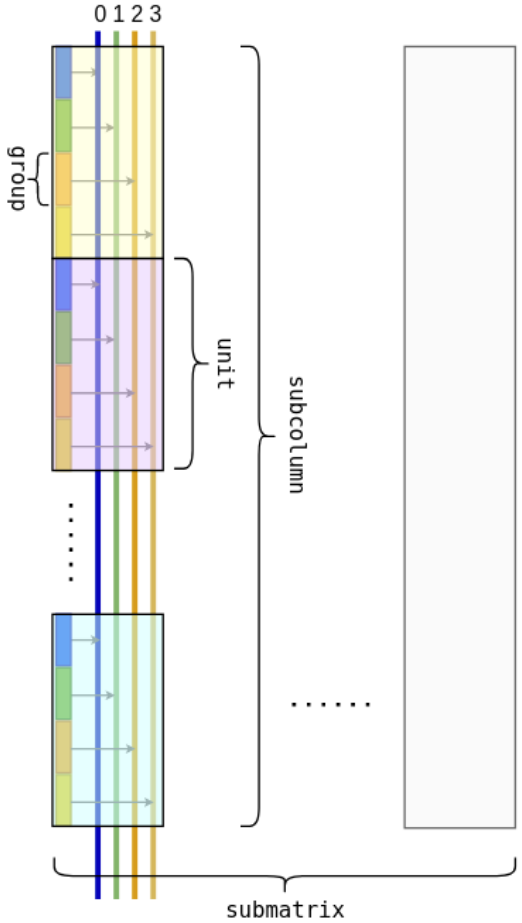
Study manufacturing yield

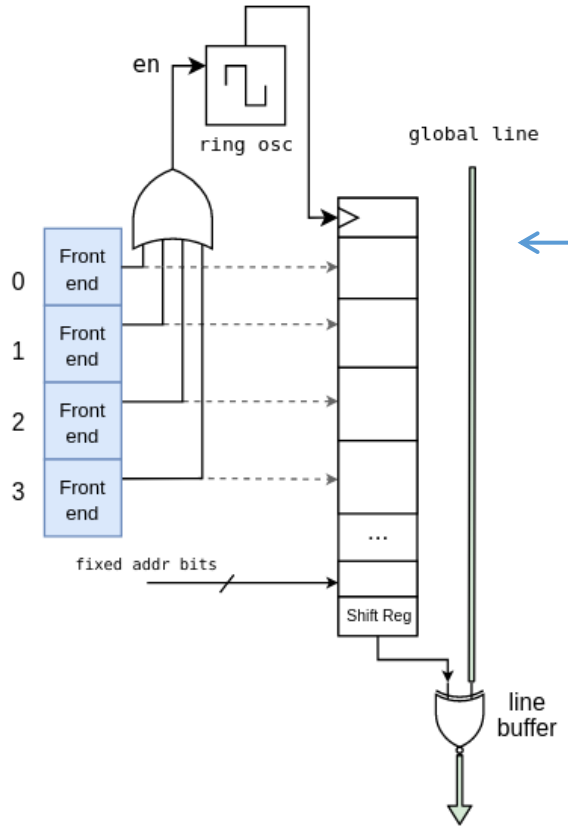
- Functional yield at half unit, block, column/row/pixel level granularity
- Possible dependence on pixel pitch and layout density?

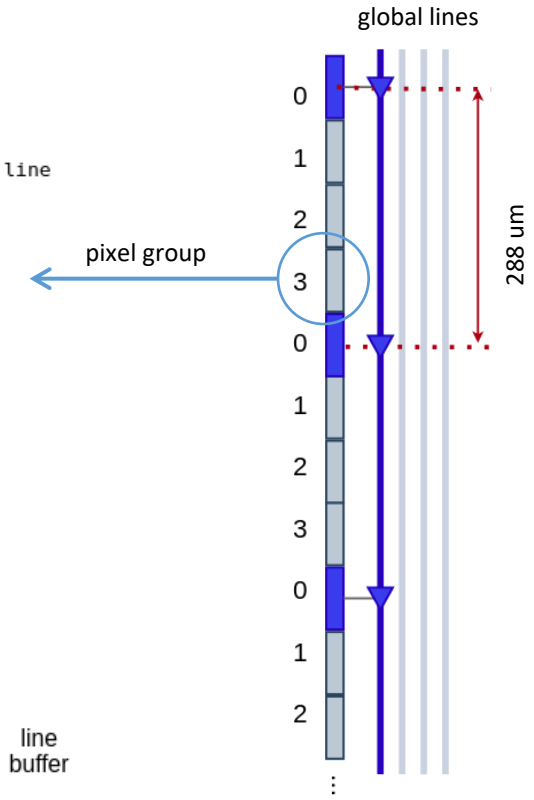
Study noise, threshold, position resolution vs pixel variants

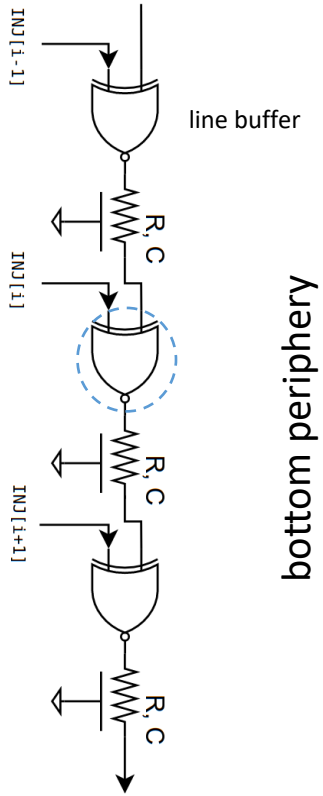
MOST Chip: more detail

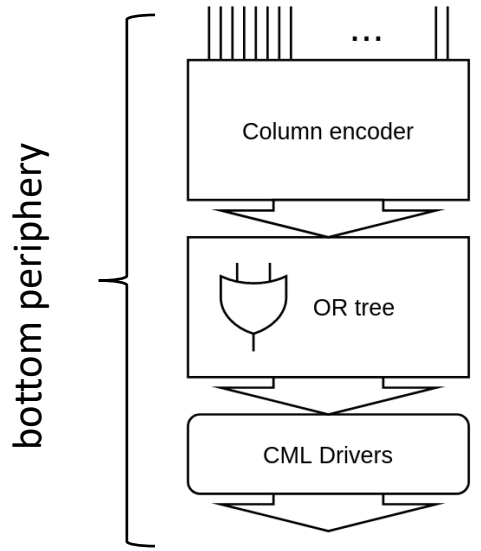
~ 90k pixels per stitch

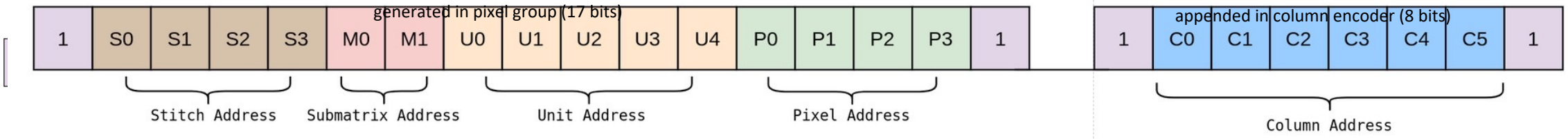




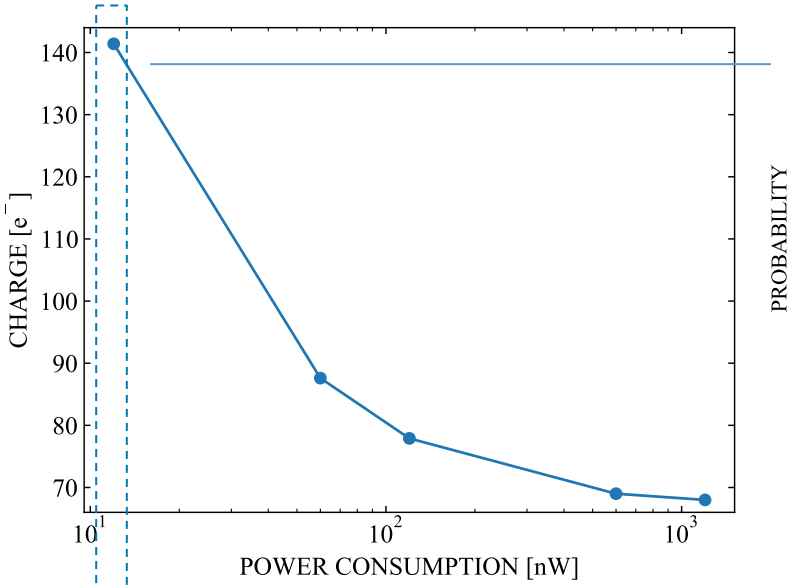


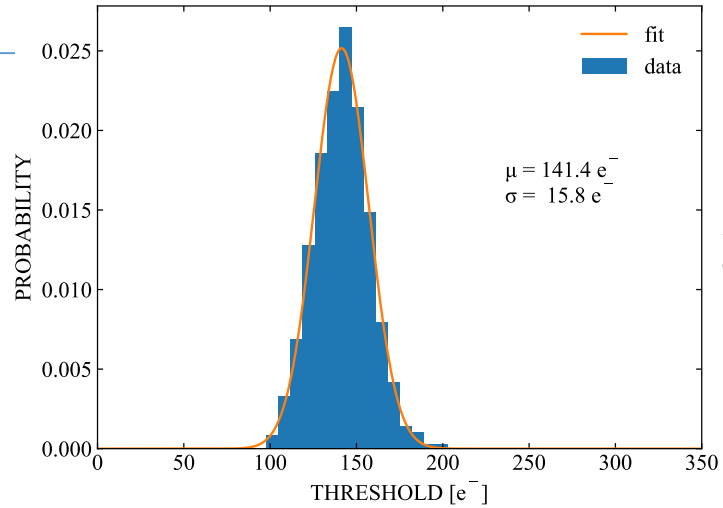


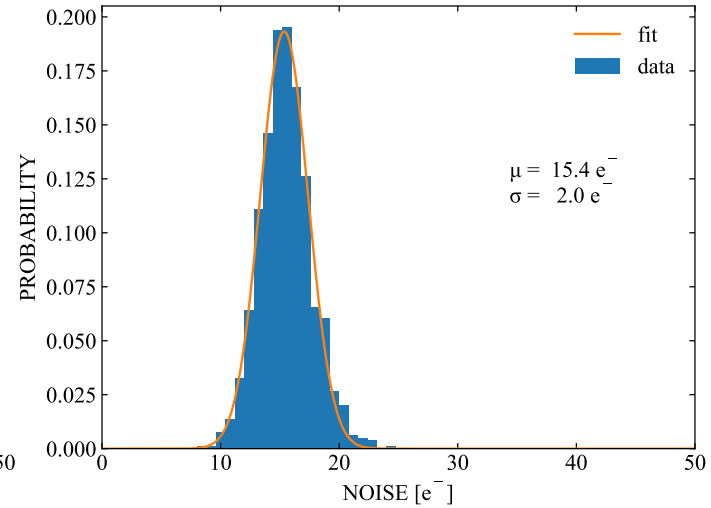




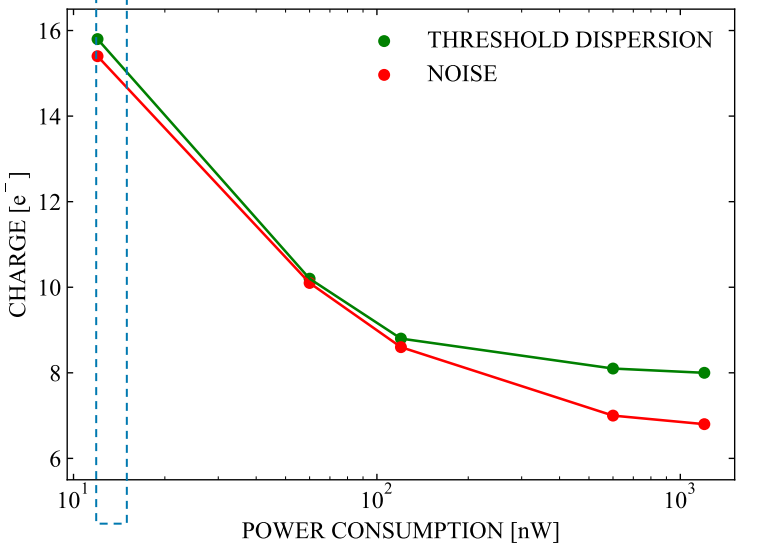
Measurements - threshold dispersion and noise

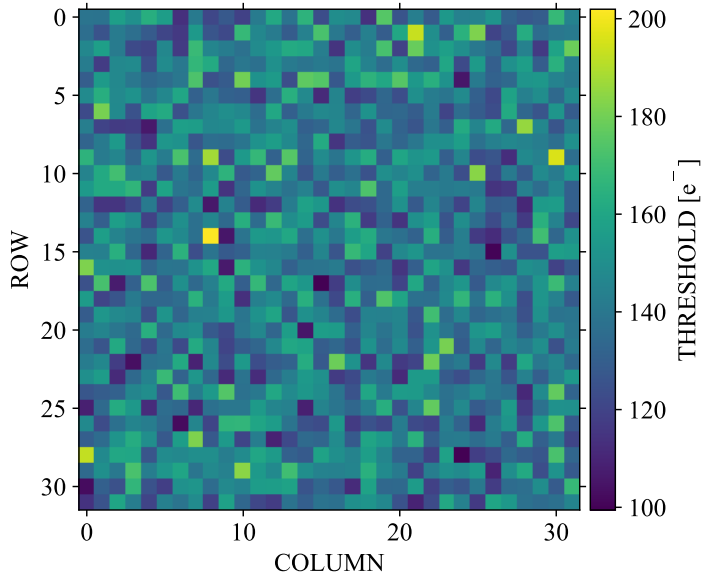


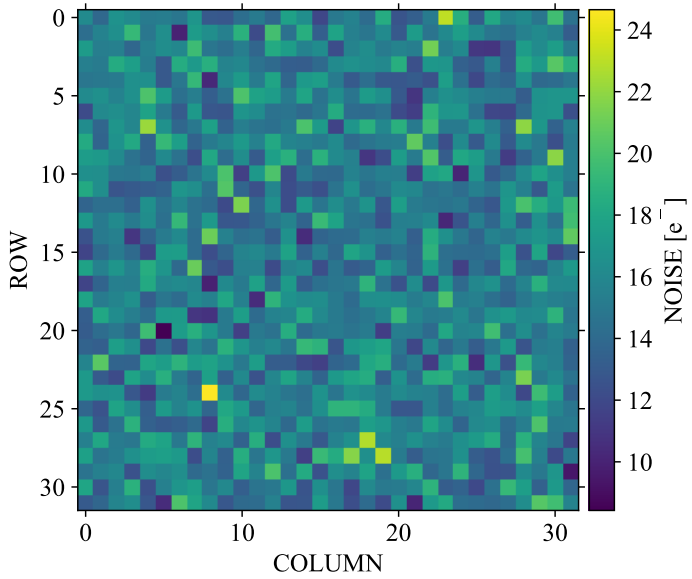




Good agreement with simulations (th.d. ≈ 15.8 e^- noise ≈ 15.4 e^-).







No systematic effect over the matrix.