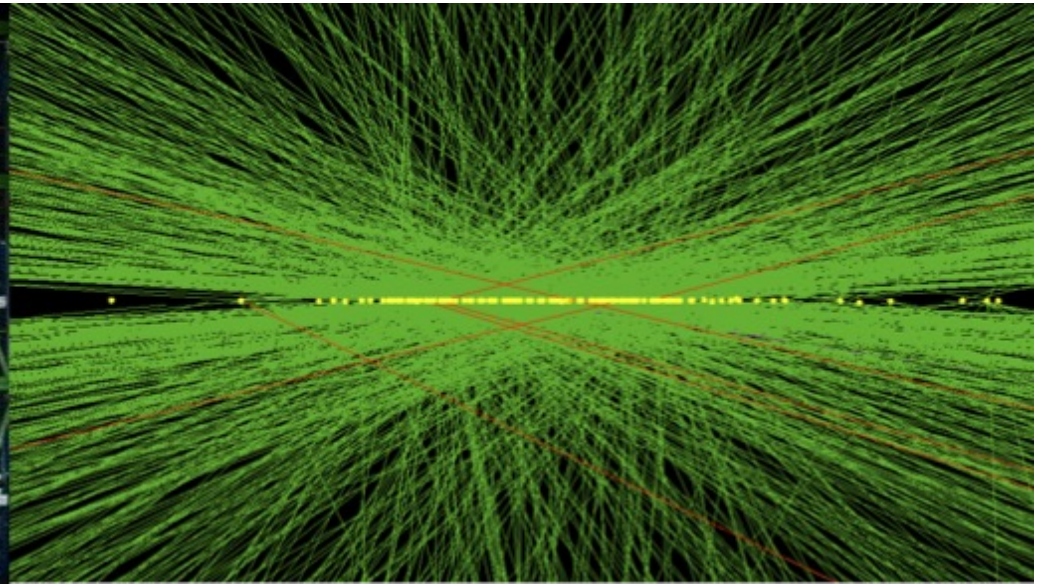
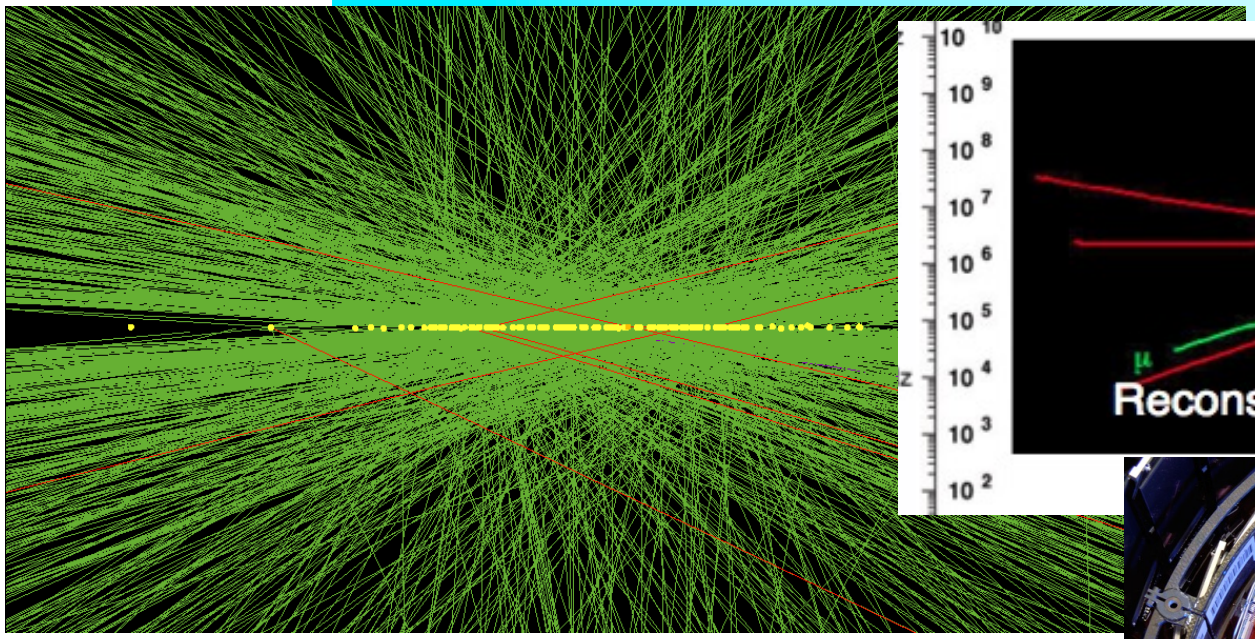
Precision timing ASIC (ETROC) development for CMS Endcap Timing Layer

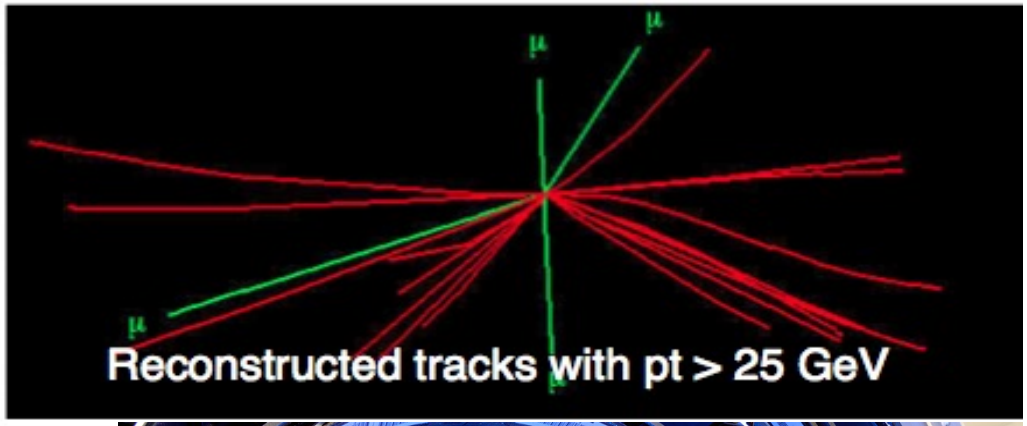
Ted Liu (Fermilab)

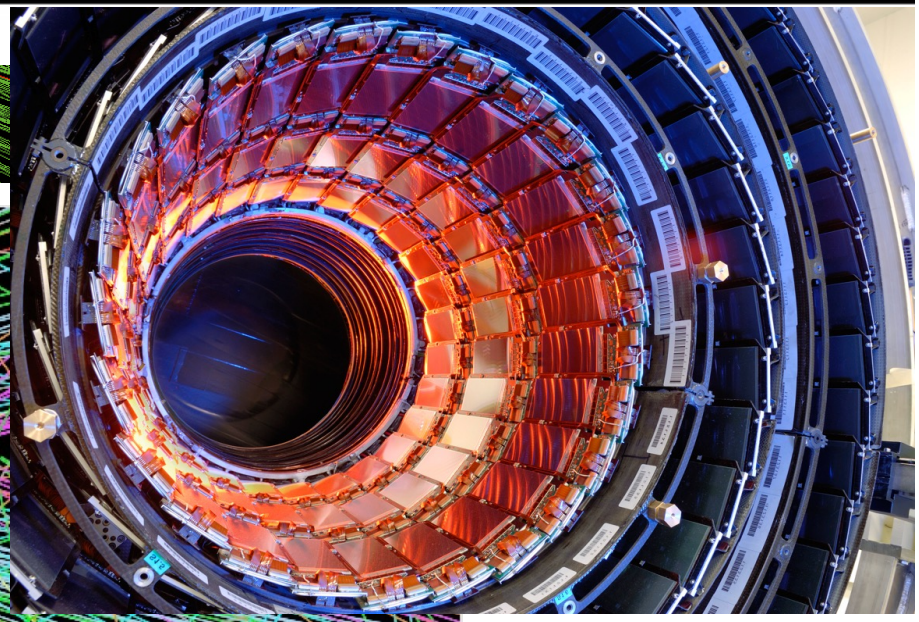
Sept 12-14, 2023, IDTM (Lisbon)

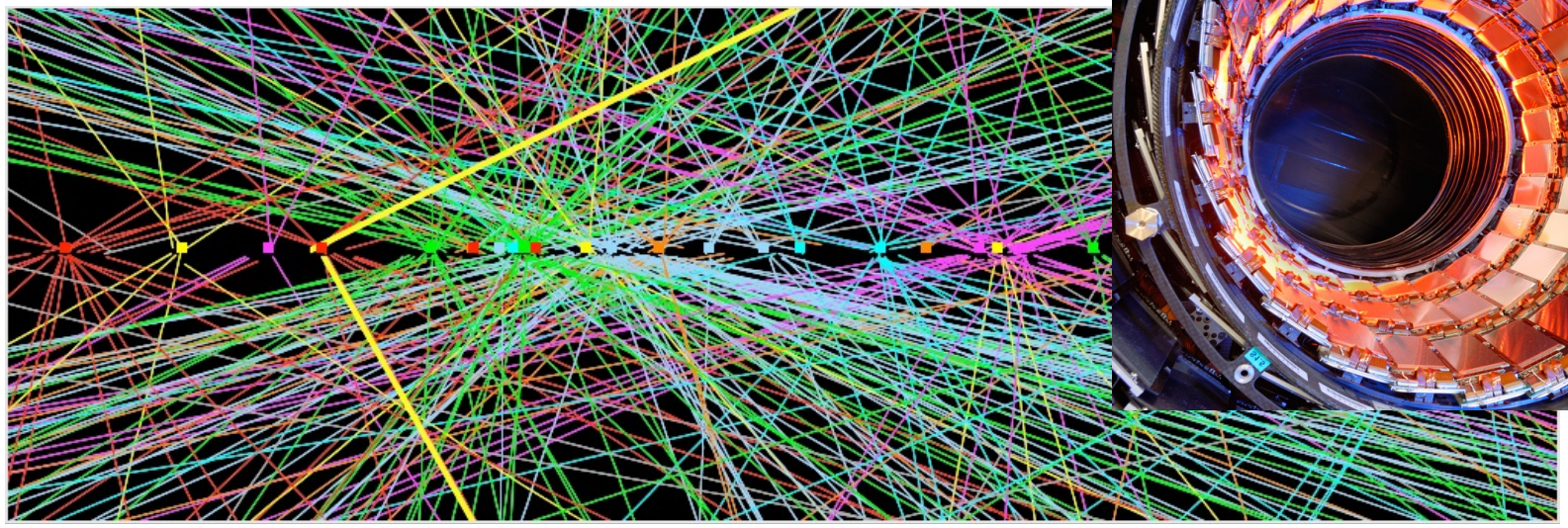


Higher luminosity means higher pile-up events





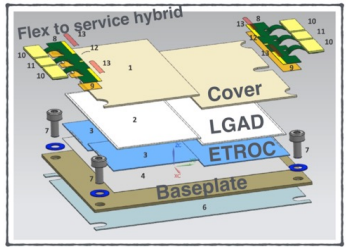




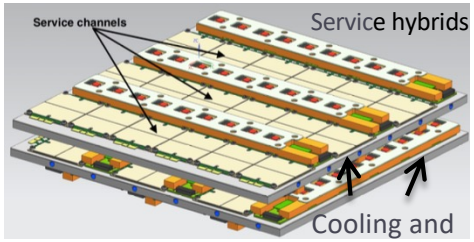
Silicon tracker with position information alone will not be enough to separate the pile-up events, precision timing detector can help: ***CMS Endcap Timing Layer (ETL) is designed for this purpose***

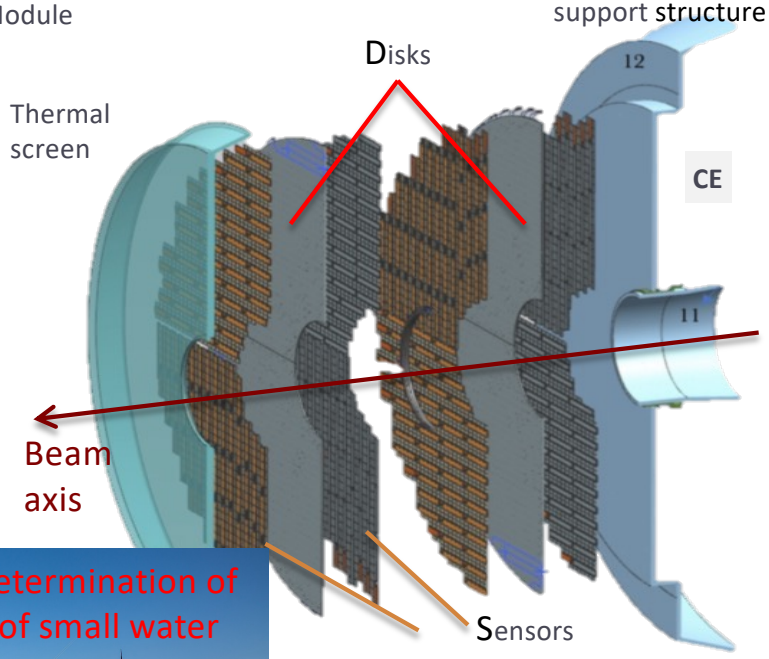
CMS ETL precision timing *challenges*

Low gain is the key ingredient to excellent temporal resolution



Module





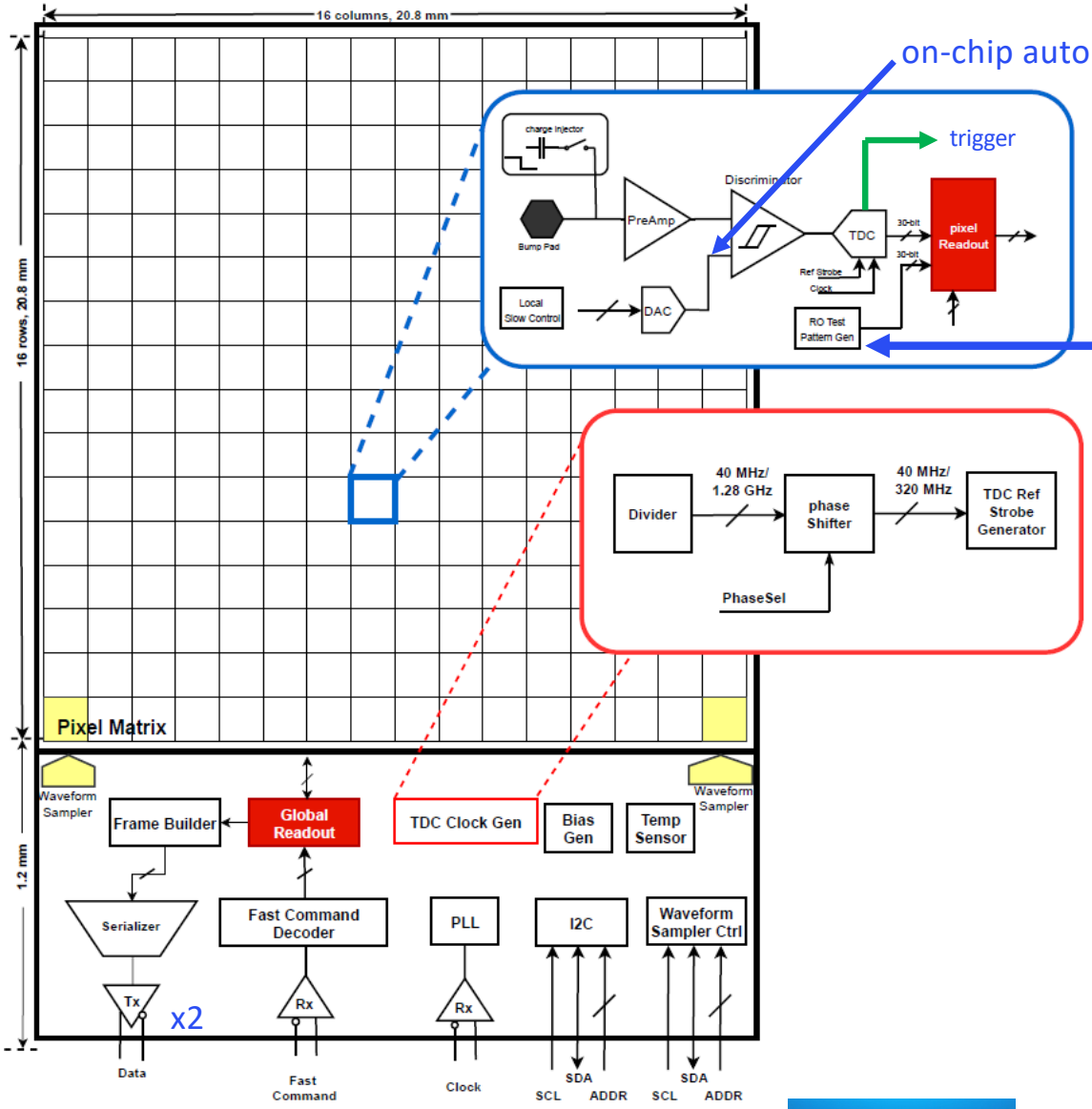
- Low Gain Avalanche Detectors (LGADs)
  - Basic unit:
    - 2x2 cm^2 LGAD bump-bonded to ETROC ASIC mounted on two sides of cooling plates
  - Two layers/disks per endcap (~2 hits per track)
  - $1.6 < |\eta| < 3.0$, surface ~14 m^2; ~9 M channels
  - Nominal fluence: ***1.7×10^{15} n_{eq}/cm^2*** (@ 3000 fb^{-1})
- LGAD gain modest: 10-30
  - LGAD Landau contribution: ~ 30ps
  - Front-end contribution should be kept < 40ps
  - < 50ps per hit, or 35ps per track (with 2 hits)
- ***Extract precision timing from***

  Small LGAD signal (typical 10-20 fC)
  - ***With low power: < 4mW/channel on average***

Challenges:

Low power and fast/precision timing,
Precision clock distribution,
Minimizing readout digital activities

ETROC: Endcap Timing ReadOut Chip



on-chip auto threshold calibration

Self-test capability (for ***design verification*** & chip and system level testing with backend)

- Measuring arrival time of LGAD signal
  - Front-end: PA + Discriminator + TDC
  - L1 latency circular buffer
  - L1A-driven readout with zero suppression
  - A coarse map of ***delayed*** hits for L1 trigger
- Interface of ETROC
  - 40 MHz reference clock
  - I2C-based slow control
  - 320 Mbps fast control
  - Serial data link 320/640/1280 Mbps
- Waveform Sampling of preamp output (only 1 pixel)
  - For test & monitoring purpose

ETROC: Precision determination of the arrival time of small water drop ripples

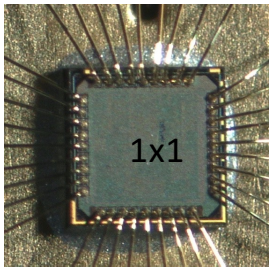
ETROC prototyping history (R&D phase before ETROC2)

Sept 2018 — Dec 2018 — May 2019 — Aug 2019 — March 2020 — May 2020 — July 2021 — Sept 2021 …

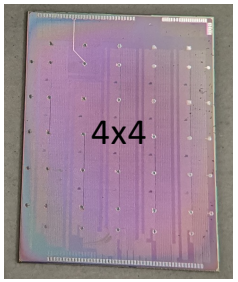
Covid

Project started

ETROC0 submitted



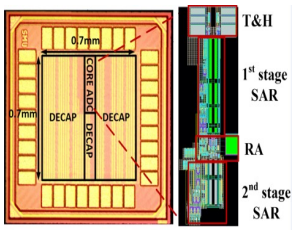
ETROC1 submitted



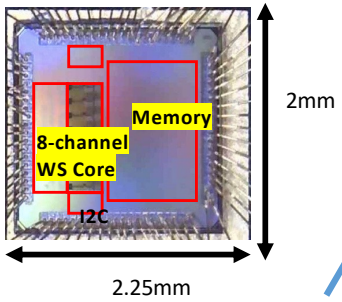
ETROC2: 8x8 → 16x16

Decision to go for full size full functionality ETROC2, Delay submission and add few test chips …

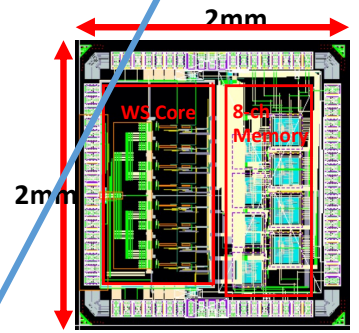
Single channel ADC submitted



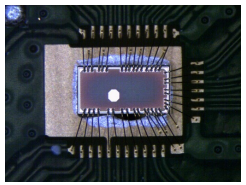
8-channel ADC Waveform Sampler (WS1) submitted



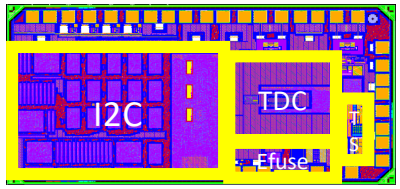
Rad-hard version of Waveform Sampler (WS2) submitted



ETROC-PLL mini ASIC submitted



I2C Test chip submitted



Total of 7 small chips so far, all successful

All analog blocks have been silicon proven in test chips
ETROC2 FPGA emulator: has verified digital readout and system interfaces

ETROC2 was submitted on Oct 21, 2022
Testing on going since end of April 2023 …

Design team: FNAL/SMU/LBNL/UCSB
Testing team: FNAL/SMU/UIC/UCSB/Lisbon/IFAE with students from KSU/KU/CNU

in collaboration with lpGBT team for PLL,
With help from ETROC God Parent Committee, ***CERN ASIC Support & CHIPS for ETROC2***,
Torino/UCSC groups (sensor), and Barcelona group (bump bonding)

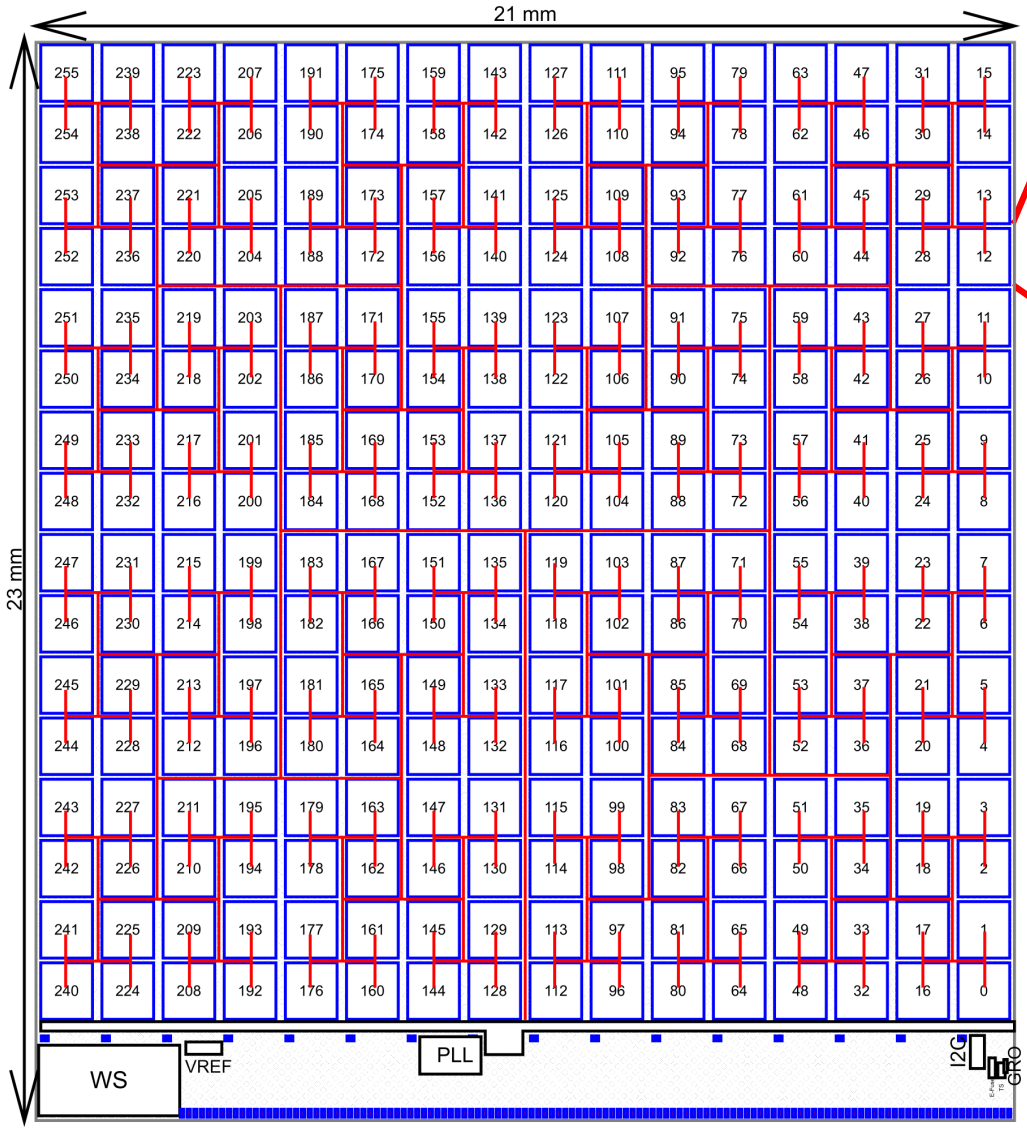
ETROC Overall Status

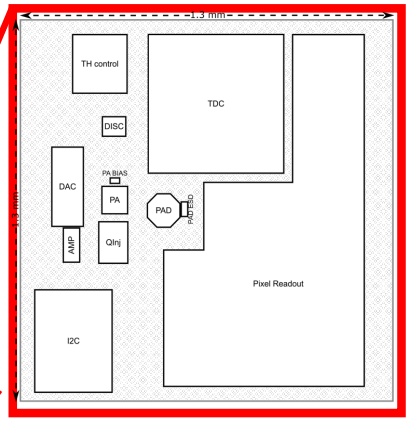
- ETROC0 (single channel, preamp + discriminator)
  - Charge injection/Cosmic/Laser done
  - TID test to 100Mrads done
  - Beam testing: ~30ps achieved in beam.
- ETROC1 (4x4), preamp + discriminator + new TDC (https://ieeexplore.ieee.org/document/9446843)
  - New TDC extensively tested: excellent performance and low power (<~6ps resolution)
  - Bare ETROC1 charge injection testing: excellent performance (~10ps resolution with charge injection)
  - ETROC1 and 5x5 LGAD sensor bump-bonded
    - ***Encountered noise related to 40MHz memory activity after bump bonding with sensor***
      - ***Noise source identified and understood, addressed in ETROC2 design***
    - ***Beam testing: results from beam telescope with LGAD at higher gain***
      - ***Obtained down to ~ 40ps per hit at system level in beam in 2021***
      - ***Second round of beam testing in 2022, results consistent***
  - *ETROC1 TID testing (not done, delayed due to COVID)*
- Towards ETROC2 (16x16): full size and full functionalities
  - ETROC PLL mini-ASIC (with lpGBT PLL core)***: test results very good, including SEU***
  - Waveform Sampler prototypes and I2C test chip works well.
  - ETROC2 emulator (for pixel and global readout) works well
- ***ETROC2 design submitted in Oct 2022, testing started April 2023***
- ETROC3: intended as final version, submission in 2024

→ ***Due to limited time, this talk will only have few highlights***

Recent talk at FEE 2023:
https://agenda.infn.it/event/36206/contributions/202630/attachments/106846/150691/ETROC.pdf

ETROC2 design: most building blocks have been silicon proven

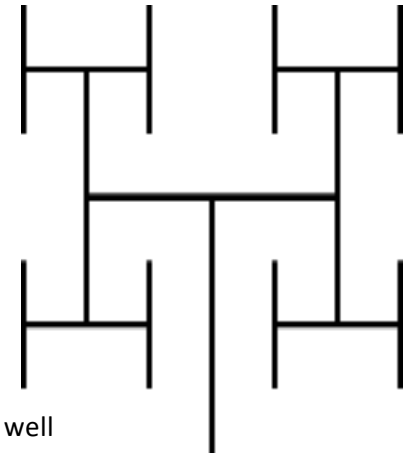




Front-end:
Charge injection/DAC
Preamp,
Discriminator
TDC

All tested in ETROC0/1,
and reused in ETROC2

- PLL
  - PLL is based on lpGBT and validated with PLL test chip (+SEU)
- I2C
  - I2C design validated with I2C test chip, including SEU
  - In-pixel I2C register expanded and verified
- TS (Temp Sensor)
  - TS validated with I2C test chip
- Efuse
  - Efuse validated with I2C test chip
- VREF
  - VREF validated with I2C test chip
- GRO
  - Reusing the GRO in ETROC1
- Tx and Rx
  - reusing Tx in ETROC1
  - Reusing Rx in ETROC1(from lpGBT)
- WS (Waveform Sampler)
  - Rad-hard version tested and works well
- In-pixel threshold calibration
  - tested with ETROC0 via FPGA emulator



All critical analog building blocks have been silicon proven in testing chips,
and the digital building blocks have been emulated in FPGA and tested with the downstream readout board with backend.

ETROC2 key features: from testing/user point of view

Initial testing almost done, bare ETROC2 is functional well

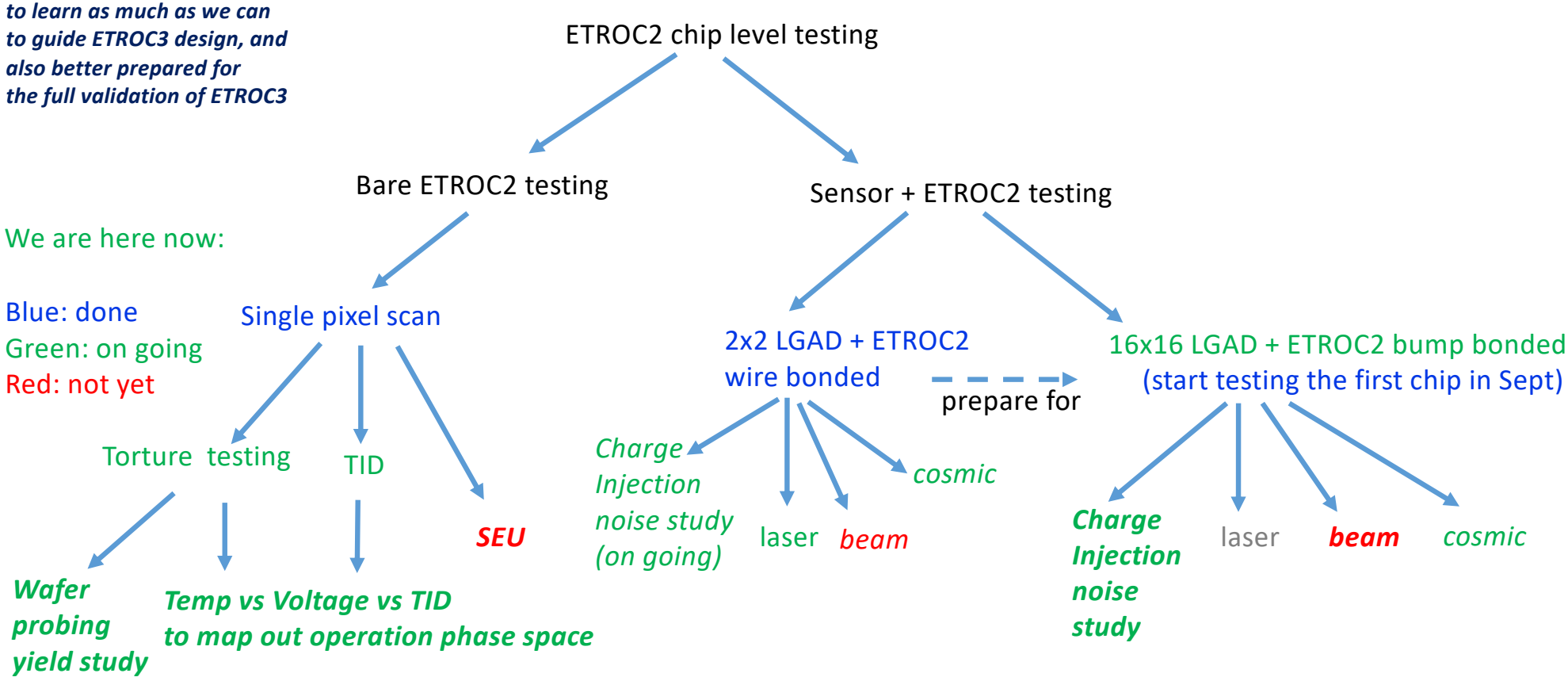
five months into testing so far,
a lot has been done, still a long way to go

- Self-test pattern generator (works well)
  - Can be used to test the digital data flow and link interfaces. Users can dial the occupancy of pixels and change patterns
    - This feature has been used extensively to simulate and verify the readout design of ETROC2, at RTL level and post layout stage
    - First thing user can test with ETROC2 emulator, the same test can then be done for bare ETROC2 and bump bonded ETROC2
    - At chip level (as *build in self-testing capability*), board level, and system level (with DAQ backend)
- Testing with charge injection (single pixel scan looking good, cluster torture testing in progress)
  - *Test the full path from charge injection to preamp to discriminator to TDC to circular buffer to event buffer to global digital readout*
  - Discriminator threshold scan and jitter measurements (bare ETROC2 first, then bump bonded ETROC2)
  - User can define the window for TOA, TOT and CAL to filter/suppress hits before readout
  - User adjustable TOA measurement window (up to 12.5ns, 11.4ns effective)
  - Each pixel can be enabled or disabled for DAQ readout
  - The relative phases adjustable between the TDC clock, pixel readout clock and global readout clock
- ***ETROC2 testing with LGAD sensor, laser, source and then beam (on going)***
  - Full path timing performance study including LGAD
- Auto-threshold scan within pixel (single pixel scan looks ok) https://iopscience.iop.org/article/10.1088/1748-0221/16/09/T09006
  - This new feature will be studied first by dedicated ETROC2 chip level testing
- ***Trigger path (useful for beam testing as self-triggering)***
  - Can be used for monitoring purpose initially, a coarse map of user defined hits continuously sent out every BC
  - Can be used for self triggering for beam test if so desired, user can define the window for TOA, TOT and CAL for triggered hit
  - Use flashing bits in empty BCID (beam gap), defined via I2C. Can be used as cross check and monitoring purpose.
- Waveform Sampler (initial test look ok, *charge injection testing on going*)
  - Able to record waveform of one pixel up to 16 bunch crossing (400 ns), start and stop controlled via fast command, readout via I2C
  - power-down when not used, intend to use for monitoring purpose during detector operation
- Power consumption estimate is ~1W per chip, being confirmed with ETROC2 chips (initial testing looks ok, detailed study after/with torture testing)

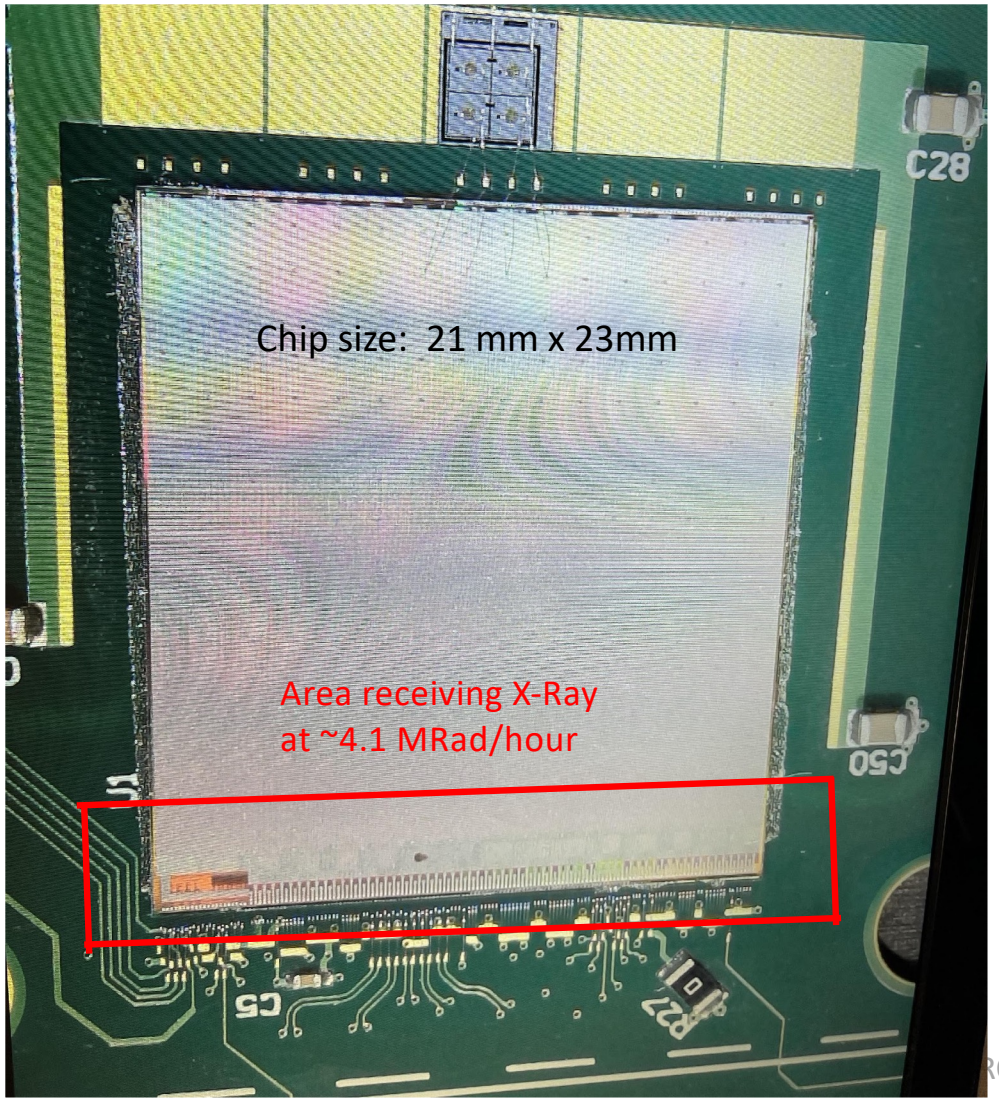
Will not have time to show the details of functional testing results in this talk,
only few highlights on TID, V-T scan and initial results with sensor ….

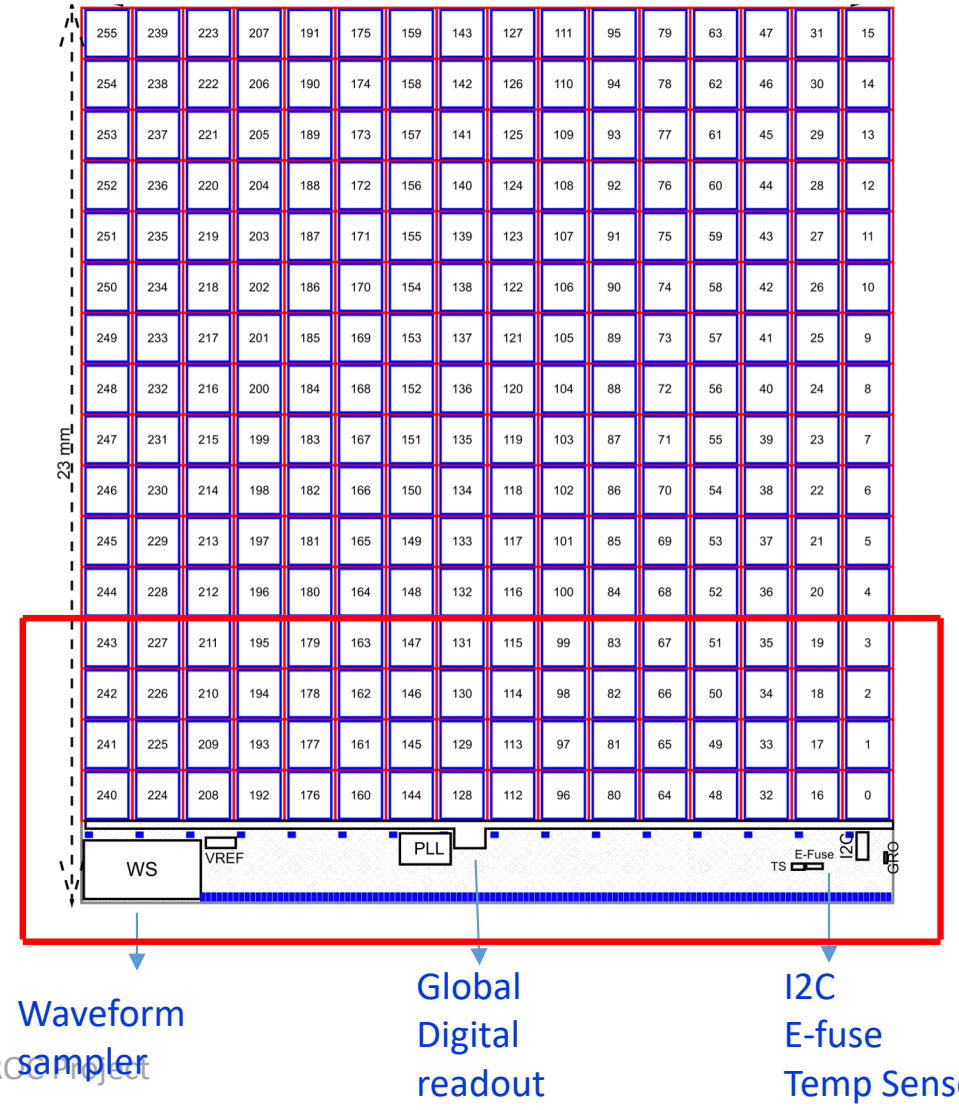
ETROC2 chip level testing road map

ETROC2 is a learning chip, need to learn as much as we can to guide ETROC3 design, and also better prepared for the full validation of ETROC3



TID testing at CERN





Waveform sampler

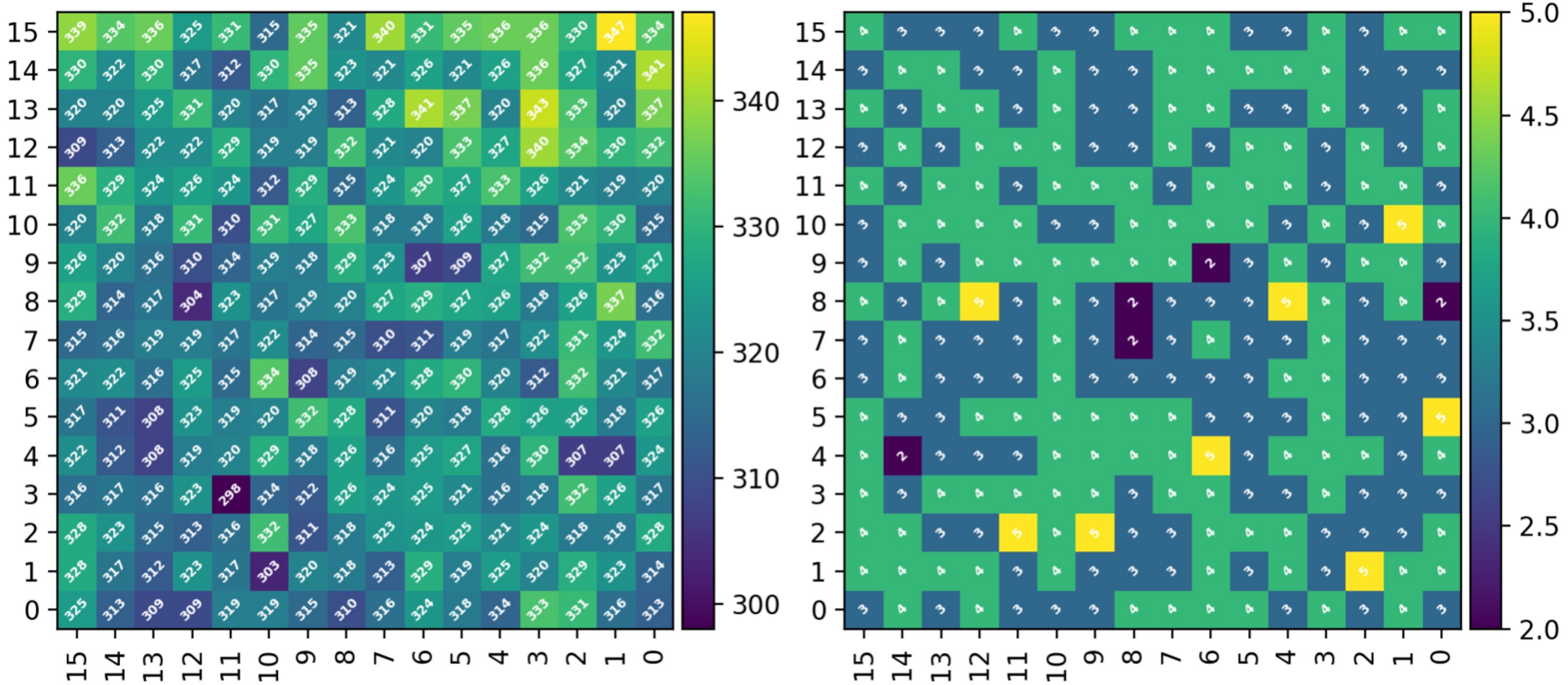
Global Digital readout

I2C E-fuse Temp Sensor

02D5-12 Before TID @ Room Temperature
2023-08-08 08:37

Baseline and noise width from
in-pixel automatic threshold scan
(very fast, to map out 16x16 array)

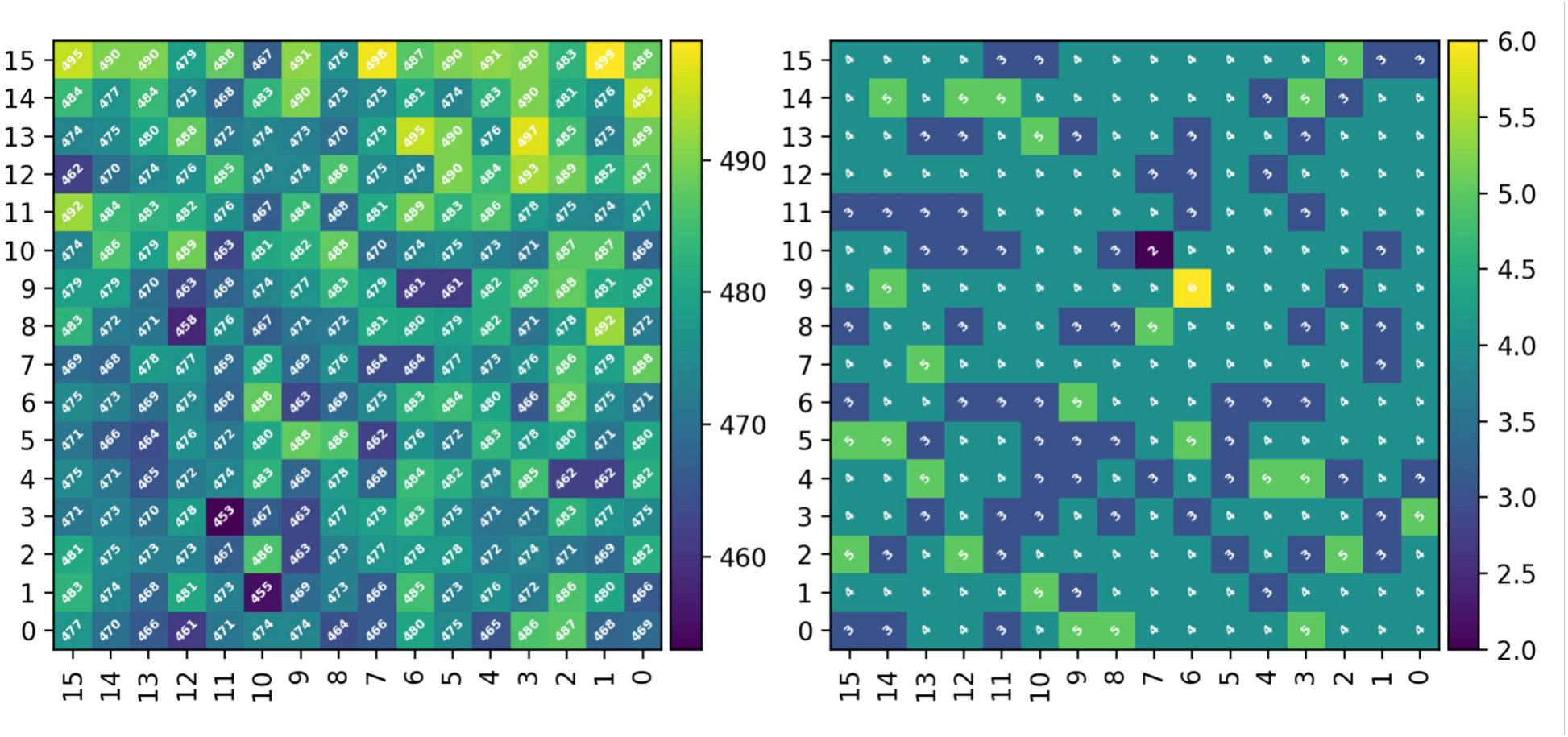
https://iopscience.iop.org/article/10.1088/1748-0221/16/09/T09006



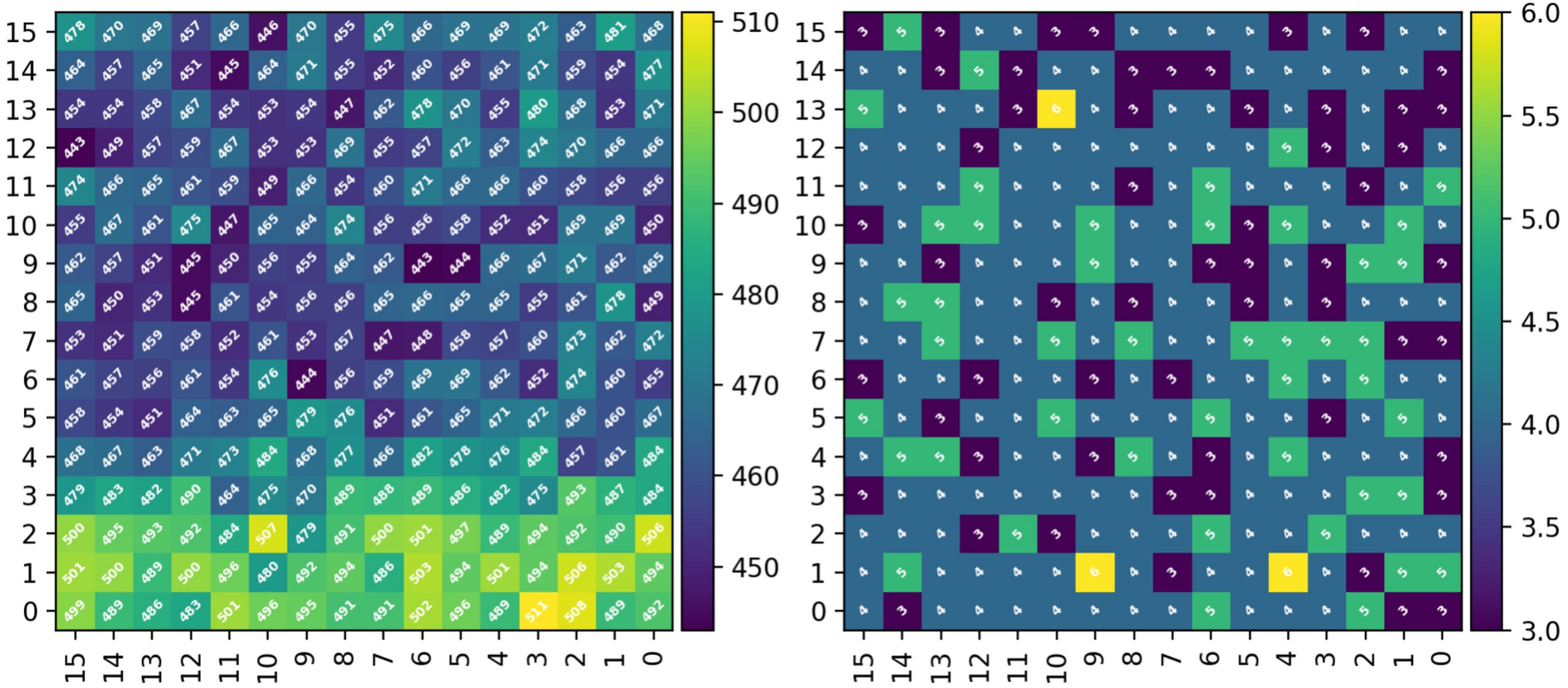
02D5-12 Before TID @ -30C
2023-08-08 12:24

From 24C to -30C: 54C change
simulation for baseline shift expected:
2.75/C x 54 ~ 150.

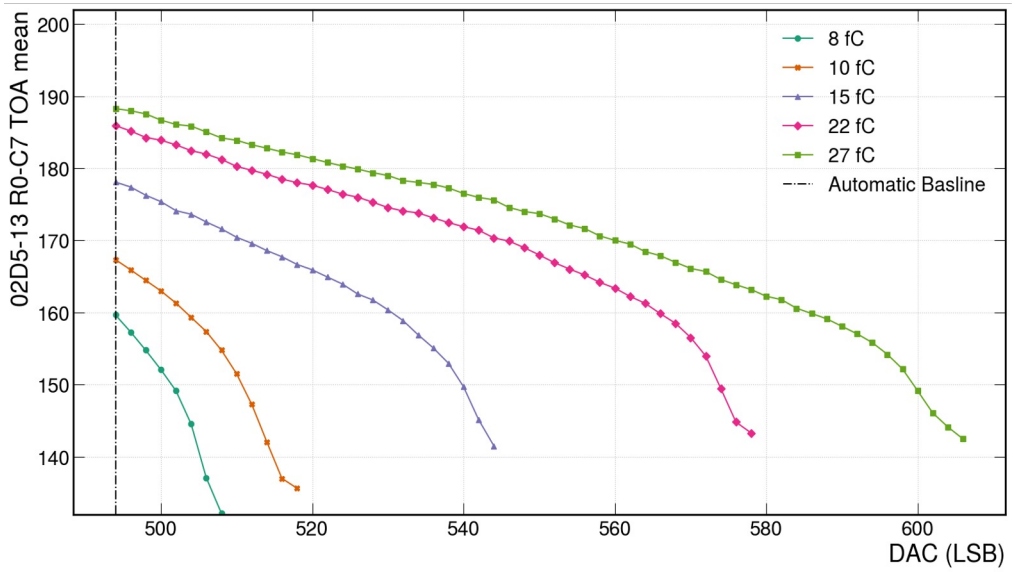
The simulation agrees with the measurements

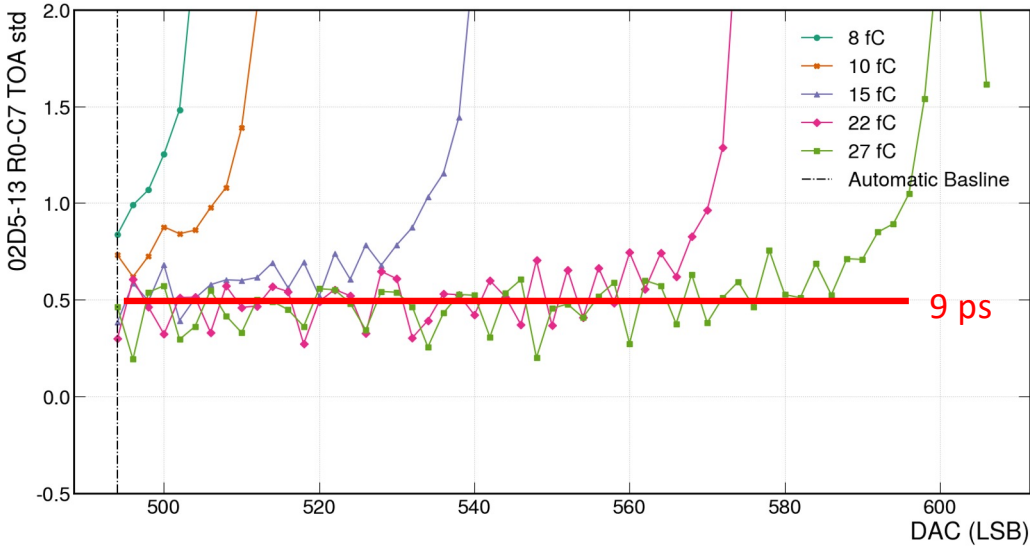


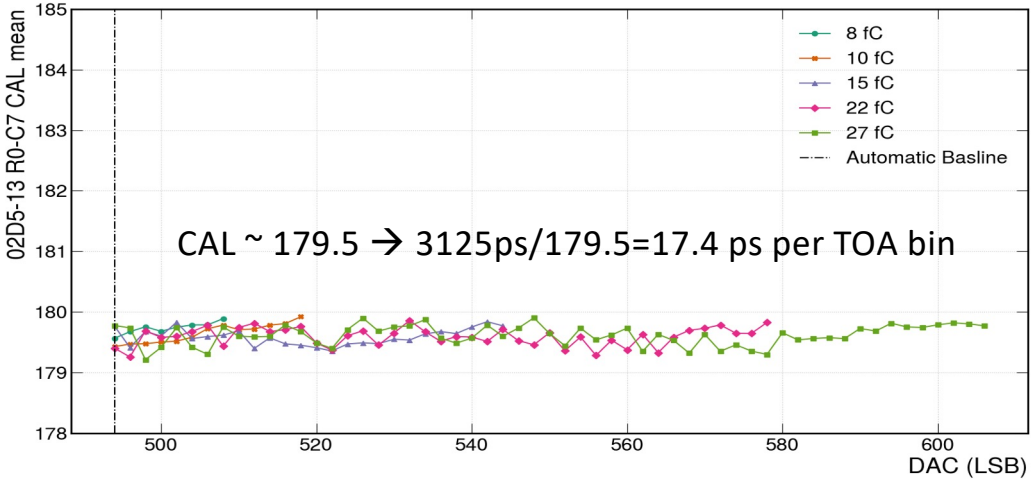
02D5-12 End of TID @ -30C, 200MGrad
2023-08-10 16:20



Charge vs DAC scan after 200 Mrad





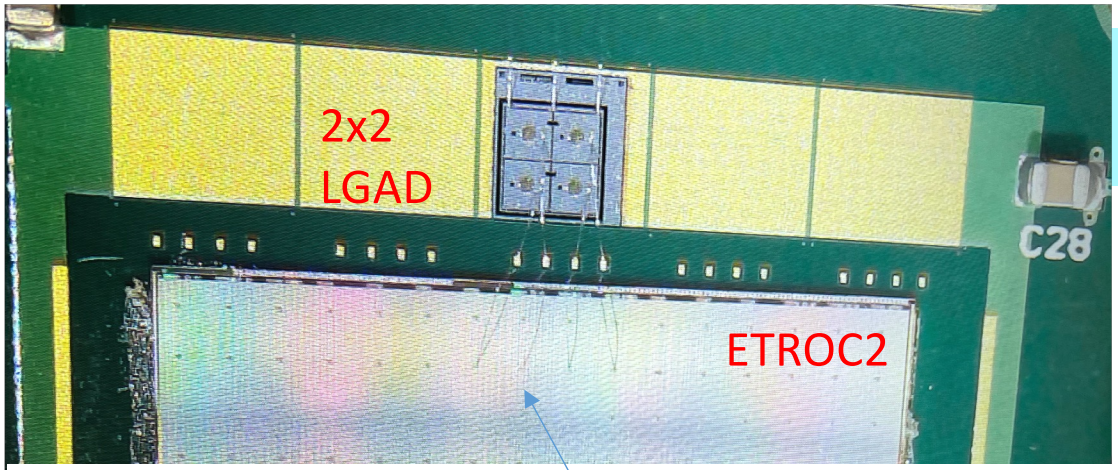


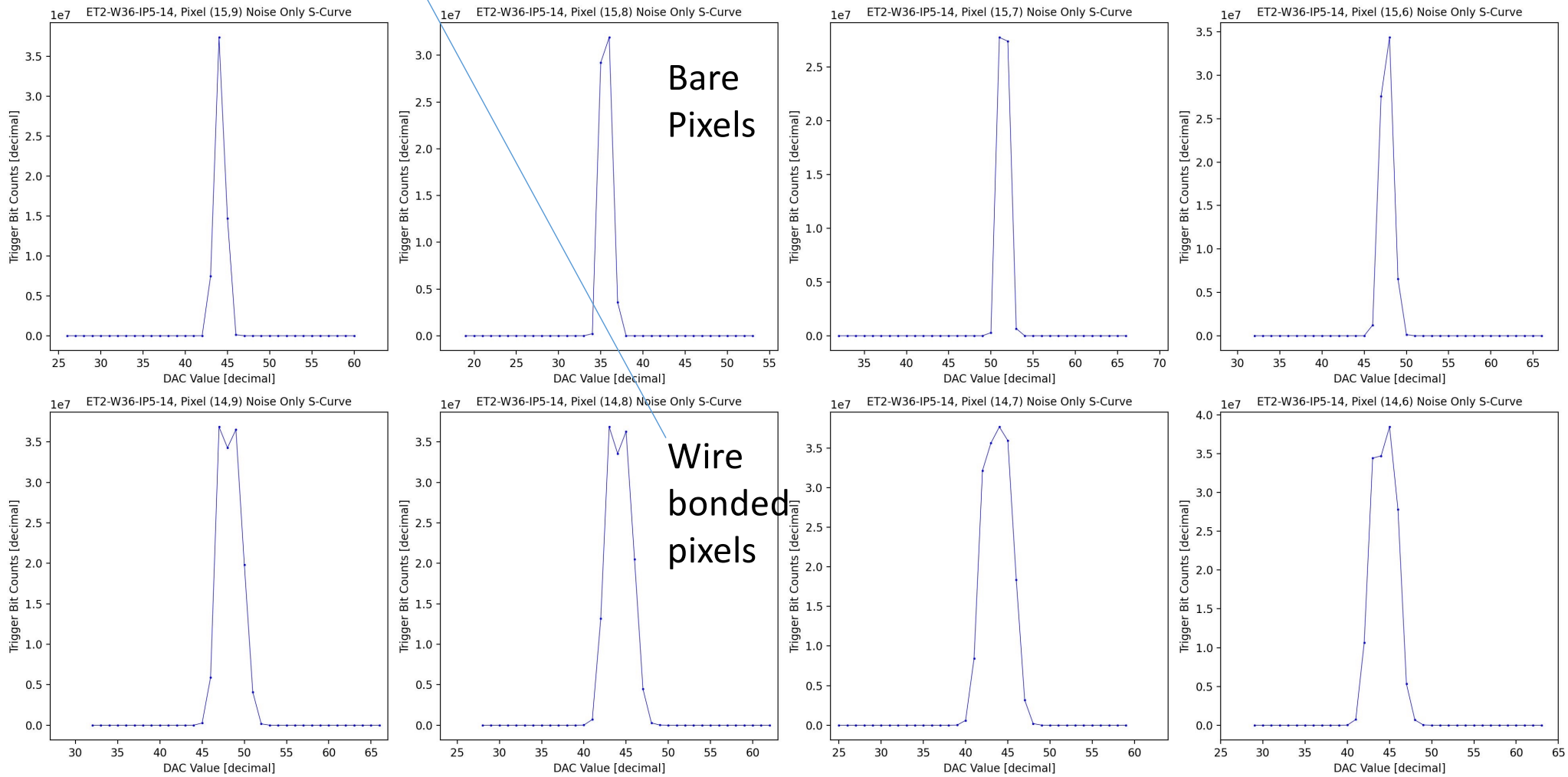
Temperature vs Voltage vs TID scan done at CERN in Aug 2023

T: from -30C too +30C
V: from 1.3V to 1.0V
TID: from 0 to 200 Mrad

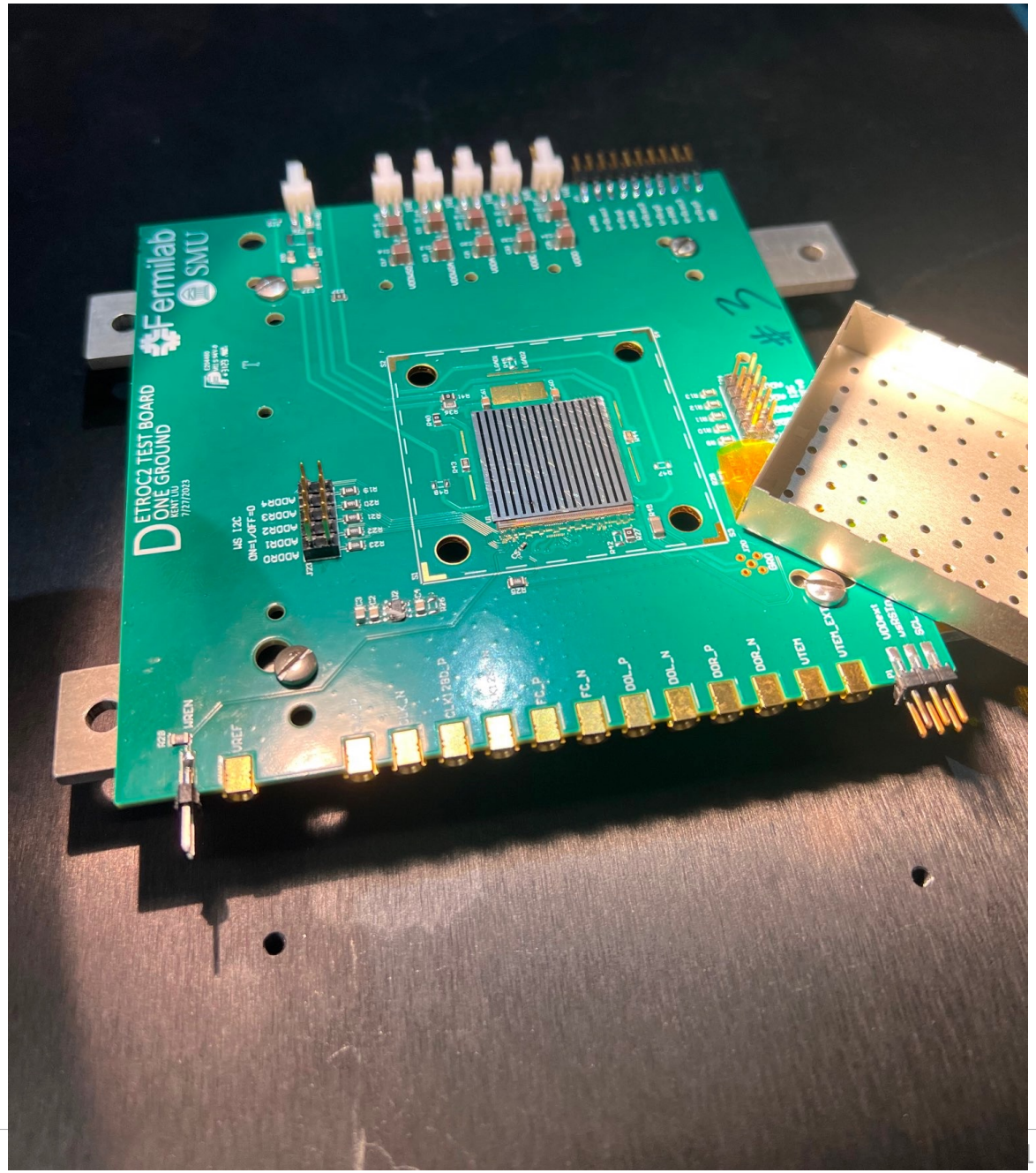
All works

Testing with 2x2 sensor wire bonded



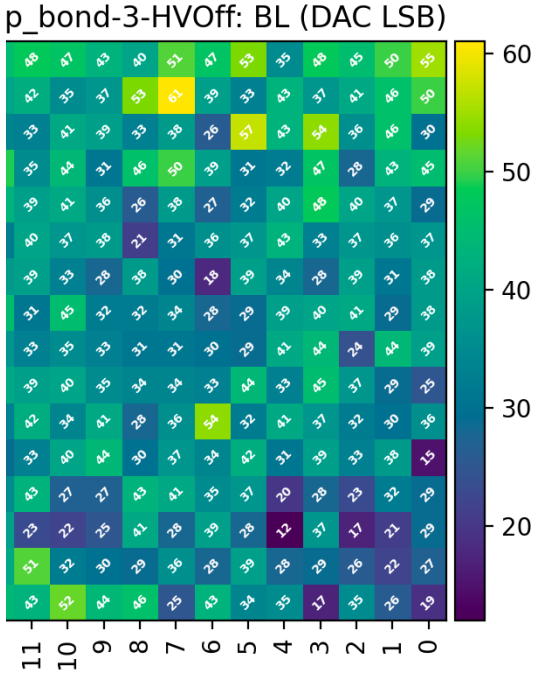


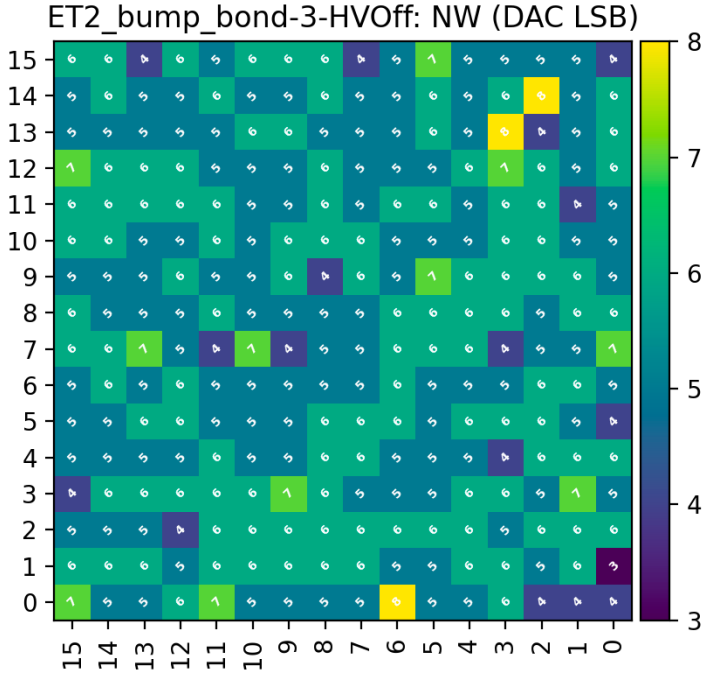
Very first bump bonded ETROC2

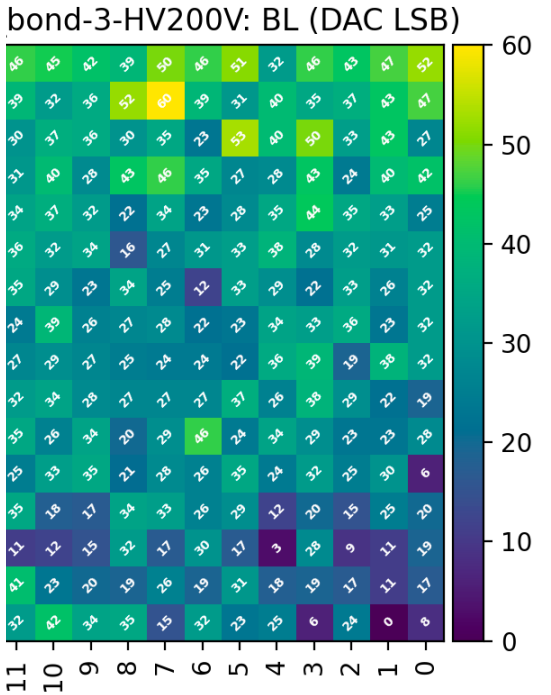


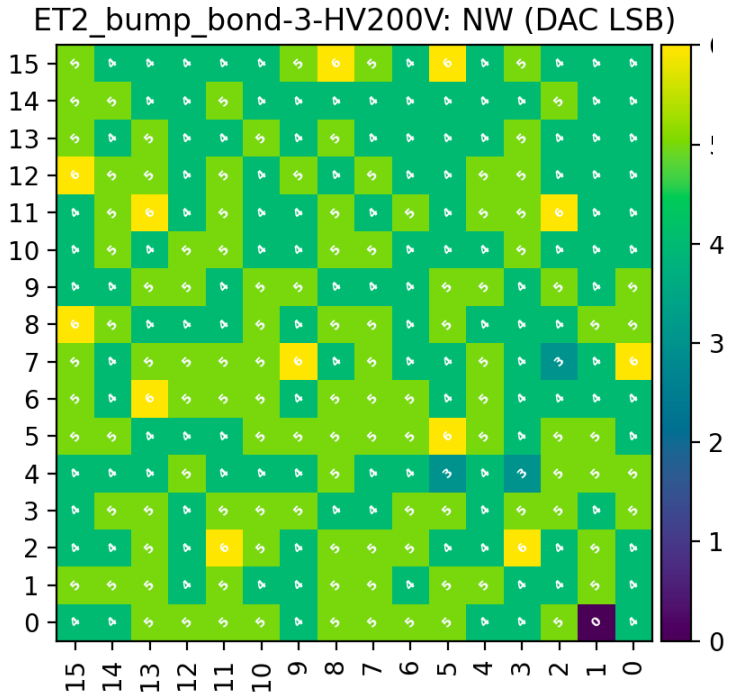
With ETROC2 chip from FFF corner Wafer

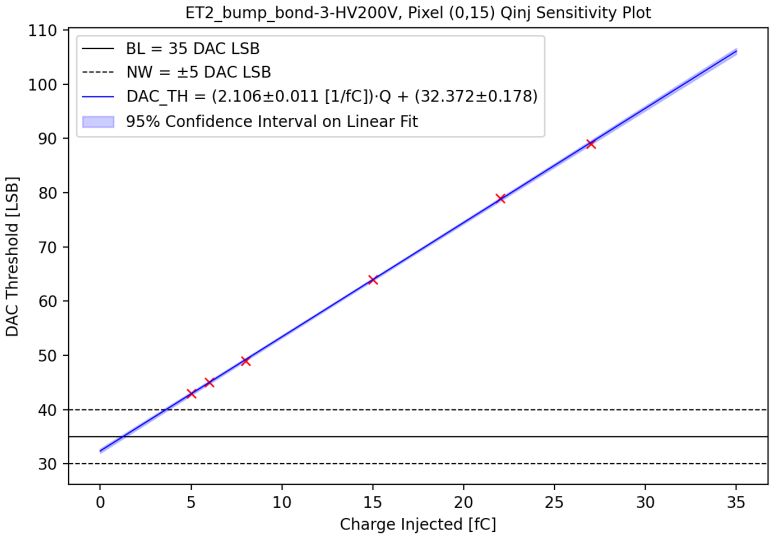
Testing started Early Sept 2023 …


p_bond-3-HVOff: BL (DAC LSB)

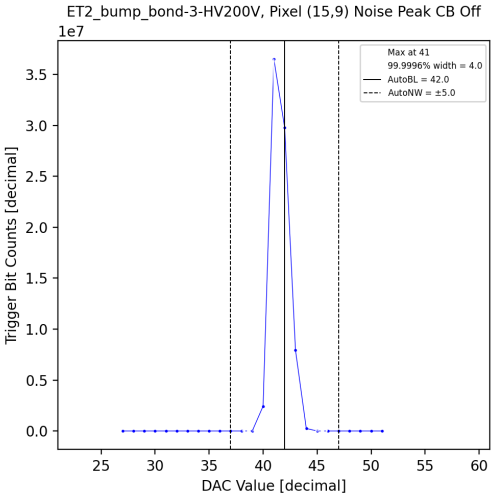

ET2_bump_bond-3-HVOff: NW (DAC LSB)

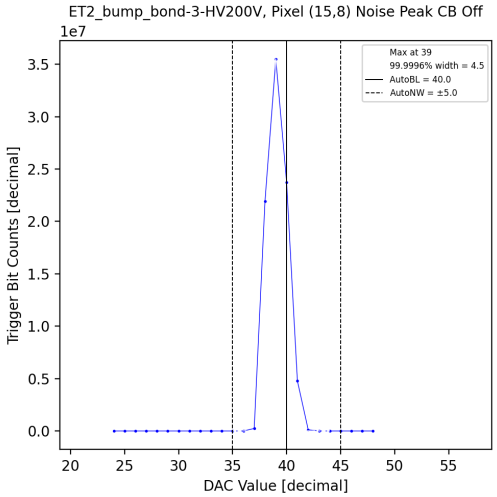

bond-3-HV200V: BL (DAC LSB)

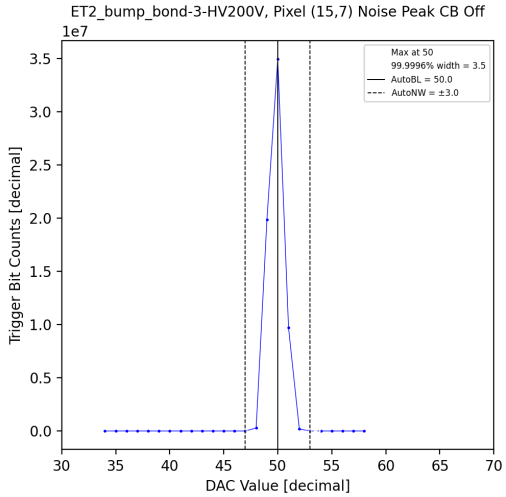

ET2_bump_bond-3-HV200V: NW (DAC LSB)

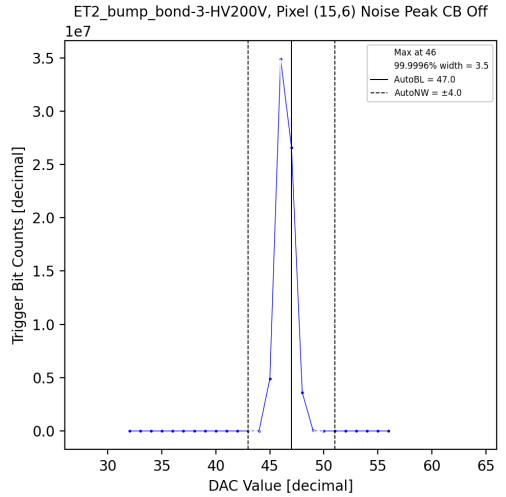

ET2_bump_bond-3-HV200V, Pixel (0,15) Qinj Sensitivity Plot
BL = 35 DAC LSB
NW = ±5 DAC LSB
DAC_TH = (2.106±0.011 [1/fC])·Q + (32.372±0.178)
95% Confidence Interval on Linear Fit
DAC Threshold [LSB]
Charge Injected [fC]

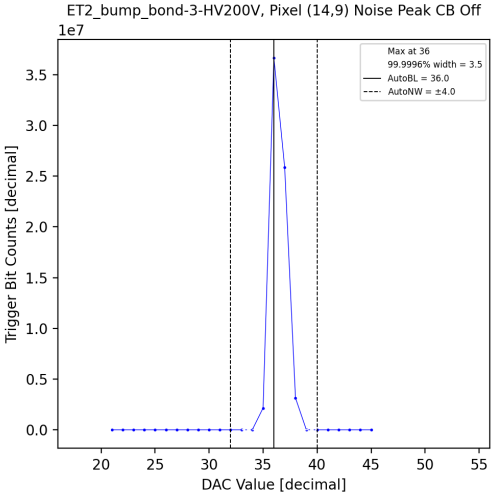
Bump bonded ETROC2

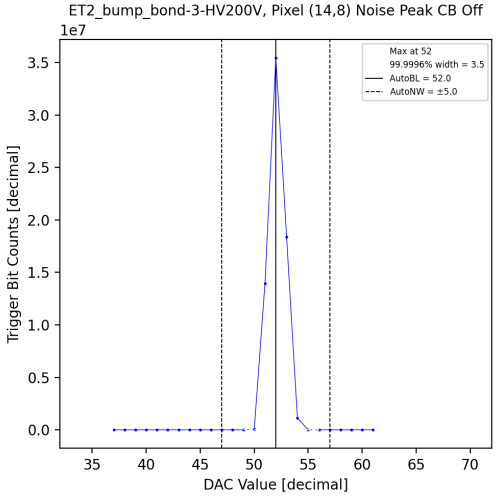


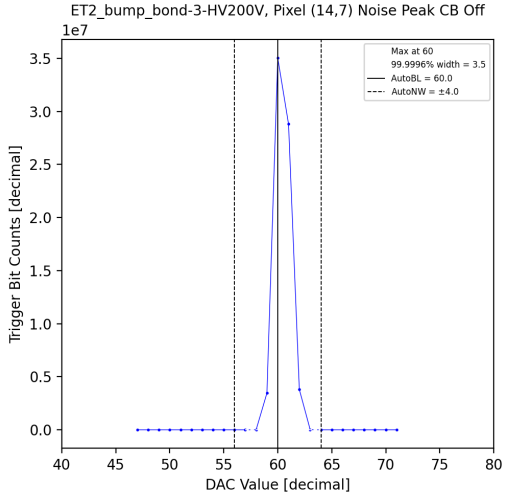


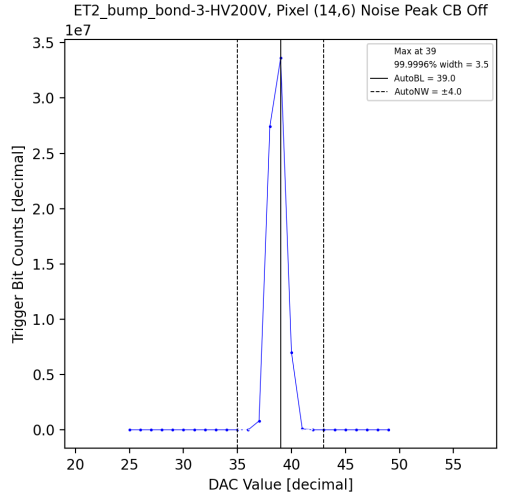




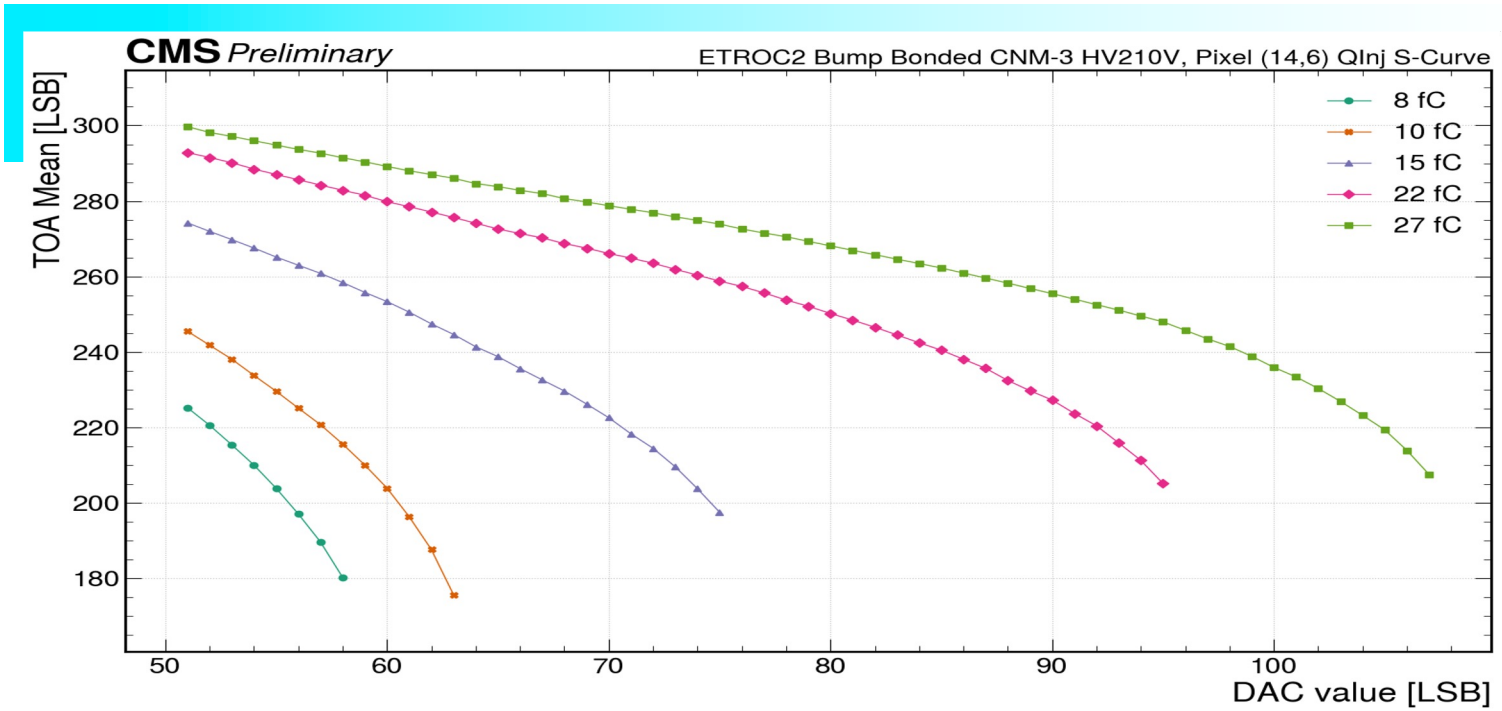


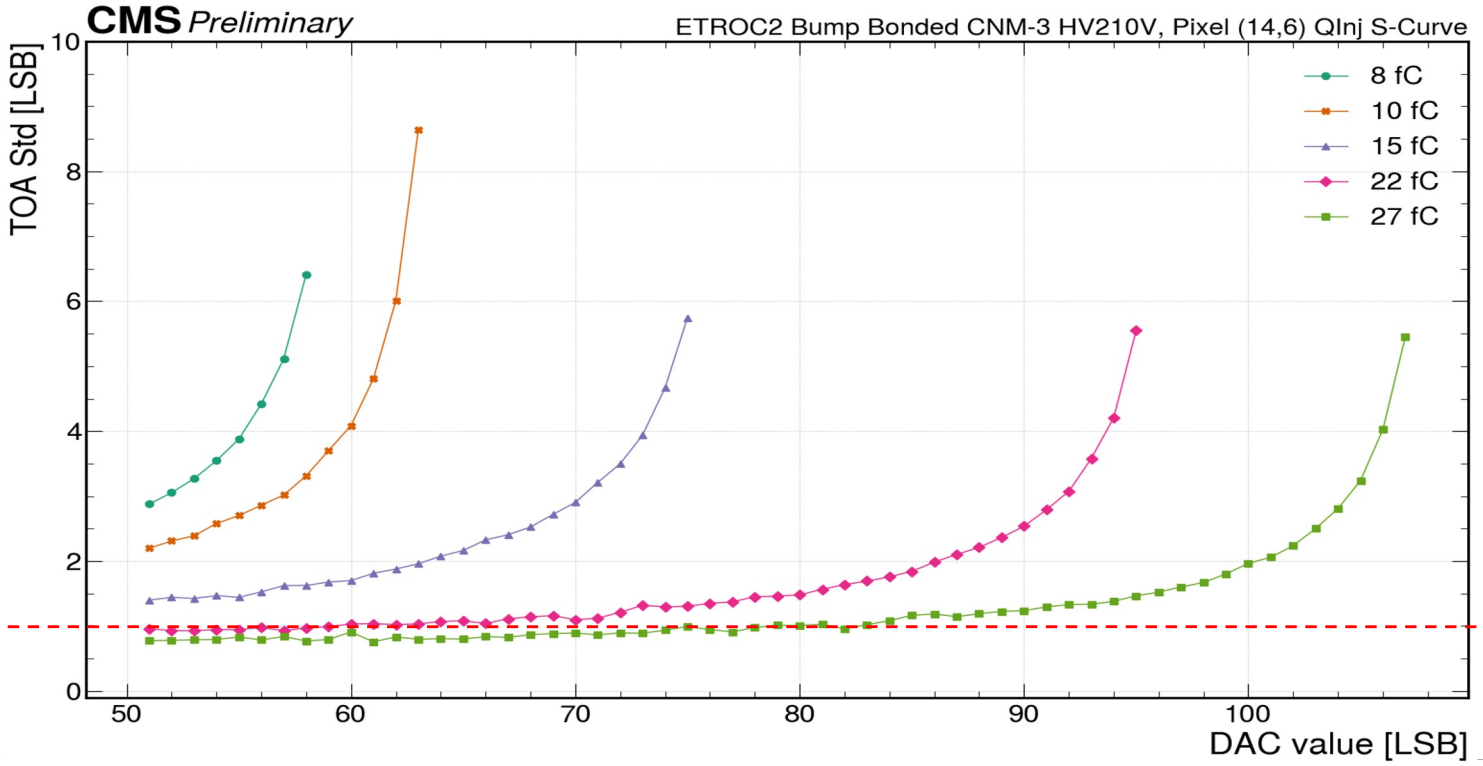




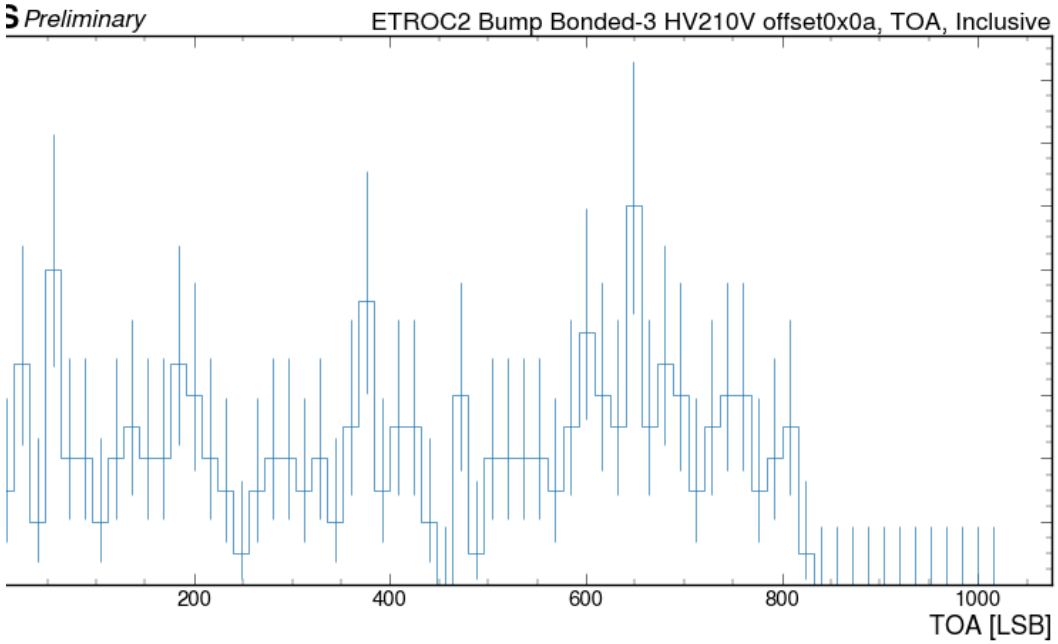


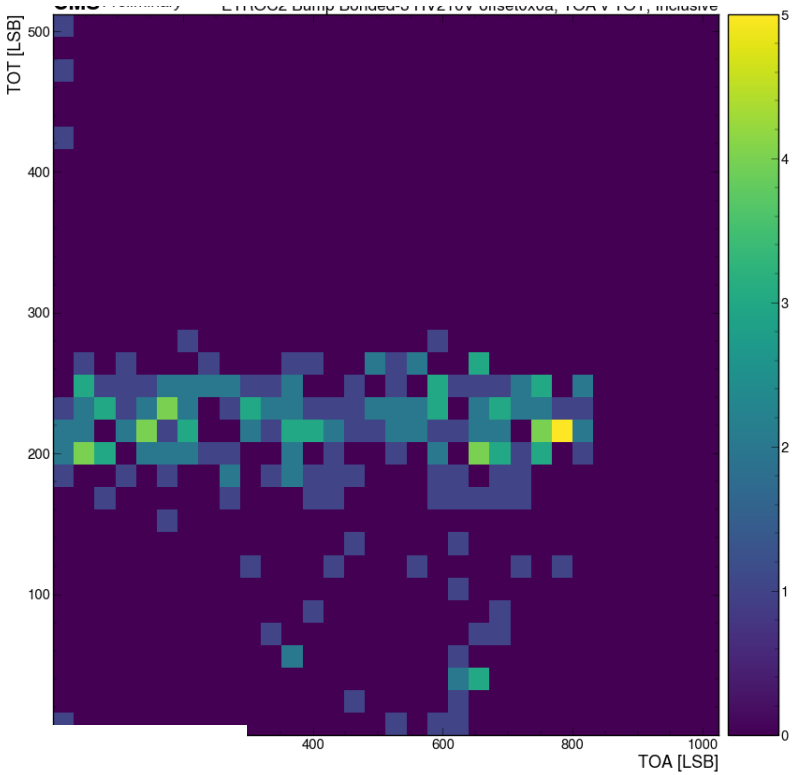
CAL ~207
TOA bin=15ps

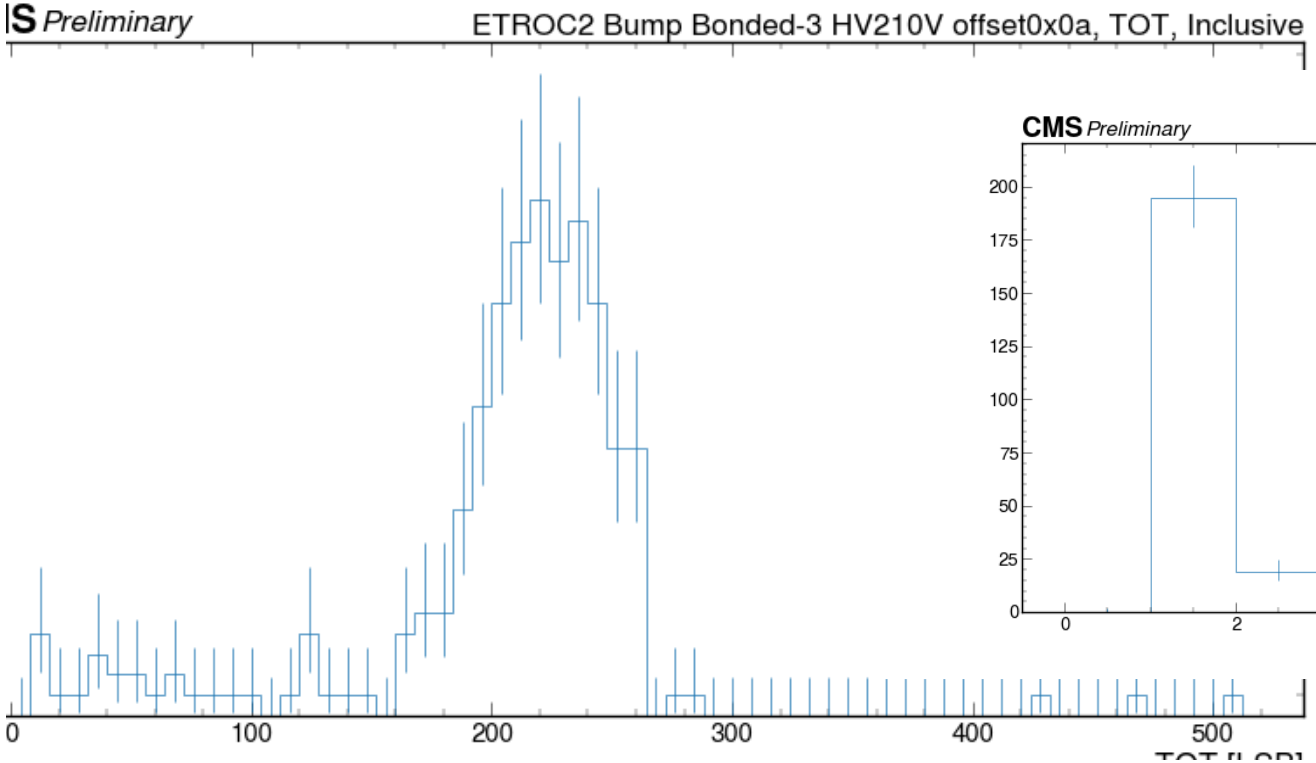


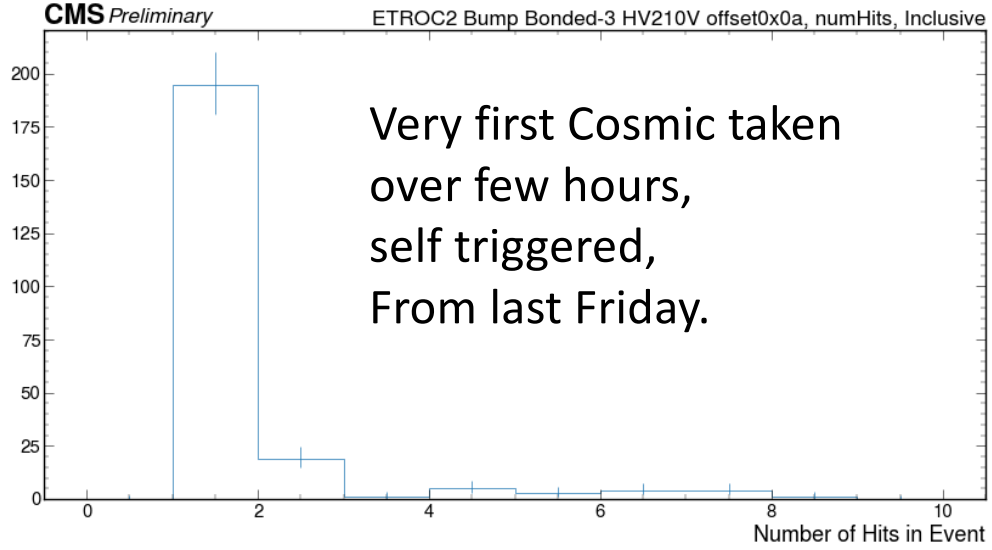


15ps line





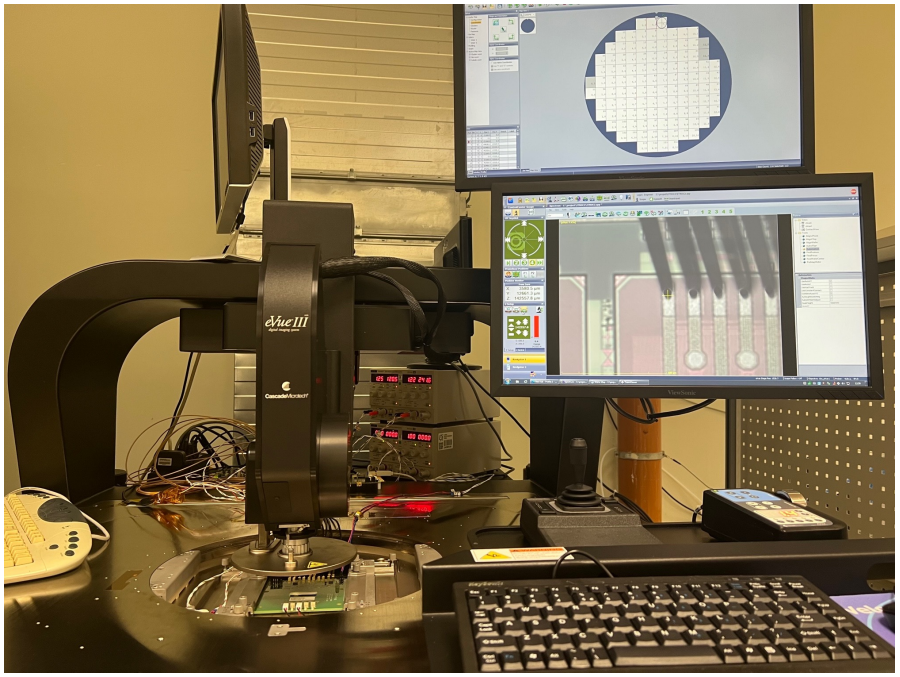


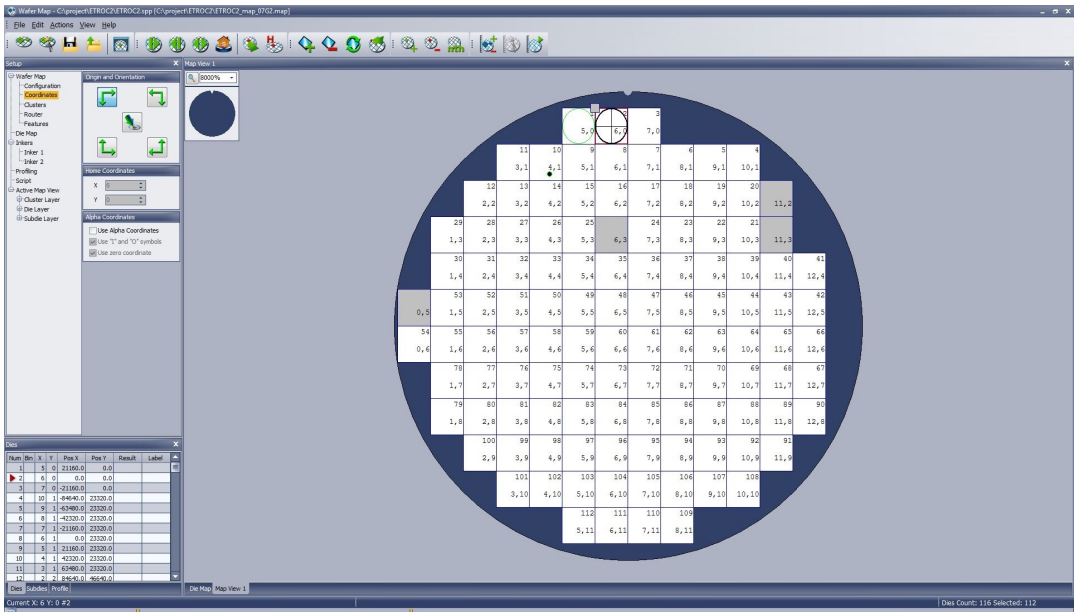


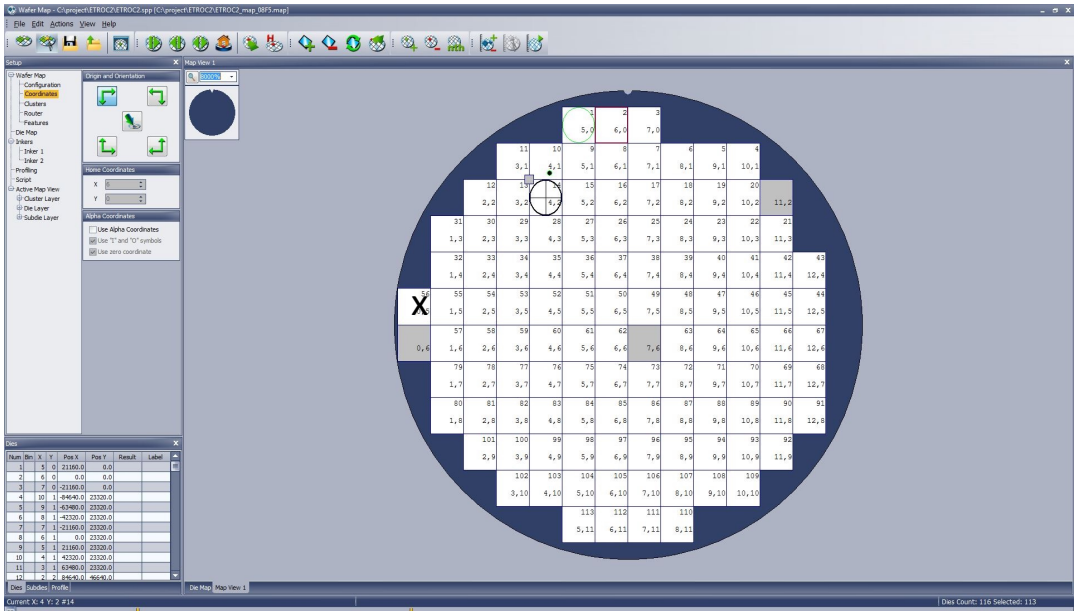
Very first Cosmic taken over few hours, self triggered, From last Friday.

Wafer probe testing for ETROC2 wafers

Setup at CERN



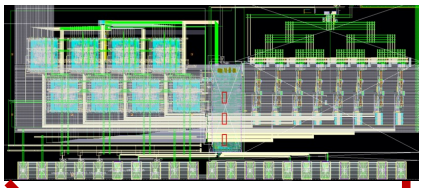


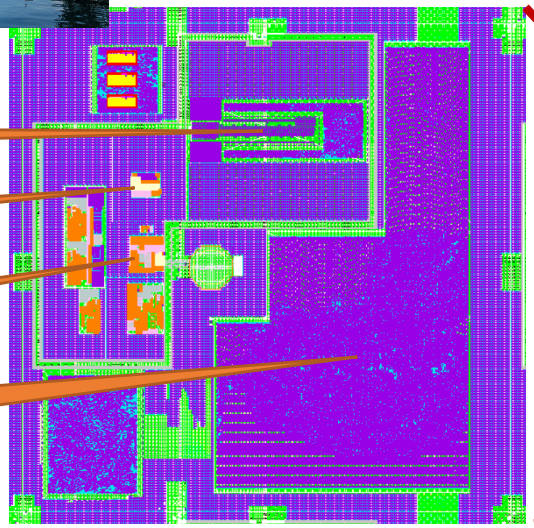


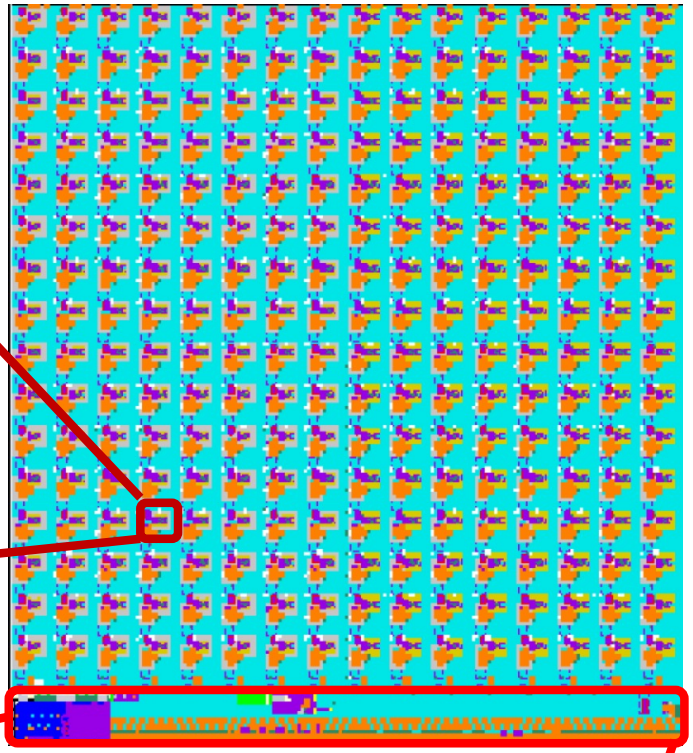
Two new ETROC2 wafers from TSMC
Arrived CERN in Aug 2023

probe testing shows 4 bad dies (out of 116 dies) per wafer in each case

ETROC2 layout (submitted on Oct 21, 2022)



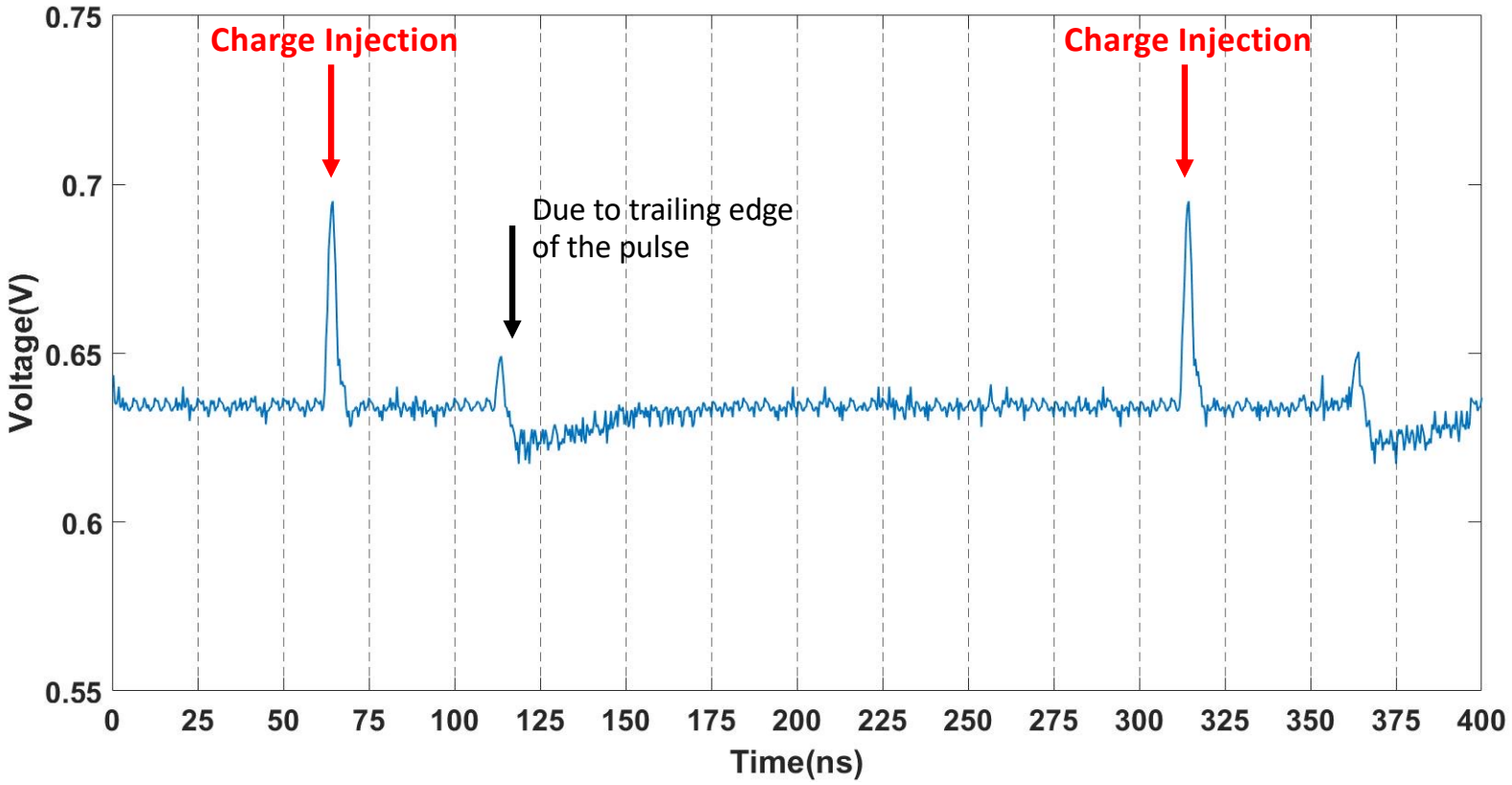




Waveform Sampler

Waveform sampler is intended for monitoring purpose only, power down if not in use.

Waveform Sampler recorded Waveform



400ns of waveform recorded in WS memory

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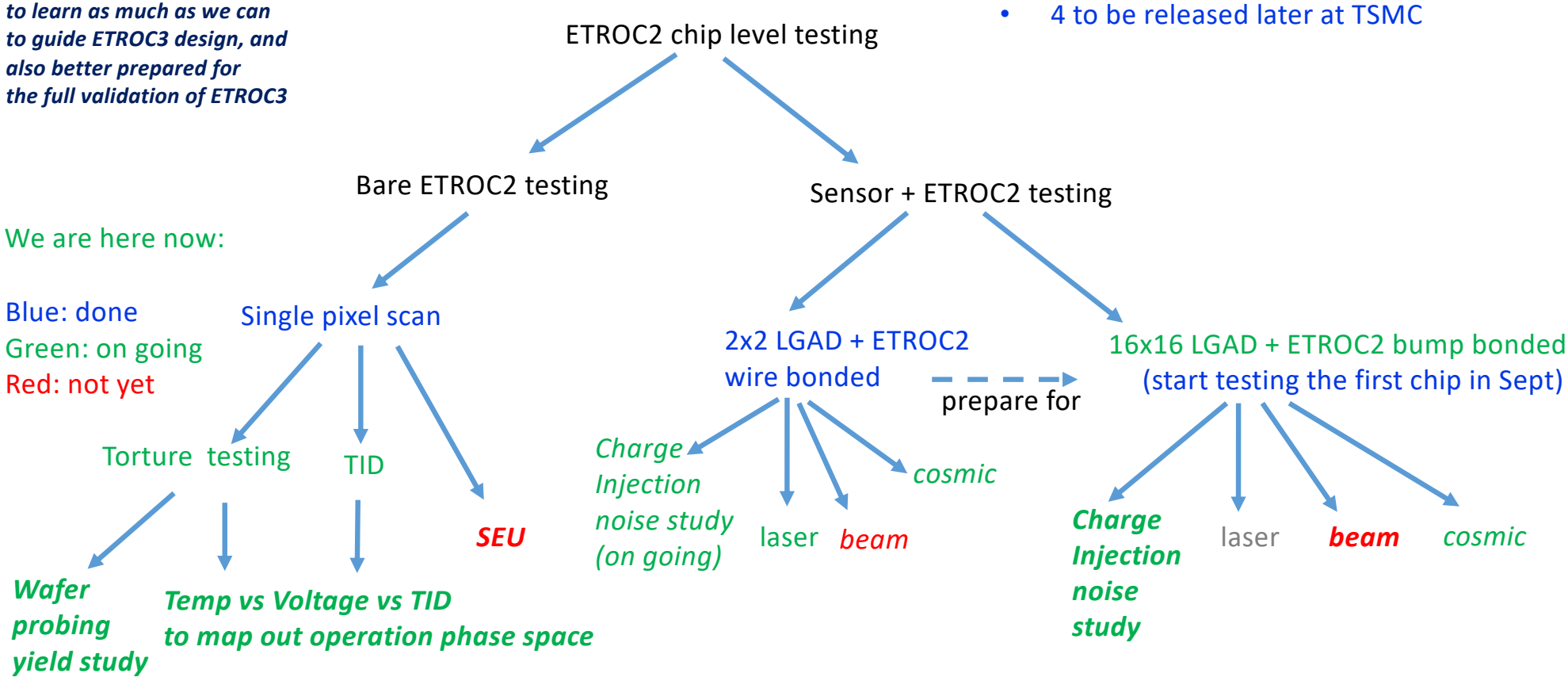
ETROC2 chip level testing road map

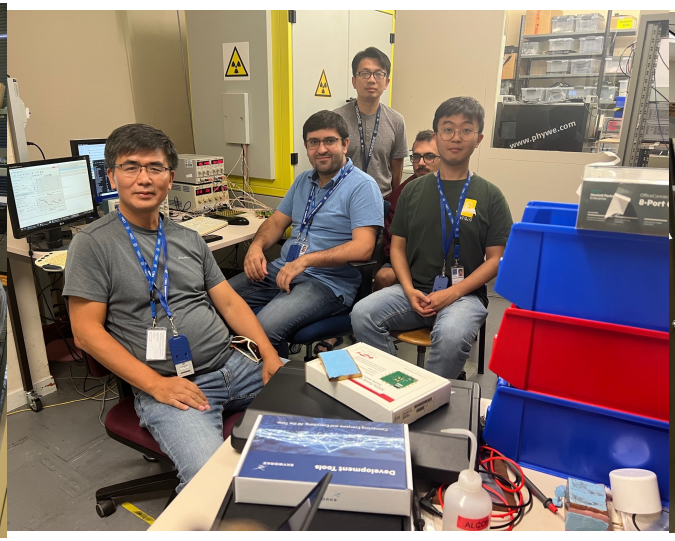
- Total of 6 wafers on hold at TSMC
- 2 new wafers released from TSMC in Aug
  - Being processed by Pactech
- 4 to be released later at TSMC

ETROC2 is a learning chip, need to learn as much as we can to guide ETROC3 design, and also better prepared for the full validation of ETROC3

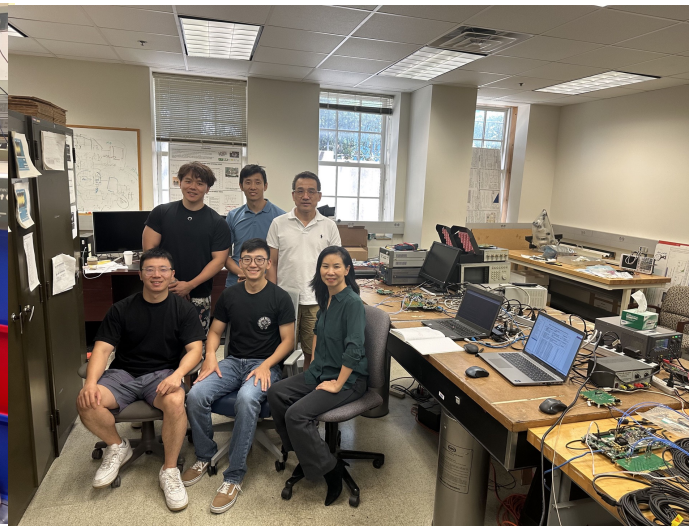


ETROC2 testing team in Aug 2023

At FNAL 14th floor teststand



At CERN X-Ray machine room (ObeliX)



at SMU (Physics + EE)

People not shown in photos but helped behind the scene:
Quan Sun in Dallas
Sergei Los
Jonathan Hollar
Diego Figueriedo
Ivan Vila
Roberta Arcidiacono
Marcos Fernandez Garcia
…

Great help and support from CERN:
Alessandro Caratelli
Giulio Borghello
Jerome Alexandre Alozy …
Maxence Marc Ledoux

Extensive work has been done over the past two months to prepare for the testing at CERN in Aug (and in Sept)

Summary

- CMS Endcap Timing Layer is being developed for HL-LHC upgrade
  - One of the first generation LGAD-based precision timing detectors for HL-LHC
  - Goal is to reach ~35 ps per track with two layers (<~50 ps per hit)
- ETROC2 is the first full size full functionality prototype ASIC
  - Designed as if it were the final version, from functionality point of view
    - ***Initial ETROC2 testing results looking promising***
      - ***Extensive performance study on going***
      - ***Initial beam test at CERN in Sept and DESY in Dec***
- ETROC3
  - The same functionalities as ETROC2, with improvements based on what will be learned from extensive ETROC2 testing
  - Submission scheduled for 2024

For technical details, please see ETROC papers and recent talks.

Characterization of the CMS Endcap Timing Layer readout chip prototype with charge injection

https://iopscience.iop.org/article/10.1088/1748-0221/16/06/P06038

The Analog Front-end for the LGAD Based Precision Timing Application in CMS ETL

https://arxiv.org/abs/2012.14526

In-pixel automatic threshold calibration for the CMS Endcap Timing Layer readout chip

https://iopscience.iop.org/article/10.1088/1748-0221/16/09/T09006

FERMILAB-CONF-20-549-E

A New Scheme of Redundant Timing Crosschecking for Frontend Systems

https://ieeexplore.ieee.org/document/9447027

A 2.56 GS/s 12-bit 8x-Interleaved ADC with 156.6 dB FoMS in 65 nm CMOS

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A Low-Power Time-to-Digital Converter for the CMS Endcap Timing Layer (ETL) Upgrade

https://ieeexplore.ieee.org/document/9446843

2022 TWEPP talks related to ETROC:

From ETROC1 to ETROC2:

https://indico.cern.ch/event/1127562/contributions/4904521/ (***TWEPP 2022***, Tuesday)

ETROC Emulator:

https://indico.cern.ch/event/1127562/contributions/4904781/ (***TWEPP 2022***, Wed)

ETROC Waveform Sampler:

https://indico.cern.ch/event/1127562/contributions/4904540/ (***TWEPP 2022***, Thursday)

TDC with Uncontrolled Delay lines: calibration approach and method

https://indico.cern.ch/event/1127562/contributions/4904530/ (***TWEPP 2022***, Thursday)