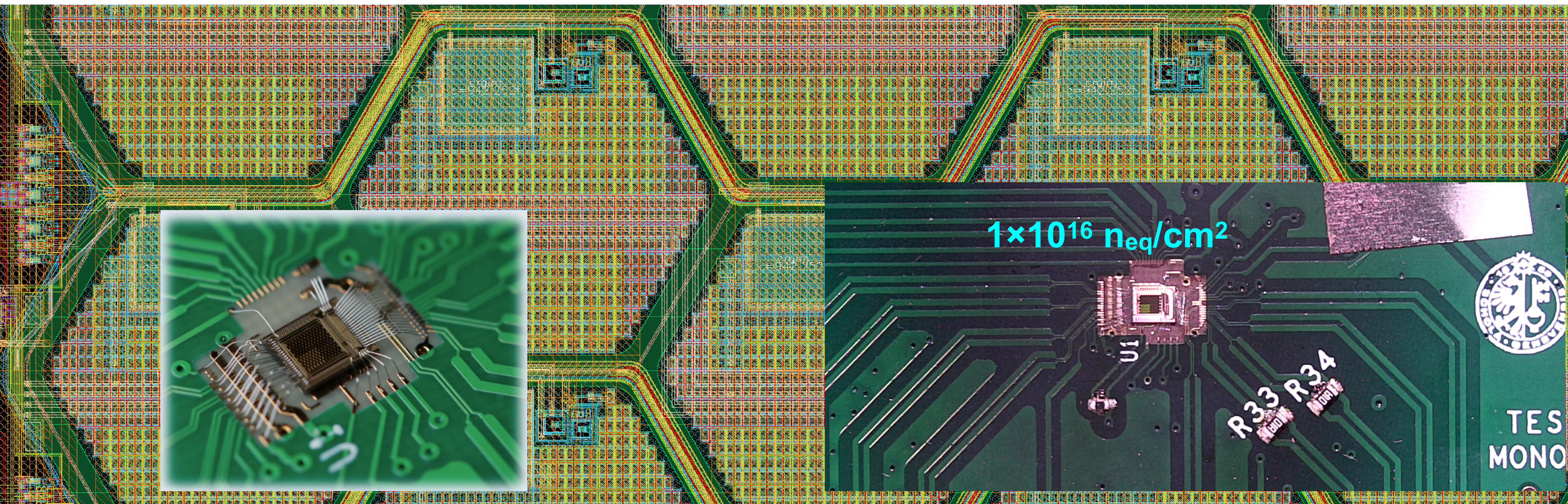


The **MONOLITH** project: towards **picosecond timing** with monolithic silicon

Giuseppe Iacobucci — Université de Genève



**UNIVERSITÉ
DE GENÈVE**



**Swiss National
Science Foundation**



European Research Council
Established by the European Commission

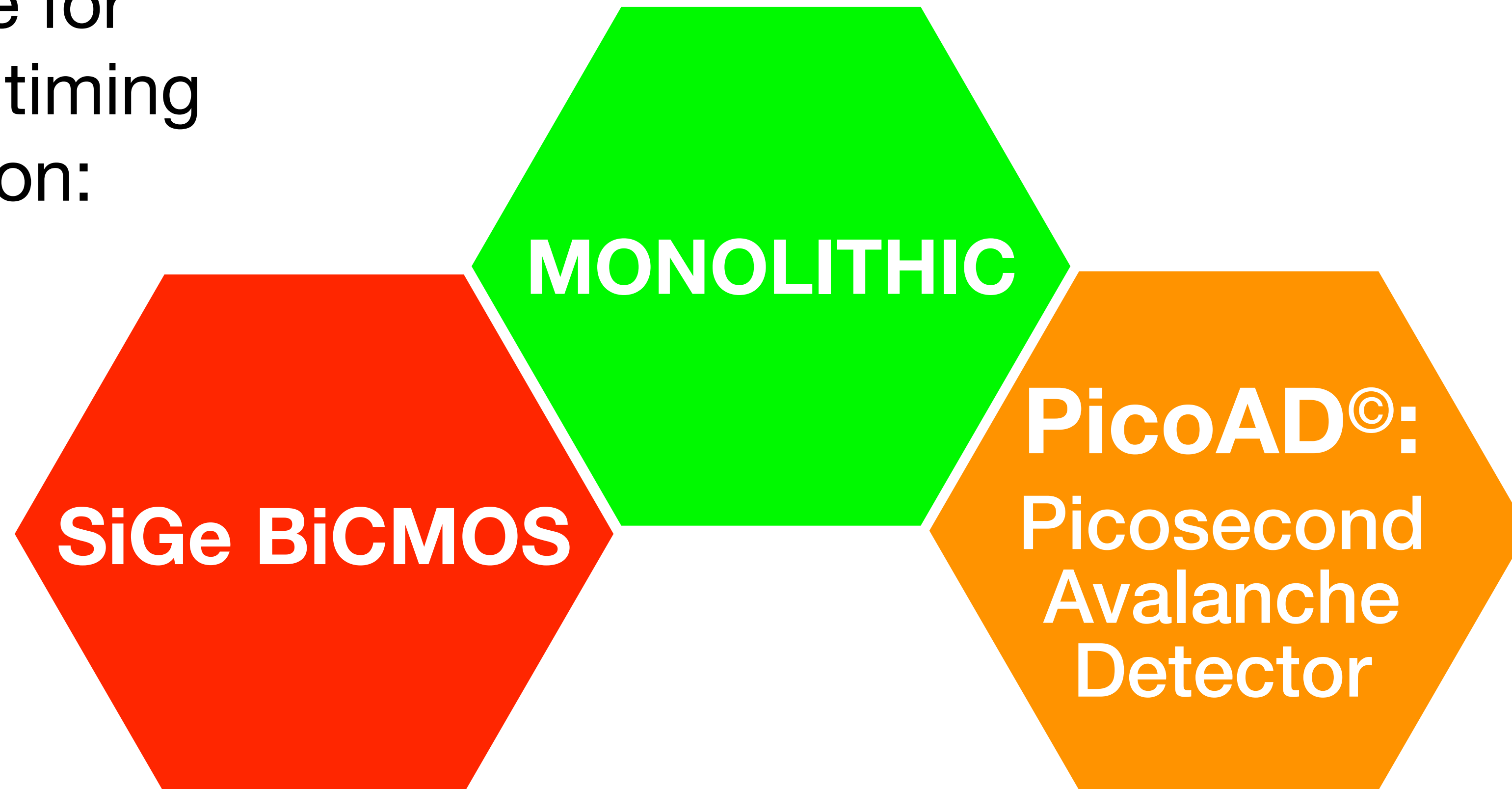
The **MONOLITH** Project



European Research Council
Established by the European Commission

Funded by the H2020 ERC Advanced grant 884447,
July 2020 - June 2025

Our recipe for
picosecond timing
with silicon:



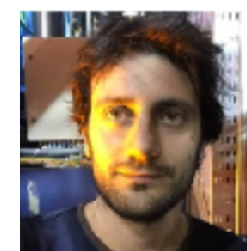


The UniGe Silicon Team



Giuseppe Iacobucci

- project P.I.
- System design



Lorenzo Paolozzi

- Sensor design
- Analog electronics



Didier Ferrere

- System integration
- Laboratory tests



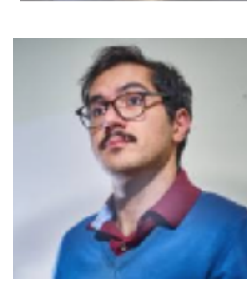
Sergio Gonzalez-Sevilla

- System integration
- Laboratory tests



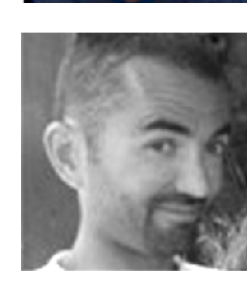
Thanushan Kugathasan

- Lead chip design
- Digital electronics



Roberto Cardella

- Sensor design
- Laboratory tests



Yannick Favre

- Board design
- RO system



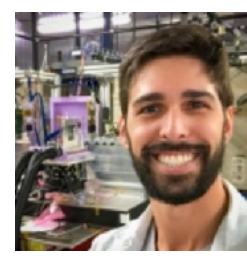
Stéphane Débieux

- Board design
- RO system



Stefano Zambito

- Laboratory tests
- Data analysis



Mateus Vicente

- System integration
- Laboratory tests



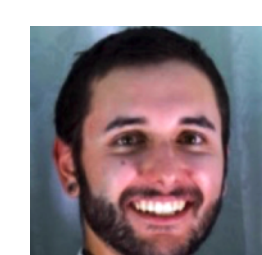
Jordi Sabater Iglesias

- Detector simulation
- Laboratory tests



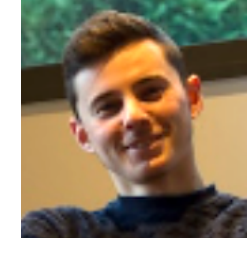
Chiara Magliocca

- Laboratory tests
- Data analysis



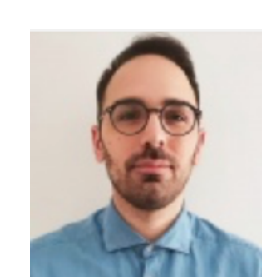
Matteo Milanesio

- Laboratory tests
- Data analysis



Théo Moretti

- Laboratory tests
- Data analysis



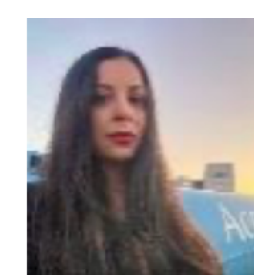
Antonio Picardi

- Chip design
- Firmware



Jihad Saidi

- Laboratory tests
- Data analysis



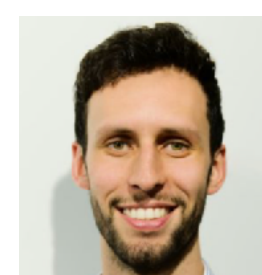
Raffaella Kotitsa

- Sensor simulation
- Data analysis



Luca Iodice

- Chip design
- Firmware



Carlo Alberto Fenoglio

- Chip design
- Firmware



Andrea Pizarro Medina

- Data analysis
- Laboratory tests

Main research partners:



Roberto Cardarelli
INFN Rome2 & UNIGE



Holger Rücker
IHP Mikroelektronik



Marzio Nessi
CERN & UNIGE



Matteo Elviretti
IHP Mikroelektronik

Funded by:



**Swiss National
Science Foundation**



Sinergia



European Research Council
Established by the European Commission



**UNIVERSITÉ
DE GENÈVE**

UNITEC



The **MONOLITH** Project



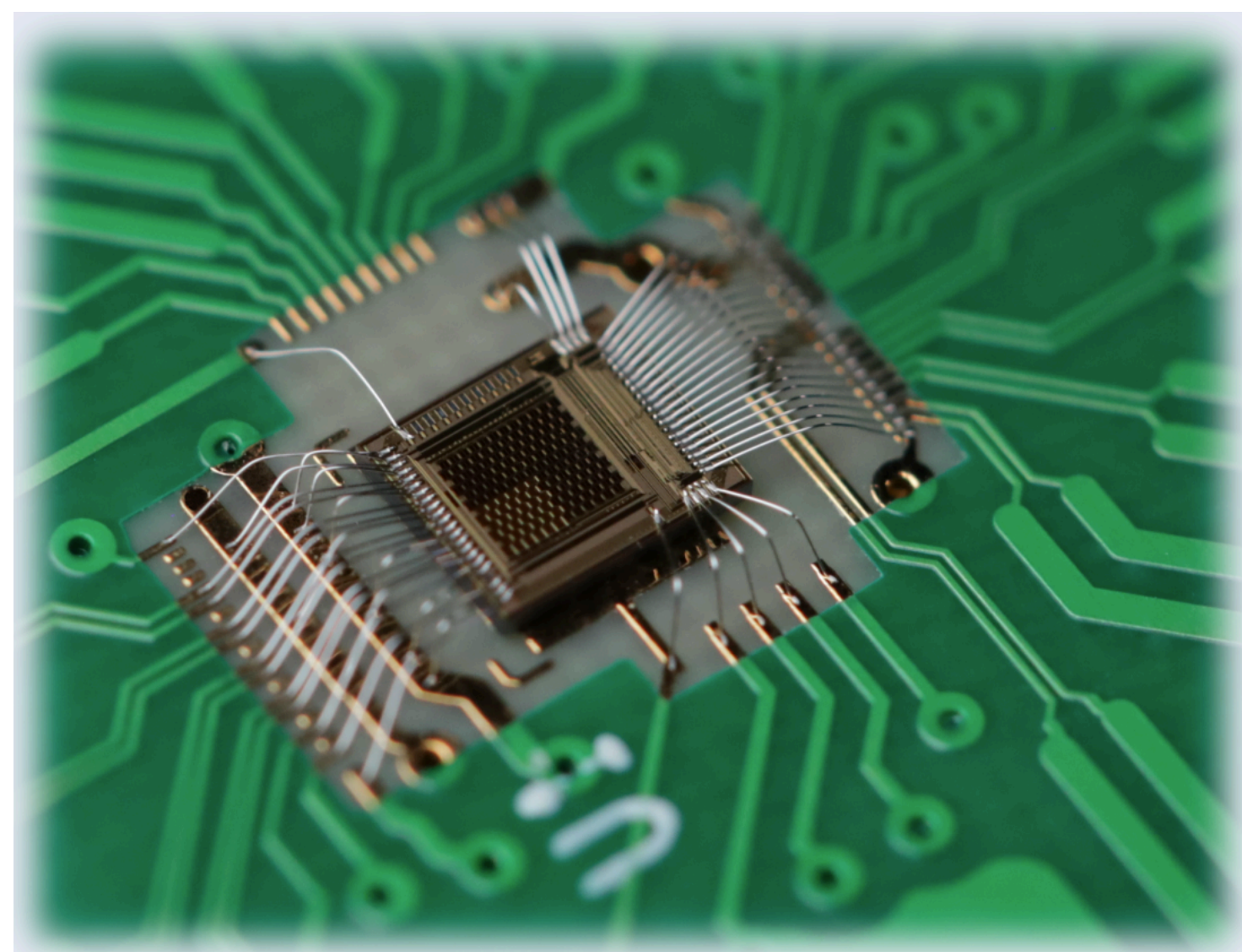
Funded by the H2020 ERC Advanced grant 884447,
July 2020 - June 2025

Today I will show the results obtained with:

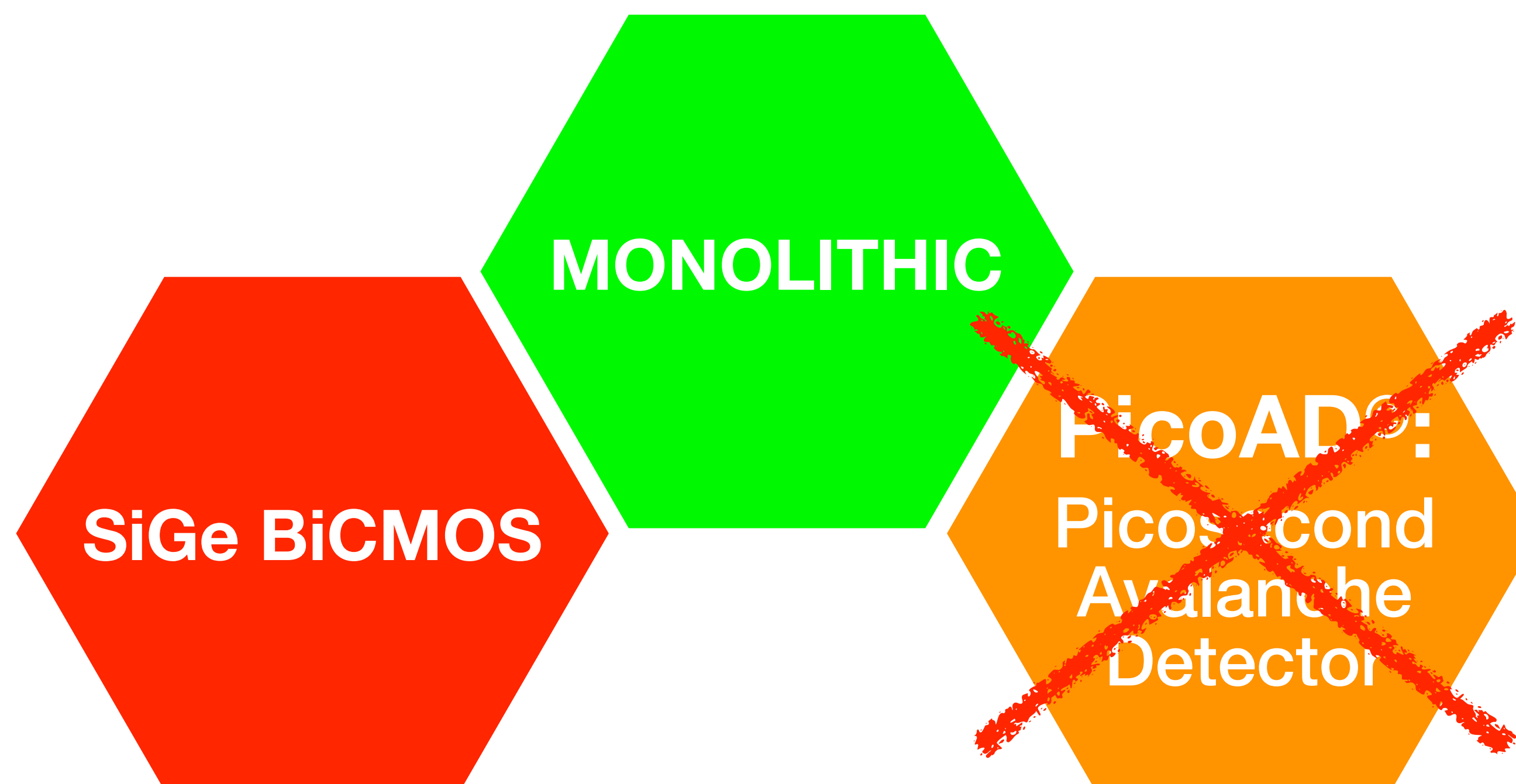
1. the **2022 prototype WITHOUT GAIN LAYER** with improved SiGe electronics, and the effects of proton irradiation up to **1×10^{16} 1MeV n_{eq}/cm^2**
➔ PicoAD version back from foundry in October
2. the **PicoAD proof-of-concept**, produced on SiGe electronics of 2020 prototype

All ASICs were produced in the 130nm SiGe BiCMOS SG13G2 process by



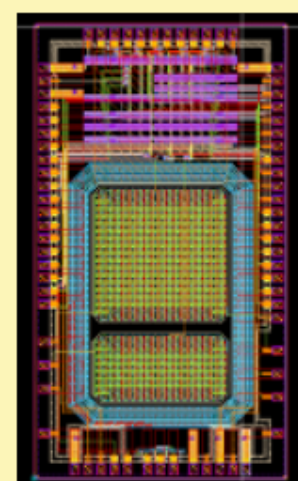


2022 prototype no gain layer



Monolithic prototypes in SiGe BiCMOS (without internal gain layer)

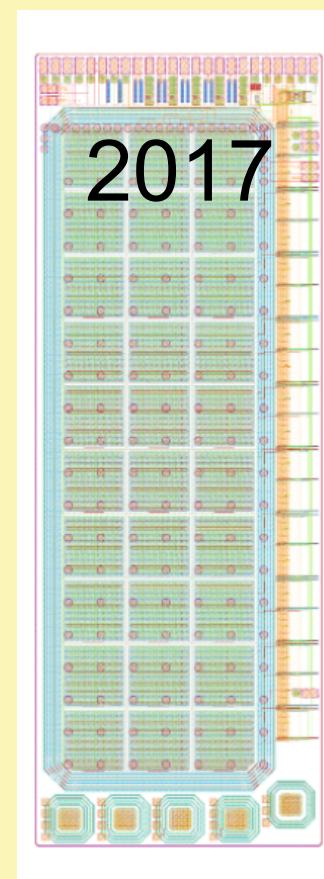
2016



200ps

- 1 mm² pixel
- Discriminator

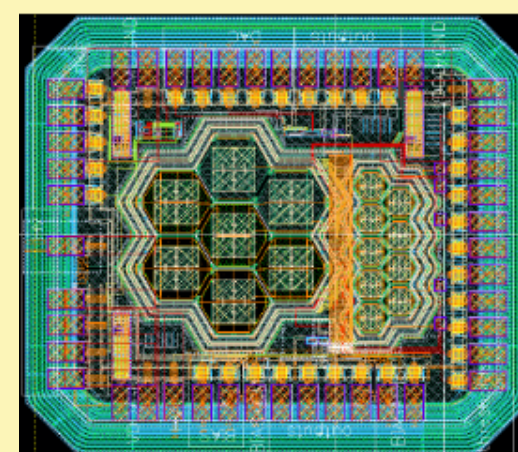
2017



110ps

- 30 pixels 500x500μm²
- 100ps TDC + I/O logic

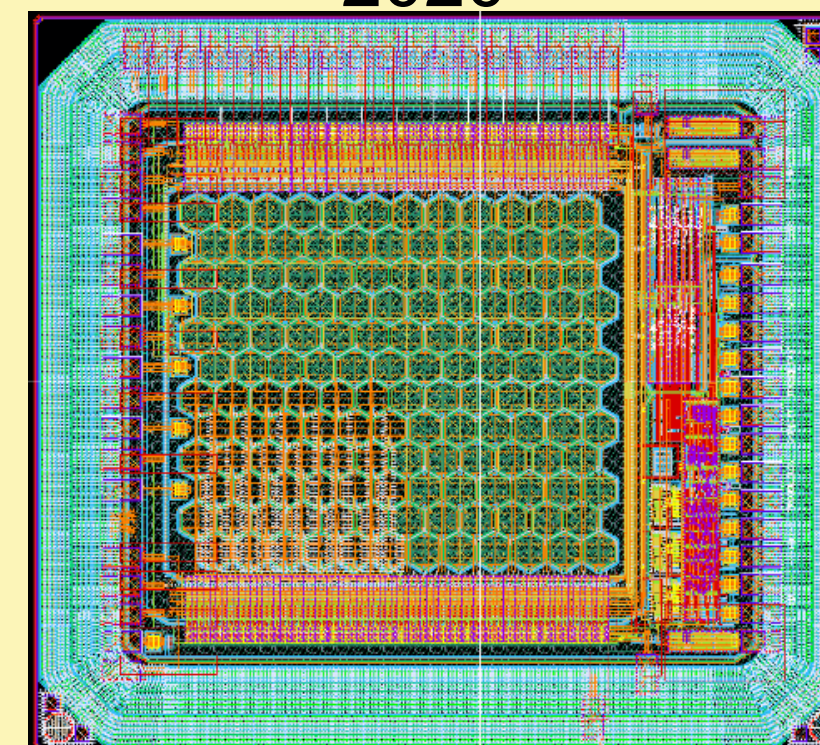
2018



50ps

- Hexagonal pixels 100μm and 200μm pitch
- Discriminator output

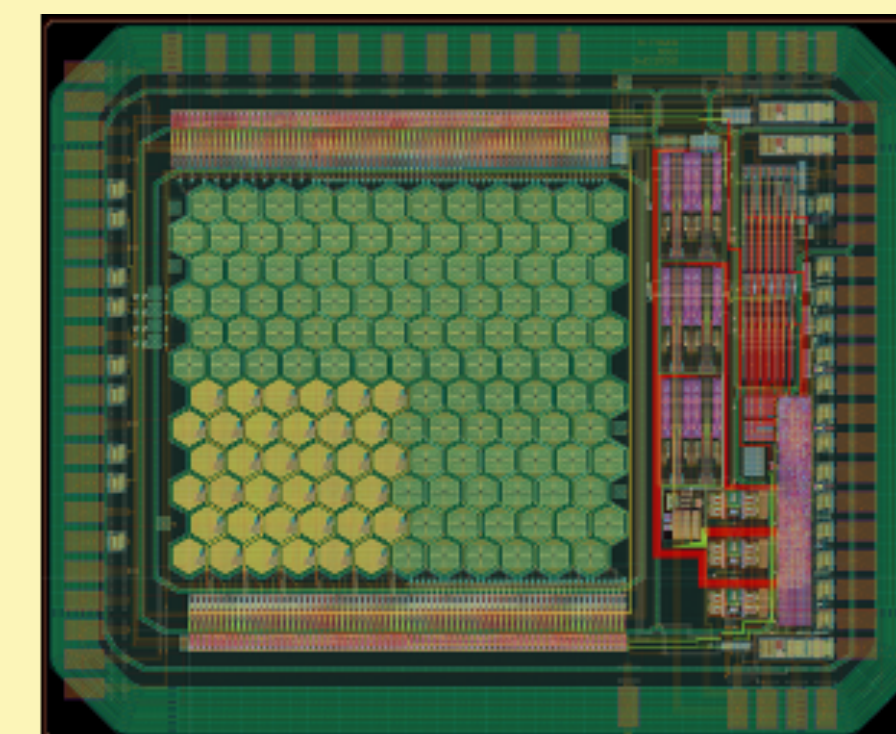
MONOLITH prototype 1
2020



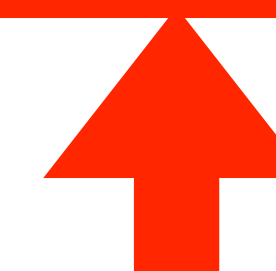
36 ps

- Hexagonal pixels 100μm pitch
- 30ps TDC + I/O logic
- 4 analog channels

**MONOLITH prototype 2
2022**

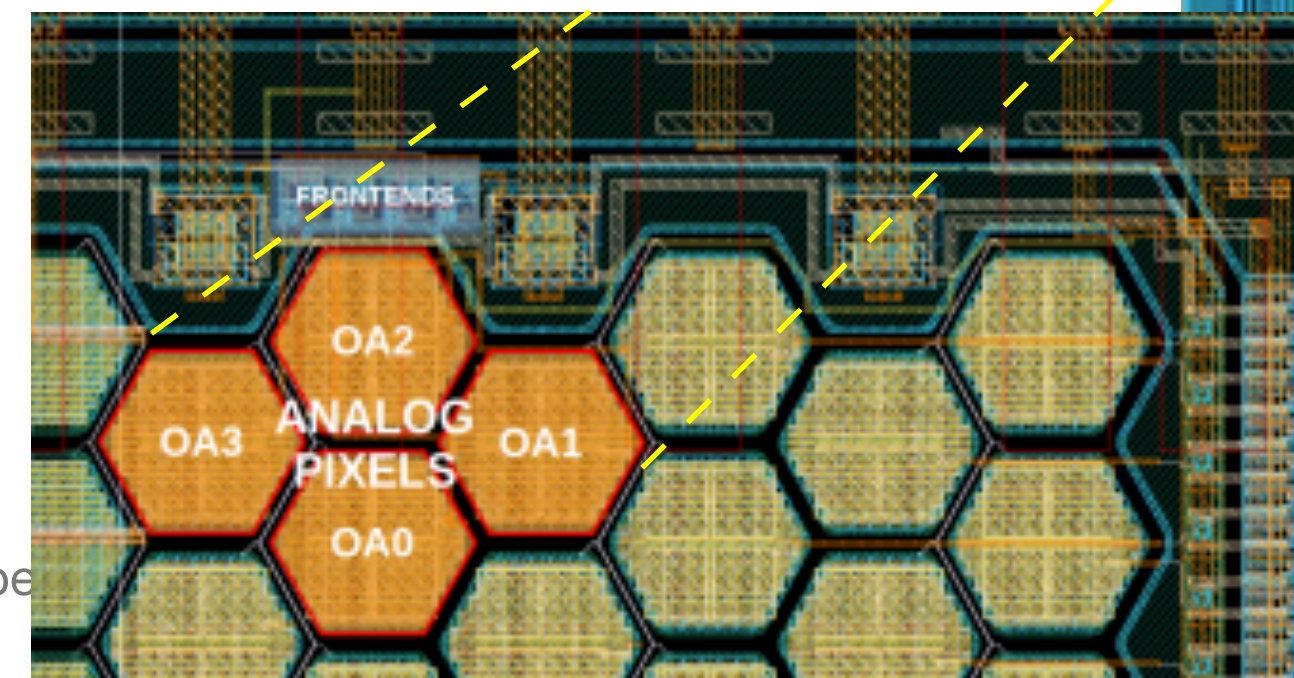
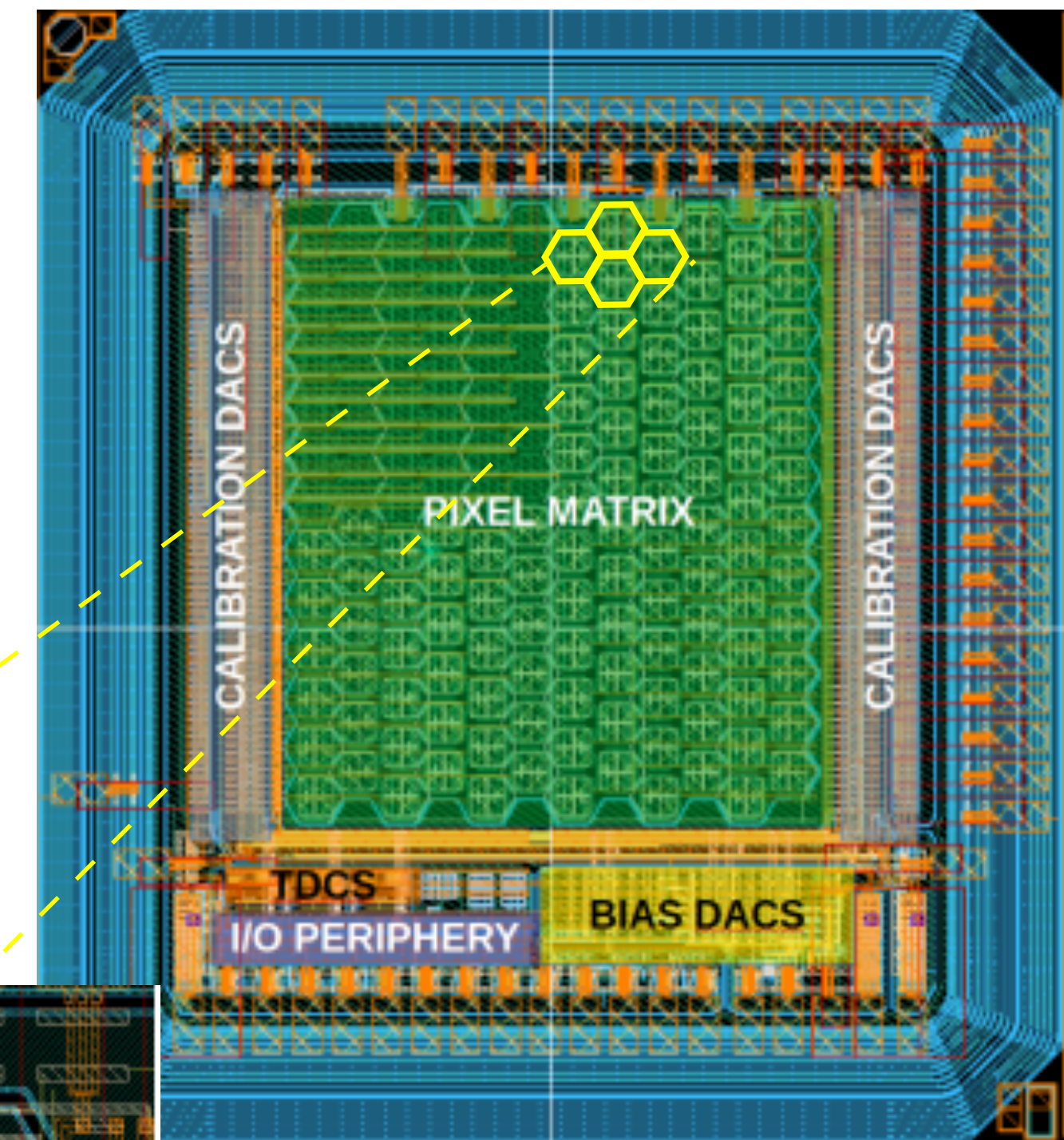
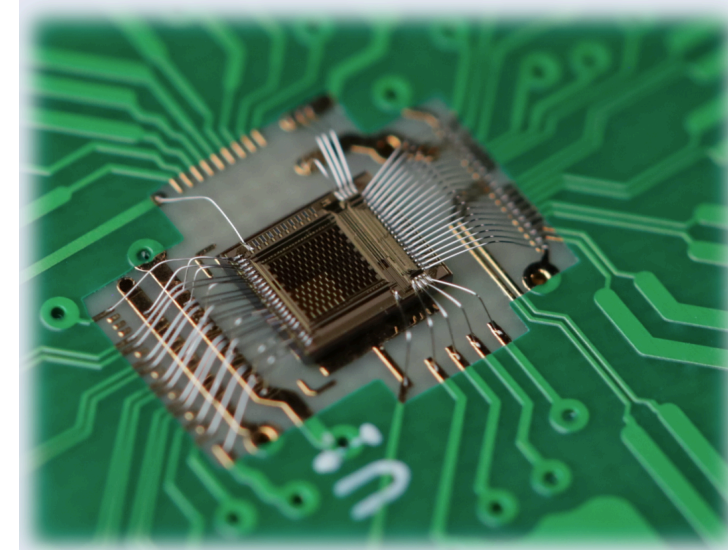


- Matrix of 12x12 hexagonal pixels
- 100μm pitch
- improved electronics
- 50μm epitaxial layer (350Ωcm)

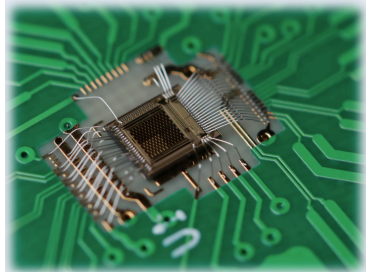


evolution of 2020 prototype

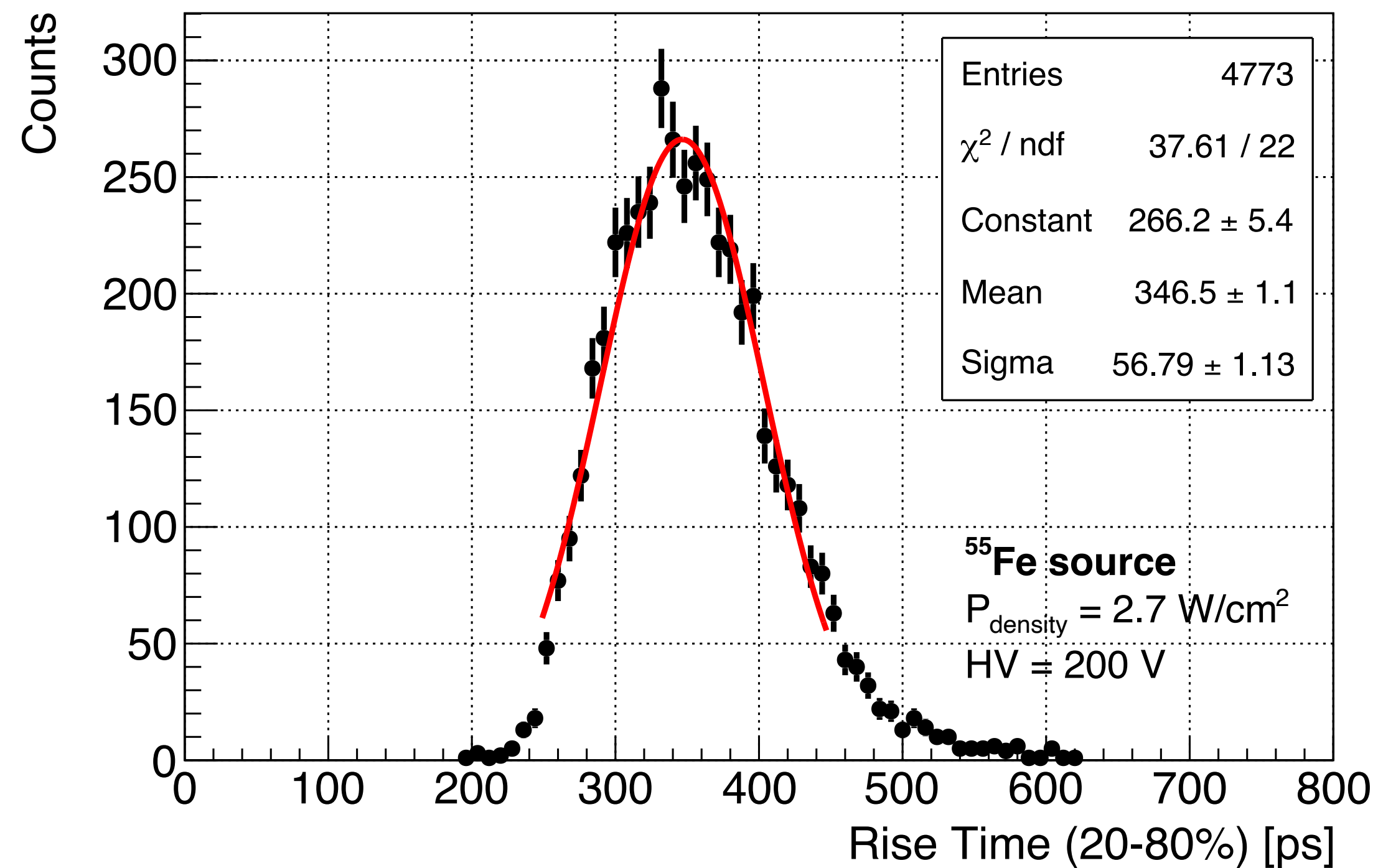
- Same matrix configuration as prototype1, but
 - ▶ **Substrate**: $50\Omega\text{cm} \rightarrow 350\Omega\text{cm}$ epilayer, $50\mu\text{m}$ thick on low-res ($1\Omega\text{cm}$)
 - ➔ smaller pixel capacitance
 - ➔ depletion $23\mu\text{m} \rightarrow 50\mu\text{m}$
 - ➔ larger voltage plateau
 - ➔ can operate sensor with V_{drift} saturated everywhere
 - ▶ **Preamplifier and driver** voltage decoupled
 - ➔ was limiting optimal amplifier operation
 - ➔ was creating cross-talk, removed
 - ▶ **Optimised FE layout, differential output**, high-frequency cables
 - ➔ better rise time ($600\text{ps} \rightarrow 300\text{ps}$)



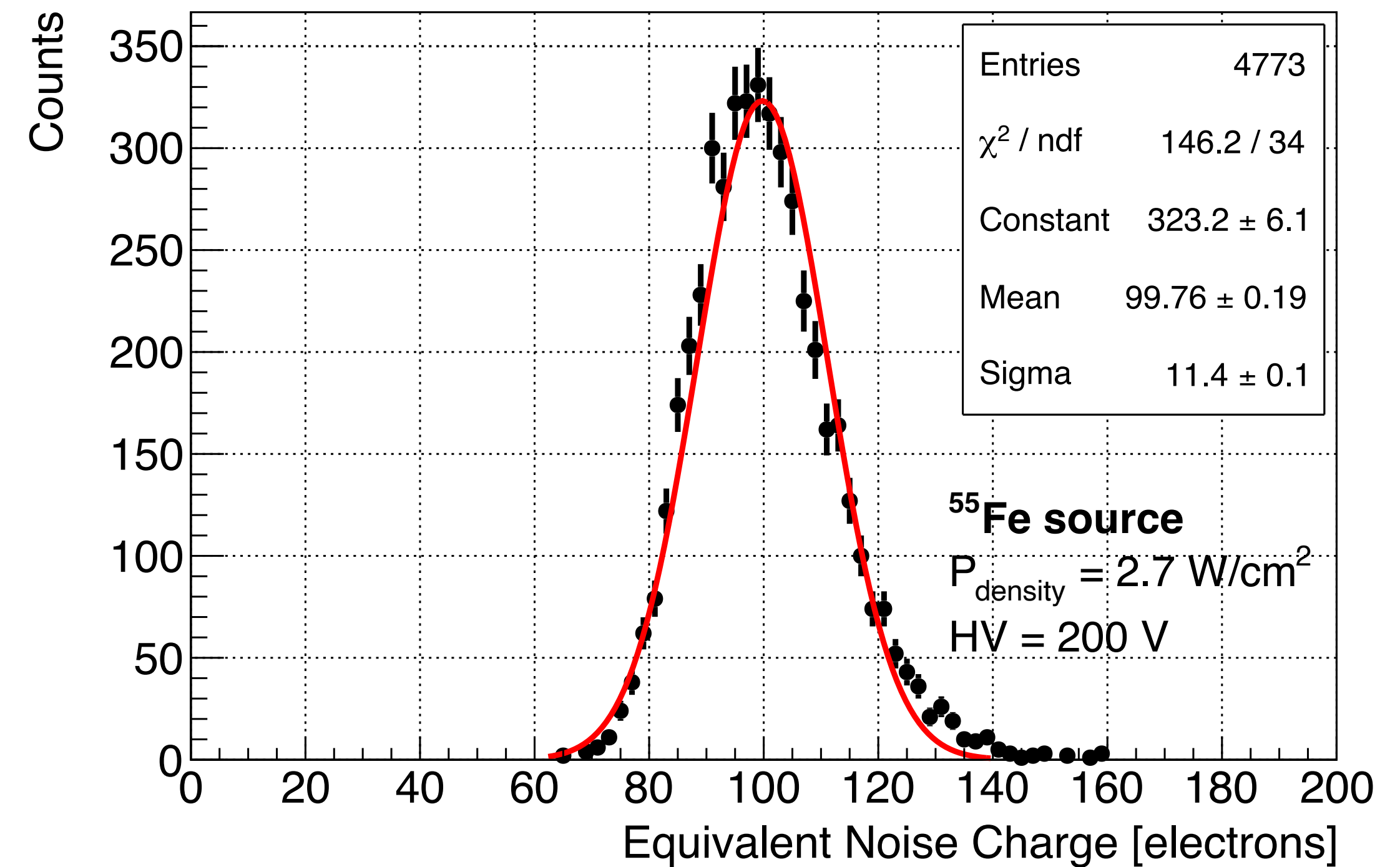
⁵⁵Fe measurements in cleanroom:



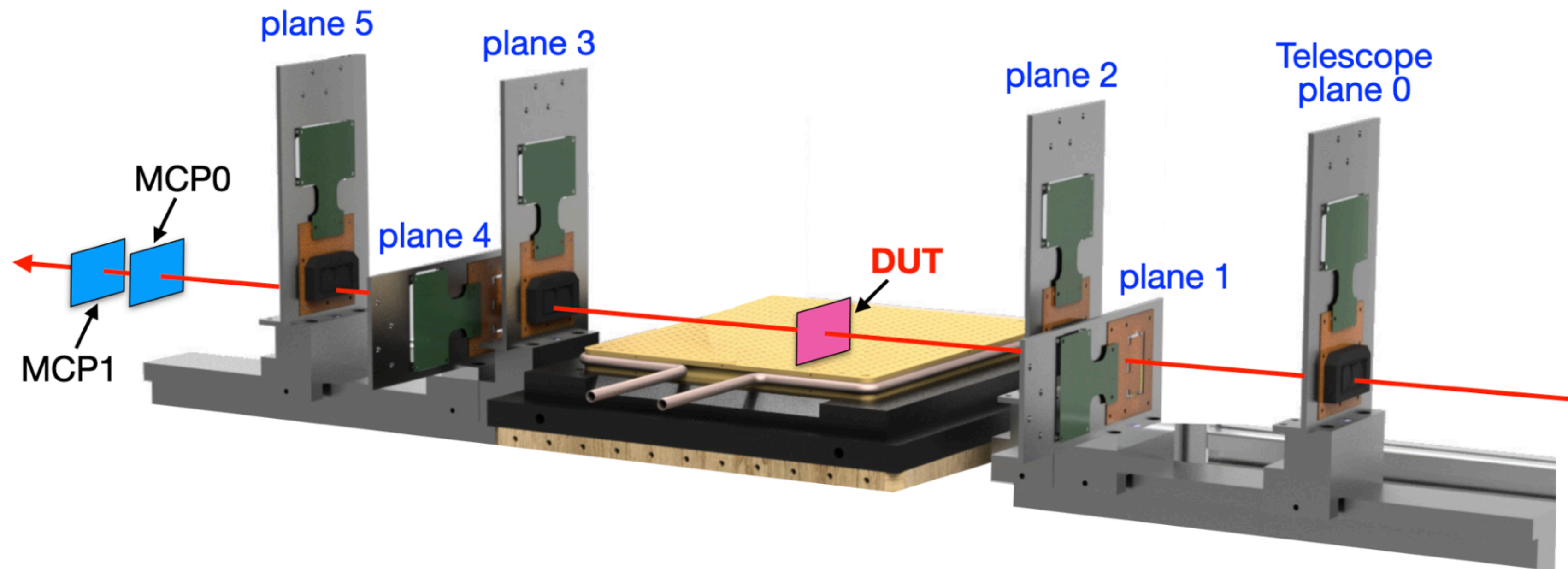
Risetime (20%–80%) $\approx$ 350 ps



ENC $\approx$ 100 e⁻



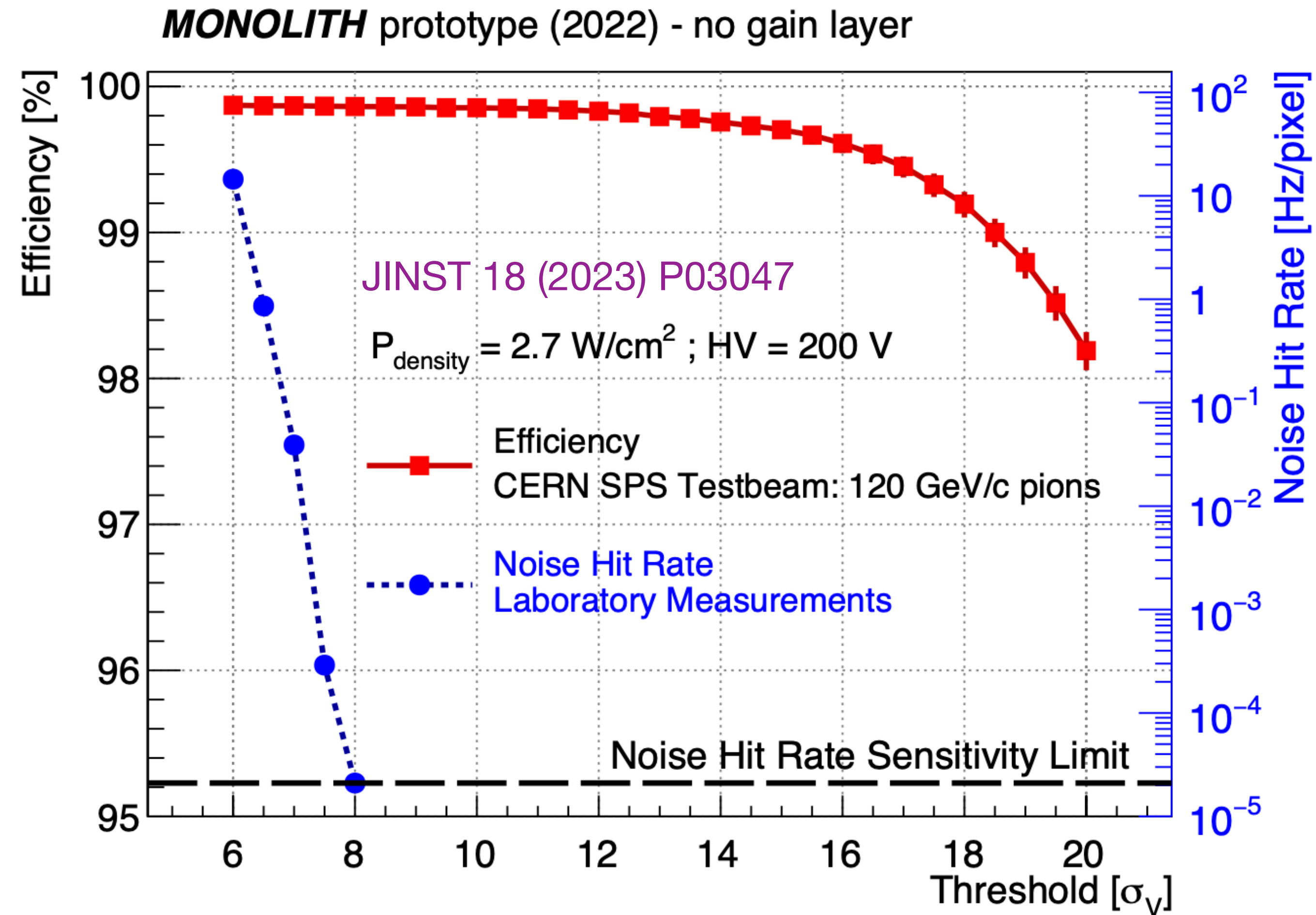
Mid October SPS testbeam with 120 GeV/c π to measure **efficiency** and **time resolution**



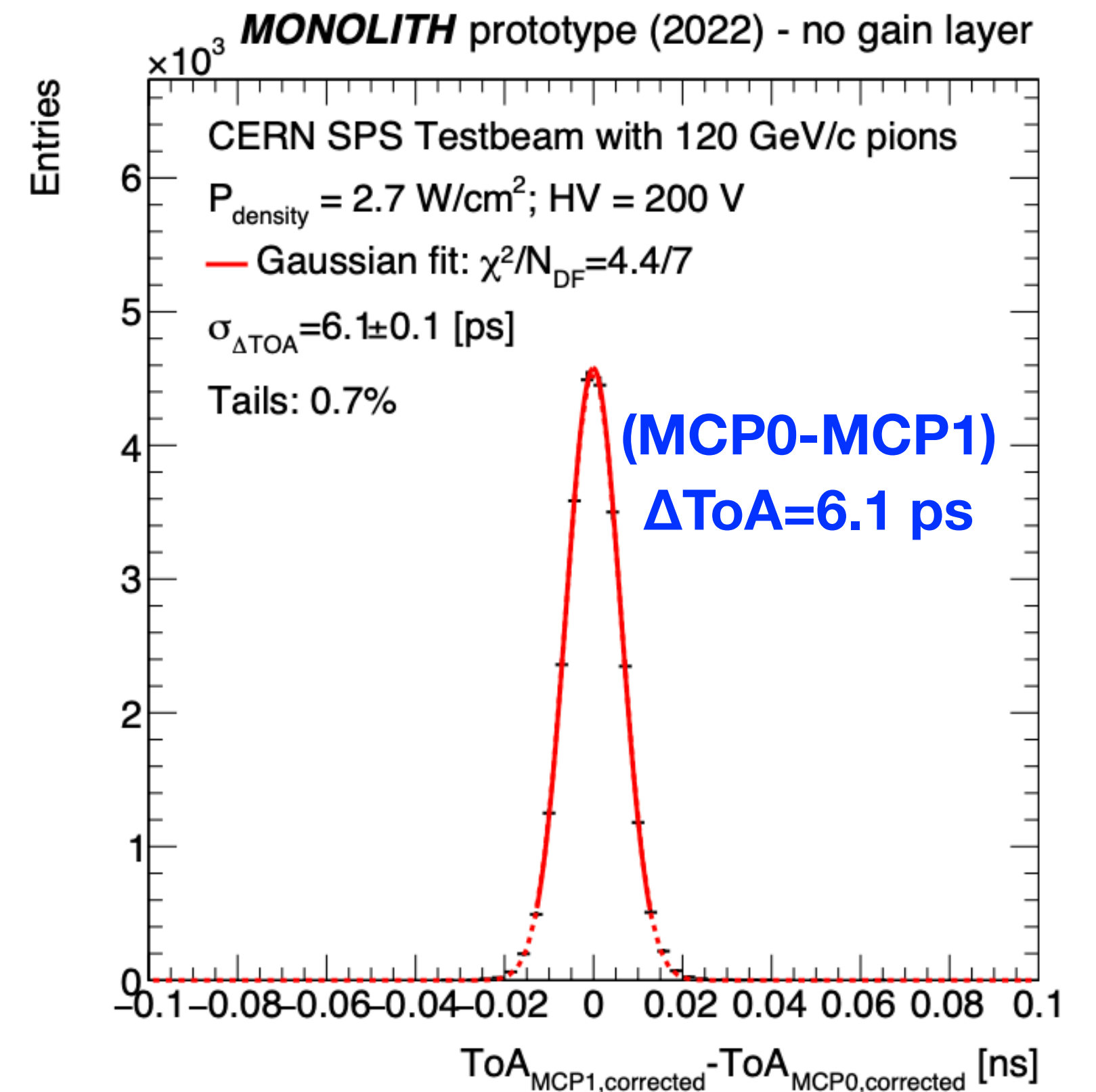
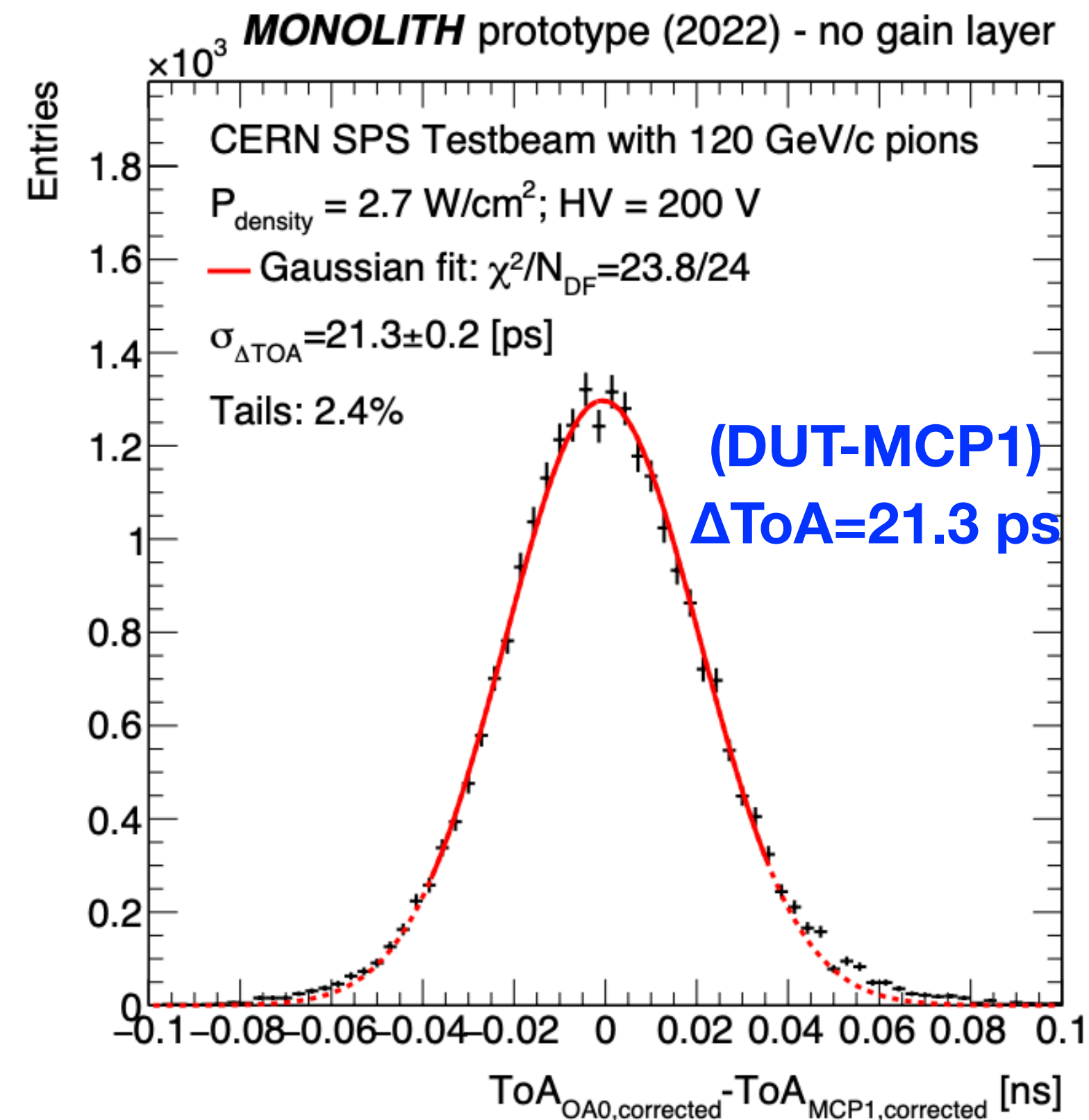
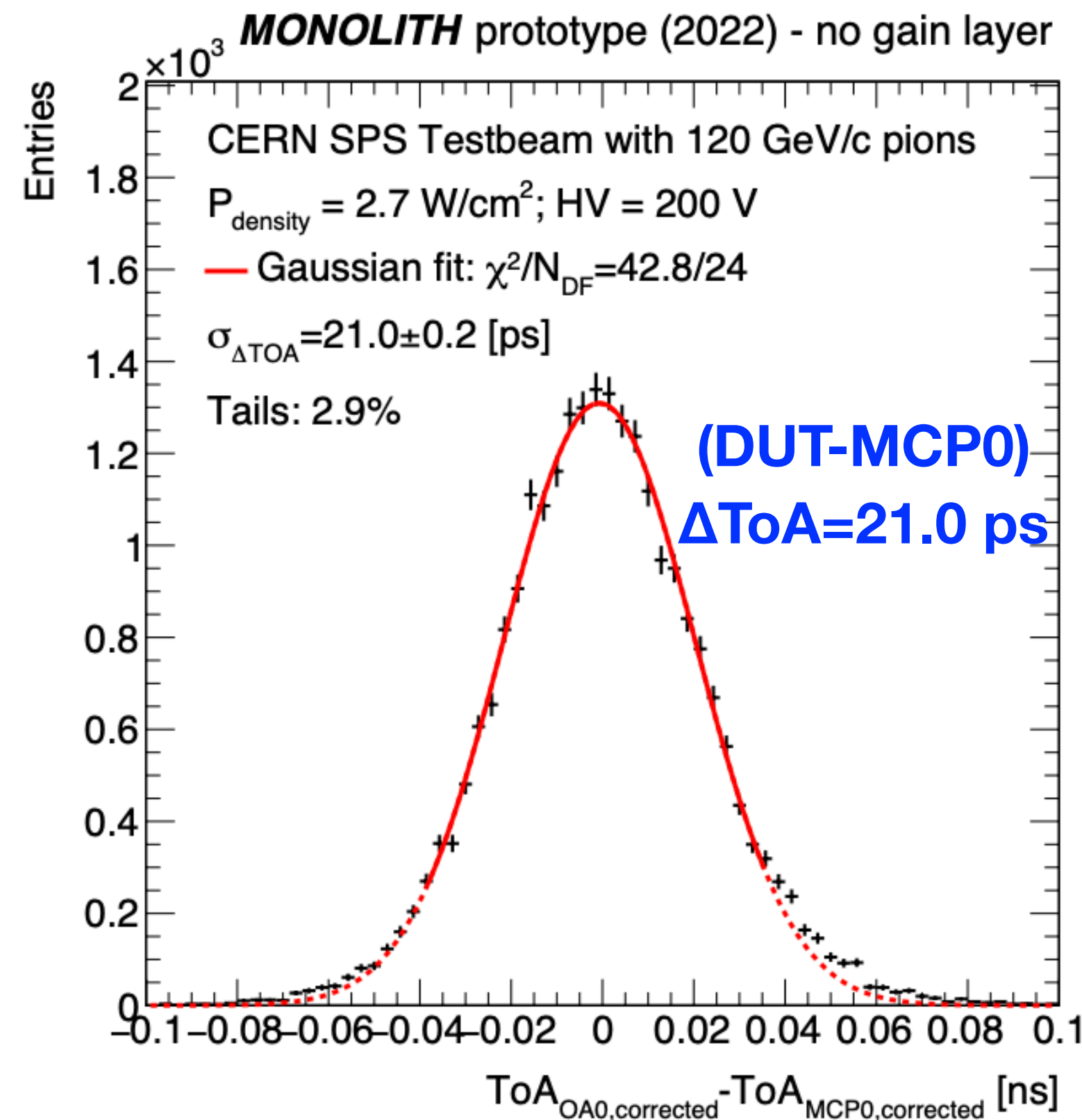
UNIGE FE-I4 telescope to provide spatial information ($\sigma_{x,y} \approx 10 \mu\text{m}$)

Two MCPs ($\sigma_t \approx 5 \text{ ps}$) to provide the timing reference

Lots of data taken: results in **JINST 18 (2023) P03047**



Large efficiency plateau at $\approx 99.8\%$,
that allows operation at very low noise-hit rate

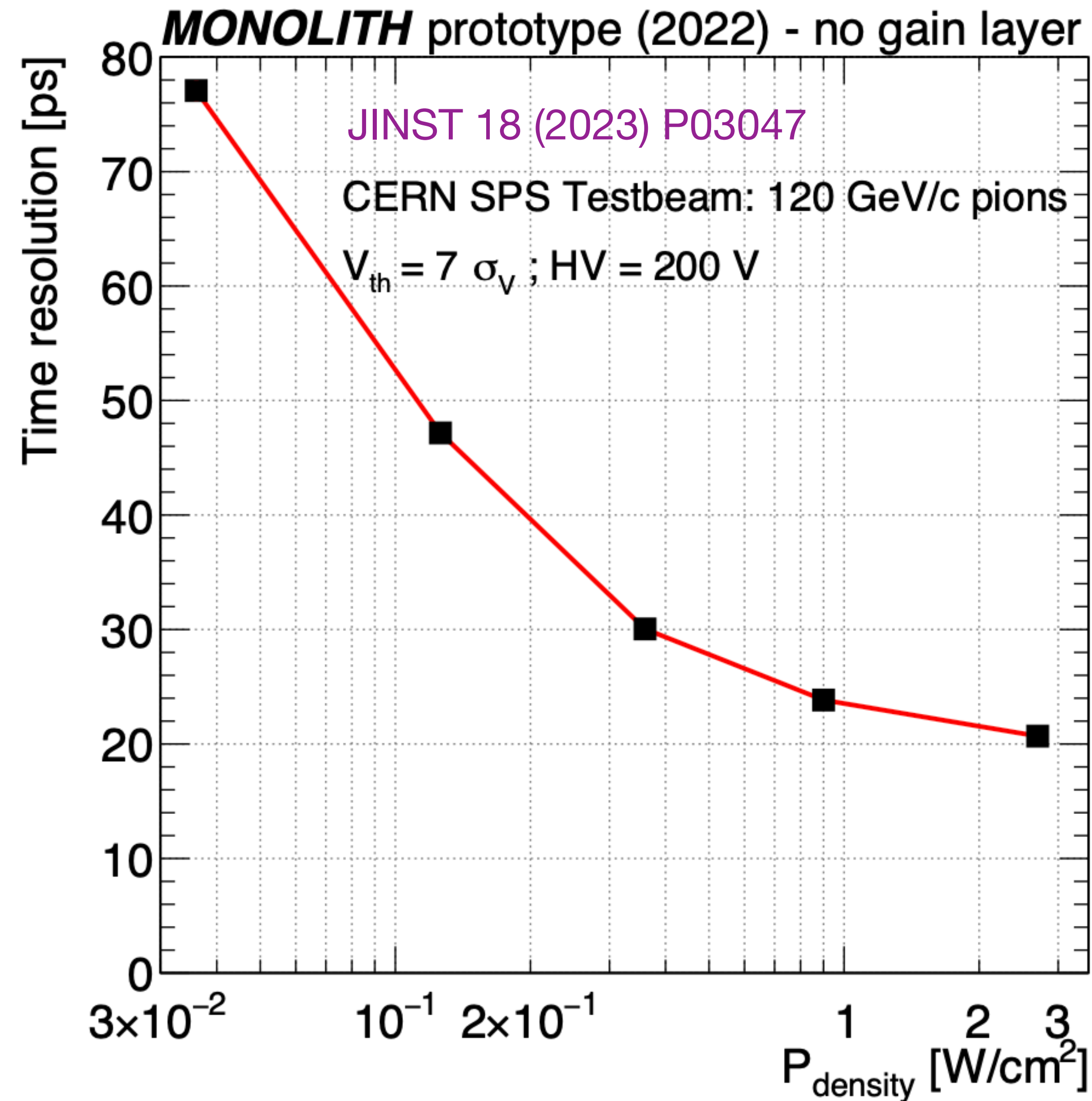


- Simultaneous fit to extract time resolutions of the DUT, MCP0, MCP1:

Fit results: MCP0 $\sigma_T = (3.6 \pm 1.5) \text{ ps}$
 MCP1 $\sigma_T = (5.0 \pm 1.1) \text{ ps}$

$\sigma_T = (20.7 \pm 0.3) \text{ ps}$

non-Gaussian tails $\approx 3\%$

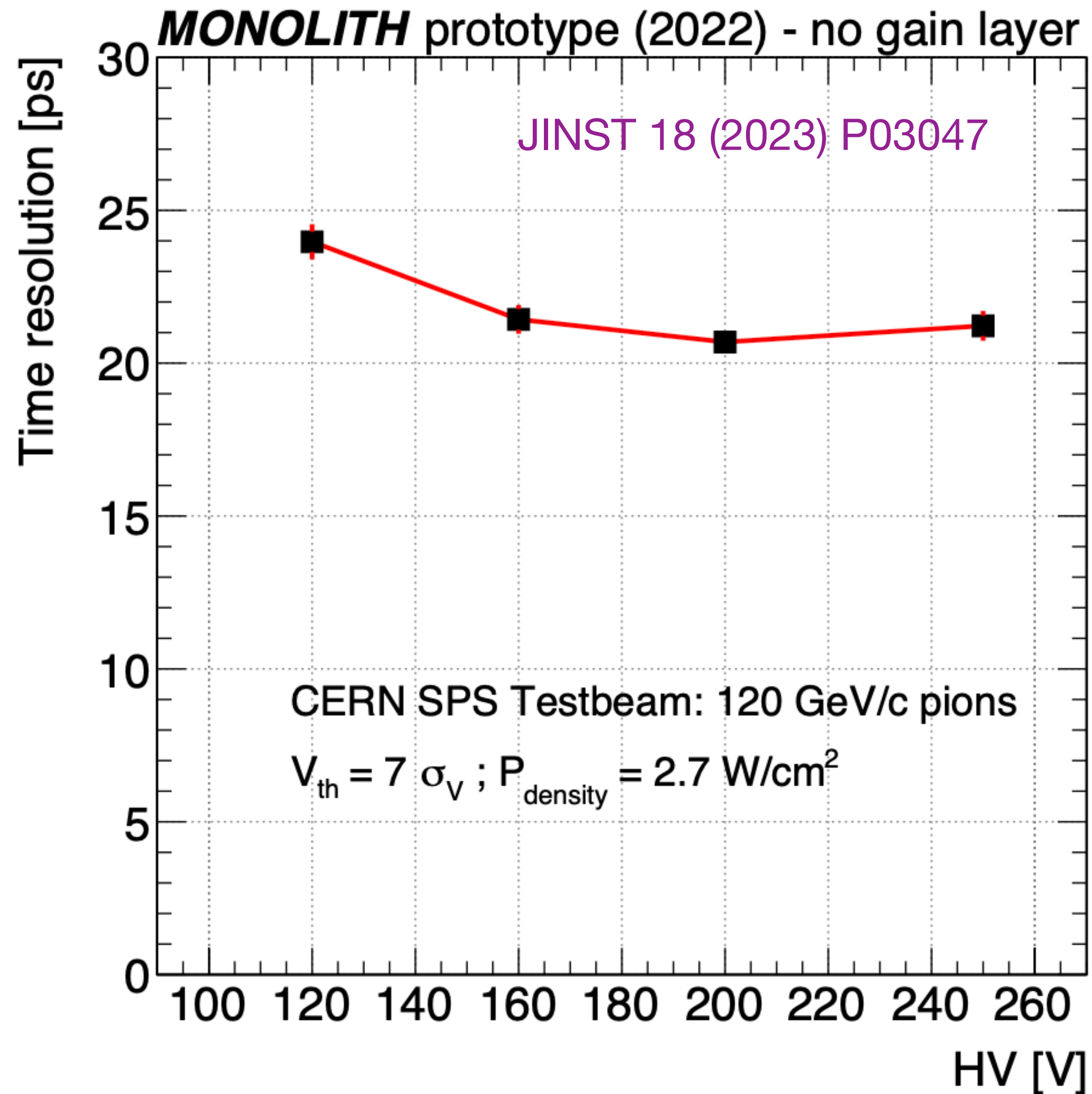


DUT operated at $HV = 200$ V and $V_{th} = 7\sigma_V$		
$P_{density}$ [W/cm ²]	Amplitude MPV [mV]	Time Resolution [ps]
2.7	48.6 ± 0.5	20.7 ± 0.3
0.9	35.8 ± 0.5	23.8 ± 0.3
0.36	22.6 ± 0.4	30.1 ± 0.4
0.13	14.2 ± 0.3	47.2 ± 0.7
0.04	16.2 ± 0.3	77.1 ± 0.9

20 ps at 2.7 W/cm²

50 ps at 0.1 W/cm²

Without gain layer.



Plateau of 100V with
time resolution of
 $\approx 20 \text{ ps}$

Without gain layer

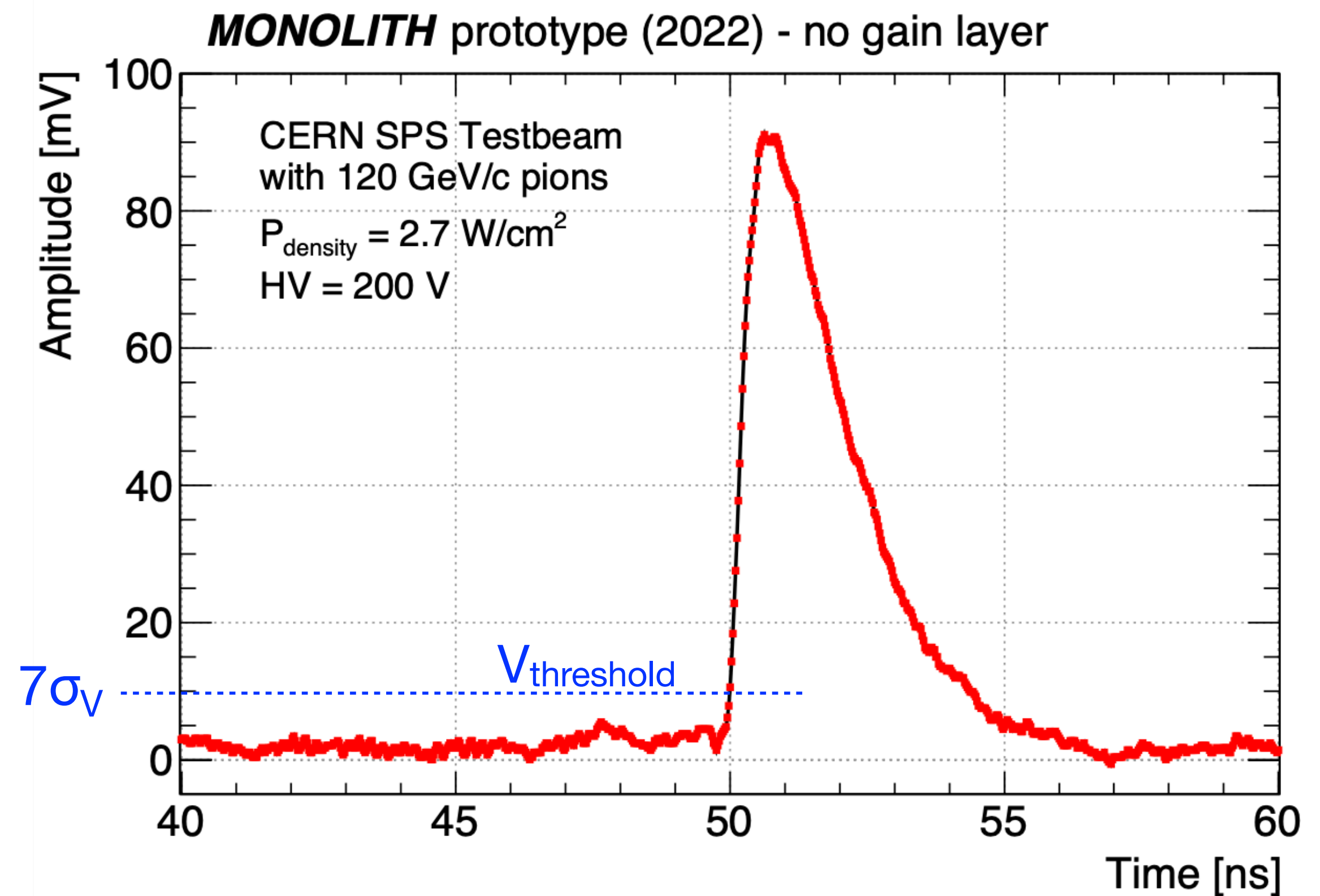
Results obtained with
simple analysis and
simple signal processing

Time resolution measurements

Remark :

20.7 ps obtained with very simple analysis:

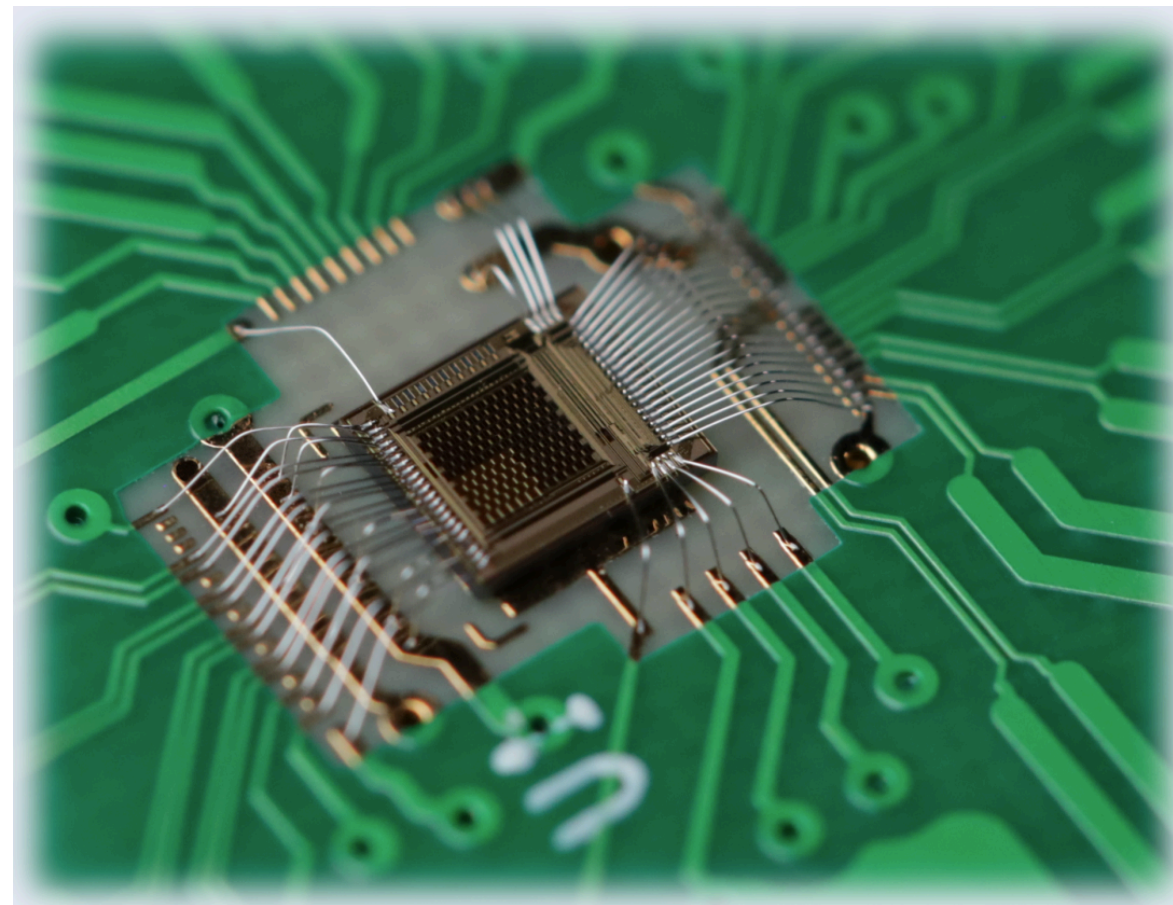
- **Linear interpolation** of oscilloscope samplings (25ps)
- Time Of Arrival (ToA): time at $V_{\text{threshold}} = 7\sigma_V$
- Δ_{ToA} distributions are **time-walk corrected**



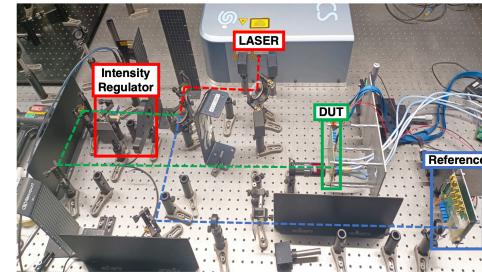
More complex analysis (spline interpolation, filtering, ...) reaches **17.7 ps**

Laser measurements

with the 2022 prototype2 without gain

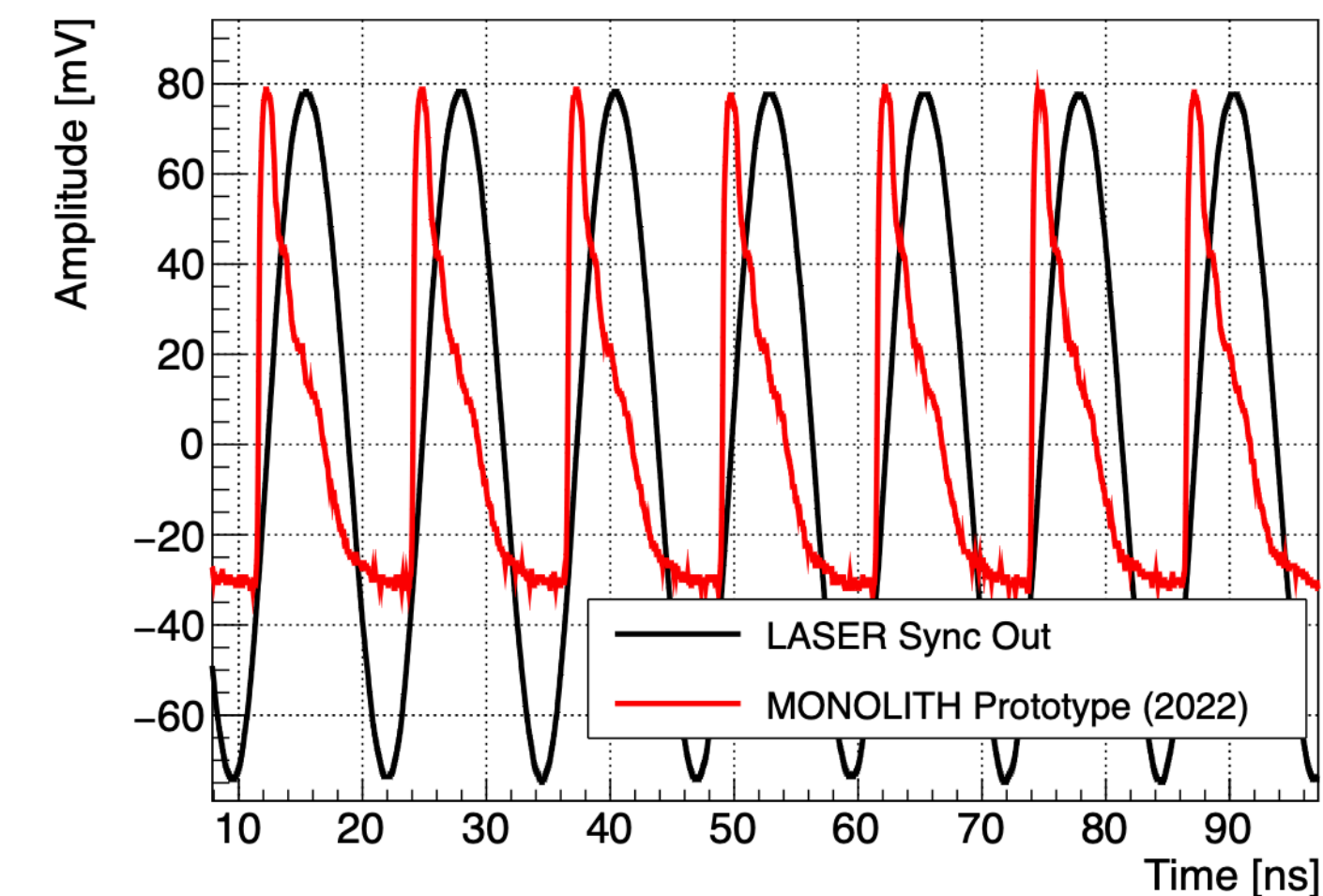
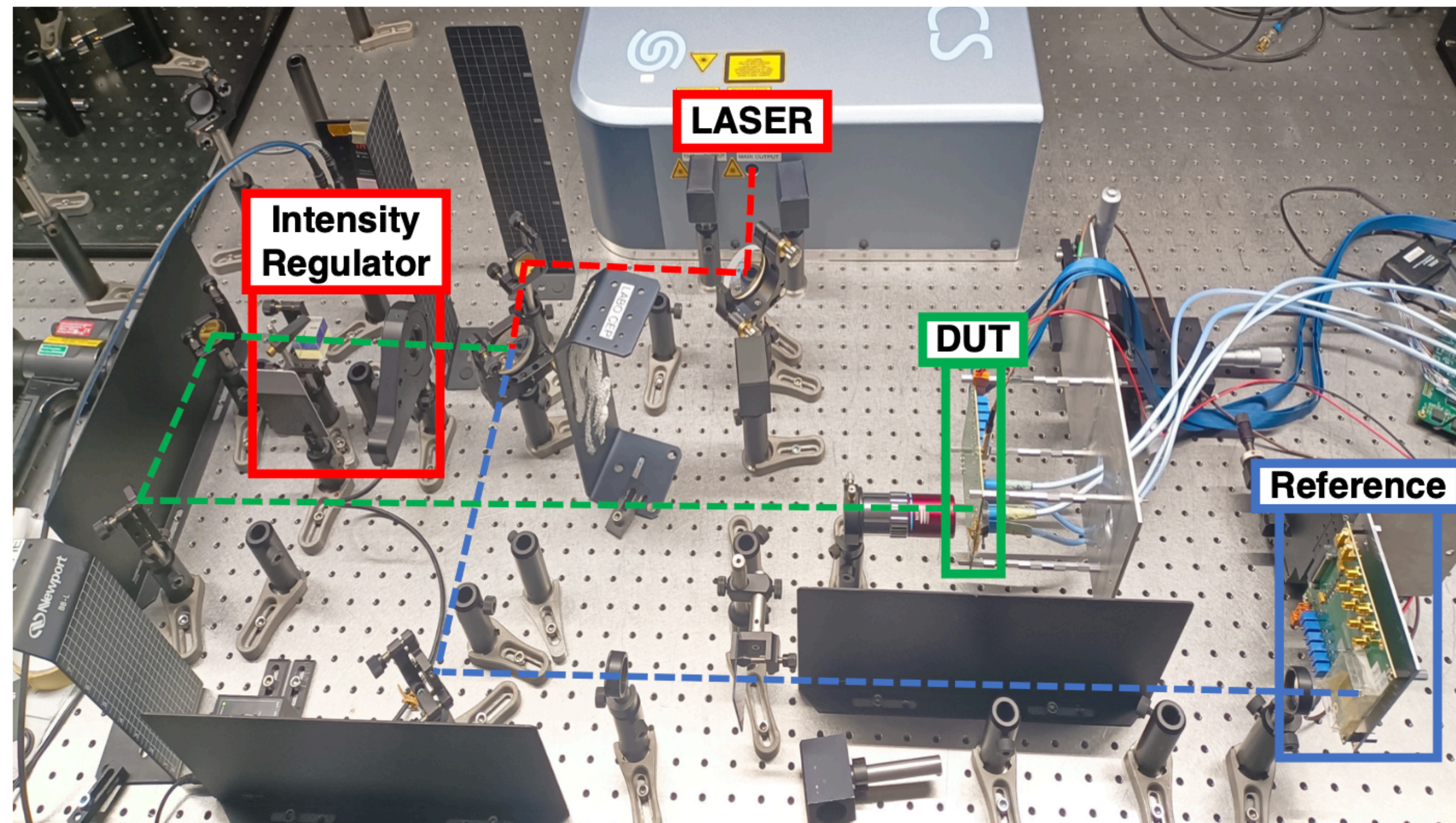


Measurement with a **laser** with a jitter of **100 fs**
(repetition frequency = **80 MHz**)



Laser Measurement

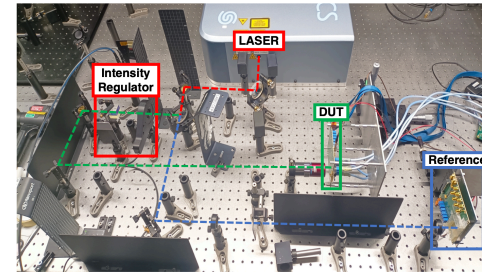
Many thanks to
L. Bonacina's lab of GAP UNIGE



Time coincidence between two of our samples:

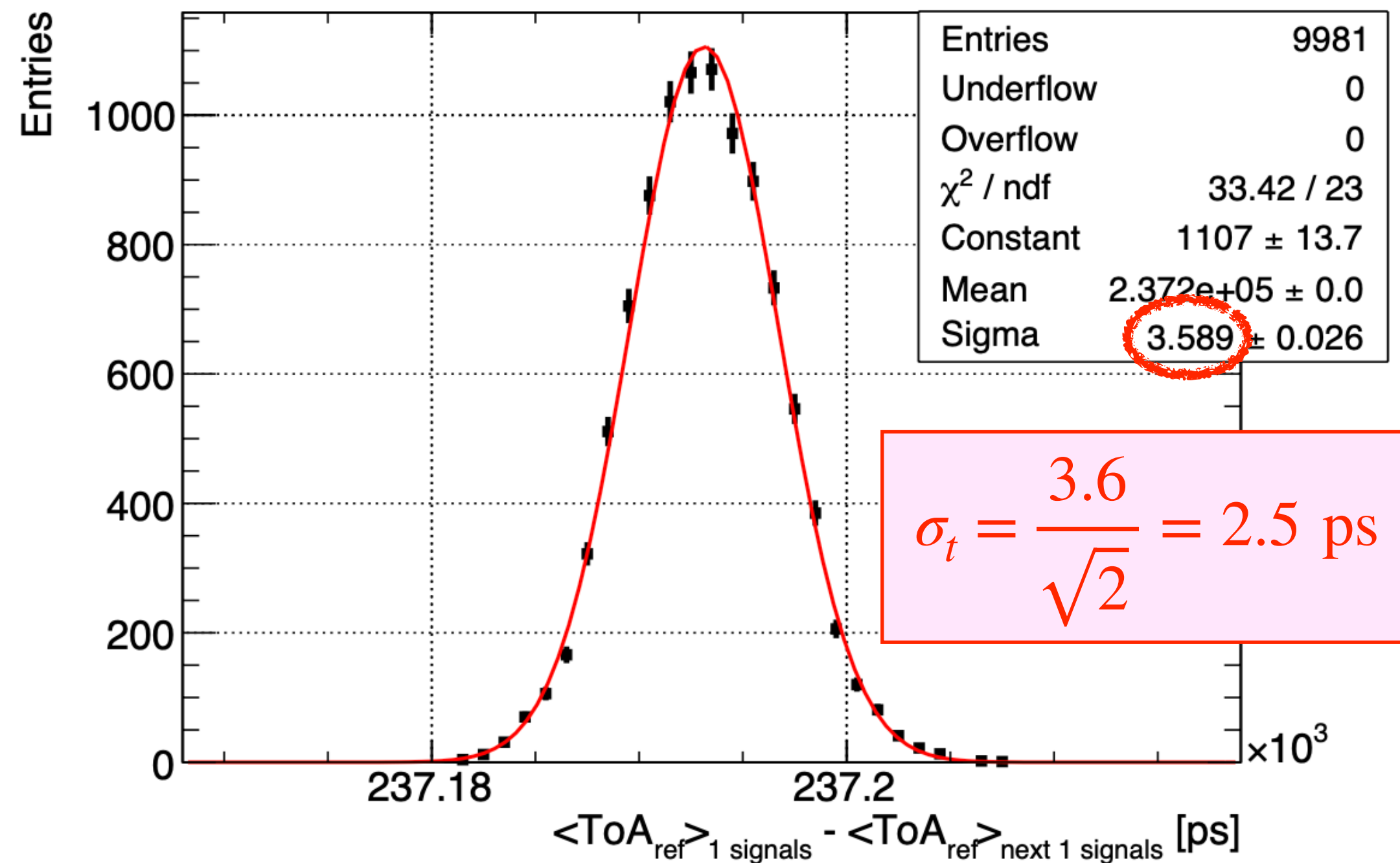
- ➔ “**Reference**” receiving always large laser pulse producing 17k electrons ($\sigma_t = 2.5$ ps)
- ➔ “**DUT**” receiving variable laser power, to study the performance vs. amplitude

Laser Measurement (preliminary)



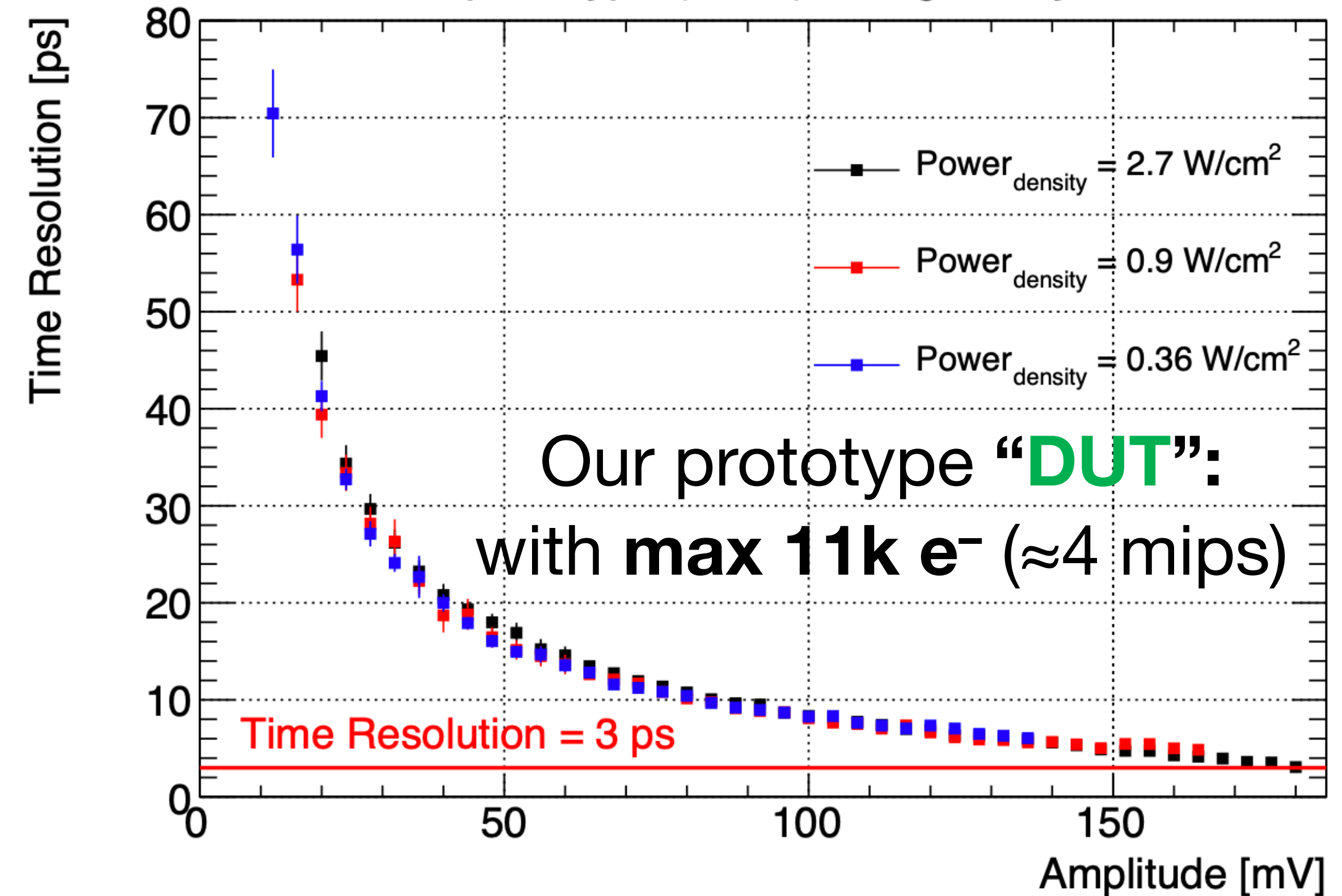
Laser Measurement

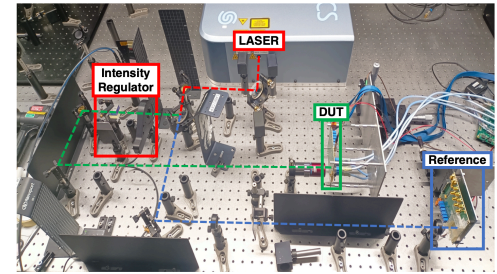
MONOLITH prototype (2022) - no gain layer



Our prototype “Reference”:
Time resolution = 2.5 ps
 with **17k e⁻** (5—6 mips)

MONOLITH prototype (2022) - no gain layer

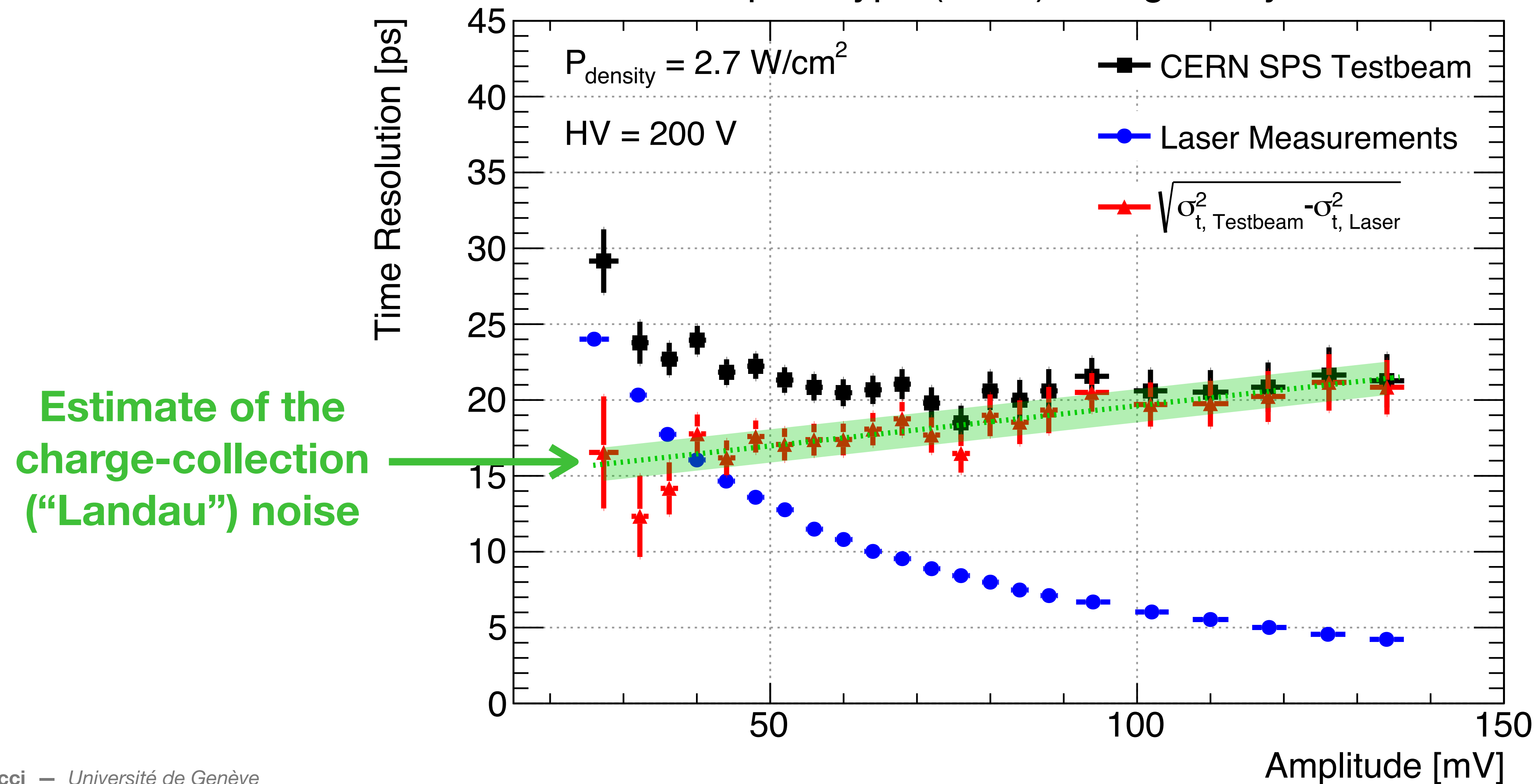




Laser Measurement

Laser Measurement (preliminary)

MONOLITH prototype (2022) - no gain layer

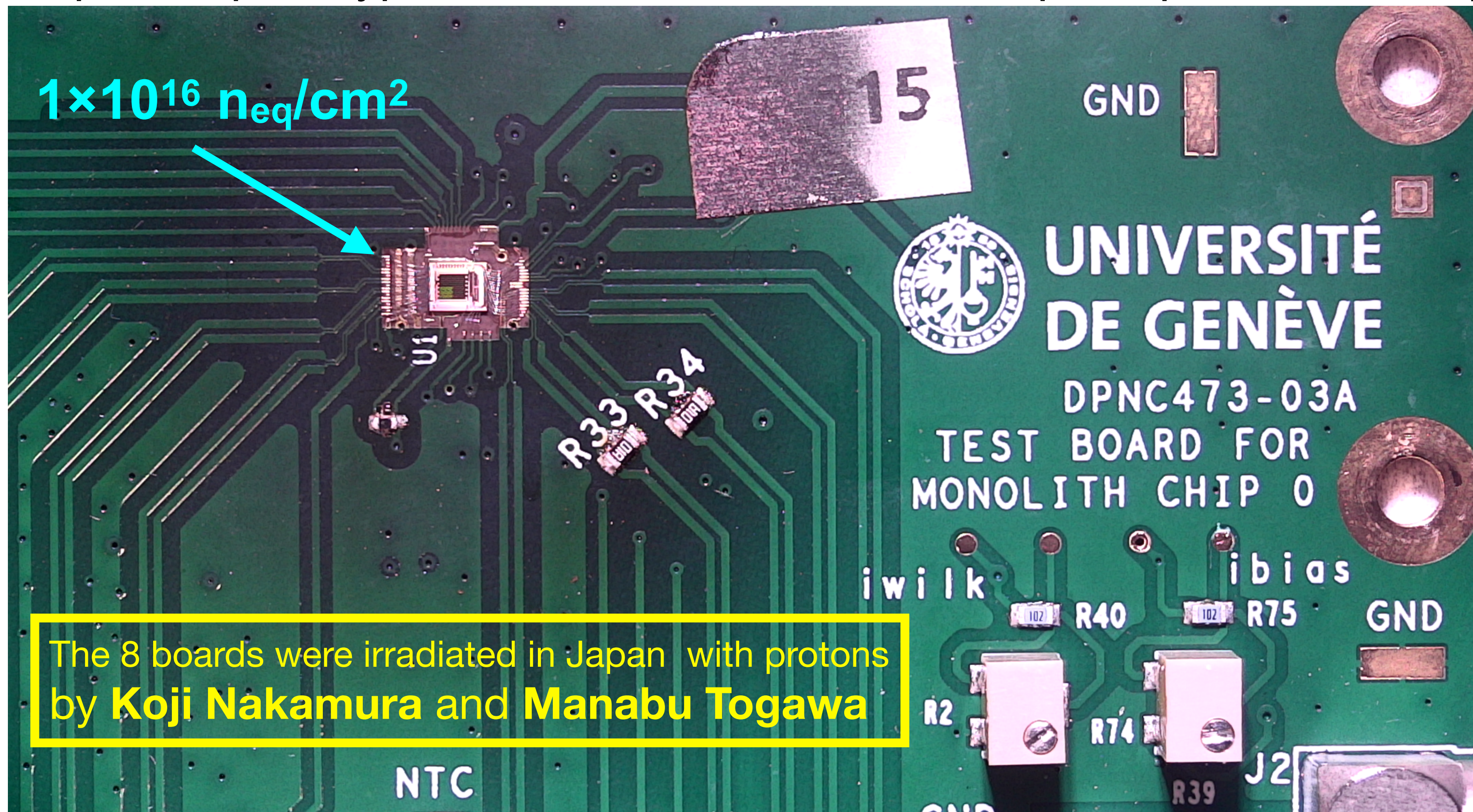


Radiation hardness studies

with the 2022 prototype2 without gain

Total of 40 analog pixels studied

Radiation tolerance studies in collaboration with **KEK** and **IHP** colleagues.
8 samples of prototype2 ASIC were irradiated in Japan up to $1 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$.



Radiation tolerance studies in collaboration with **KEK** and **IHP** colleagues.
8 samples of prototype2 ASIC were irradiated in Japan up to $1 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$.

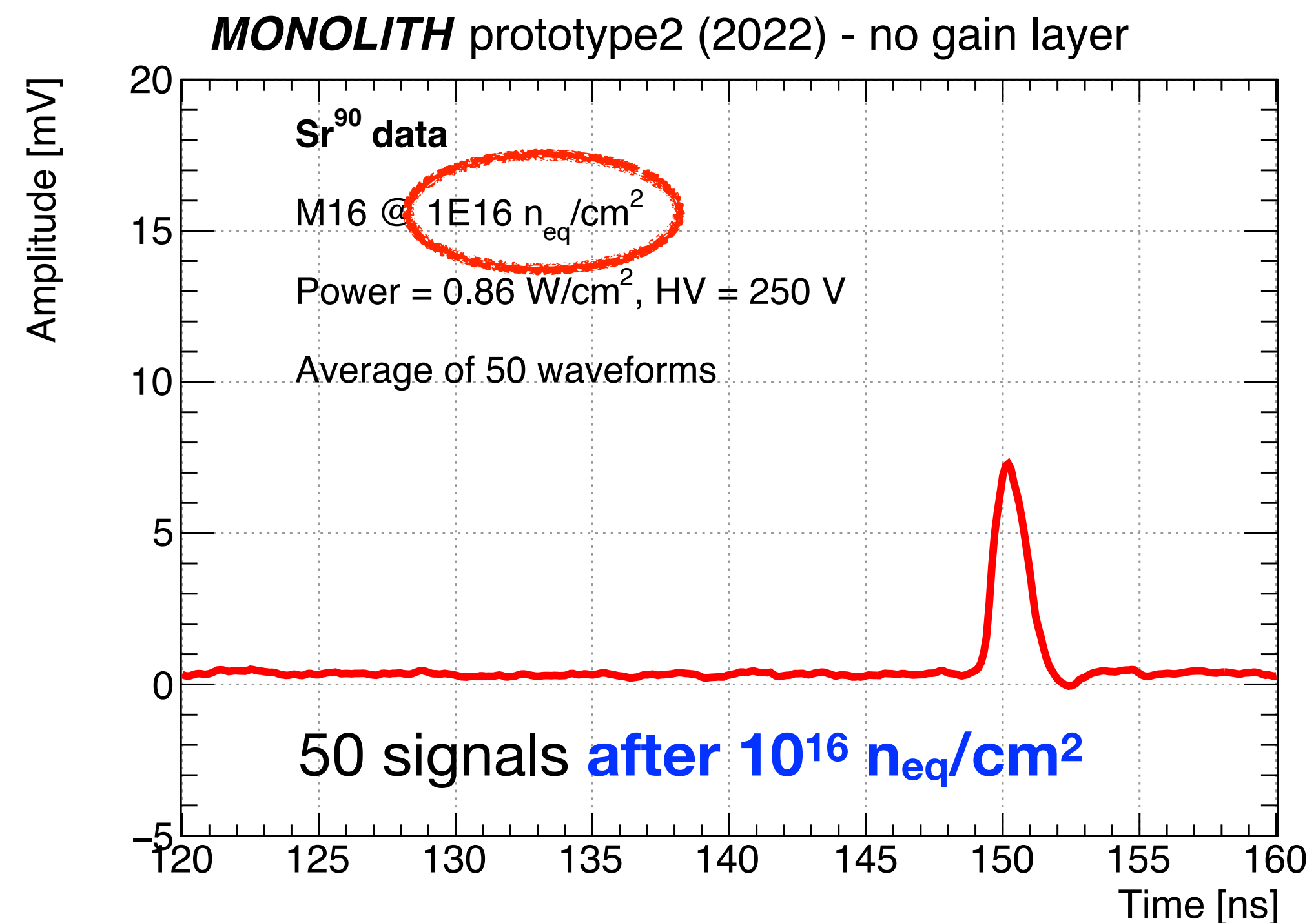
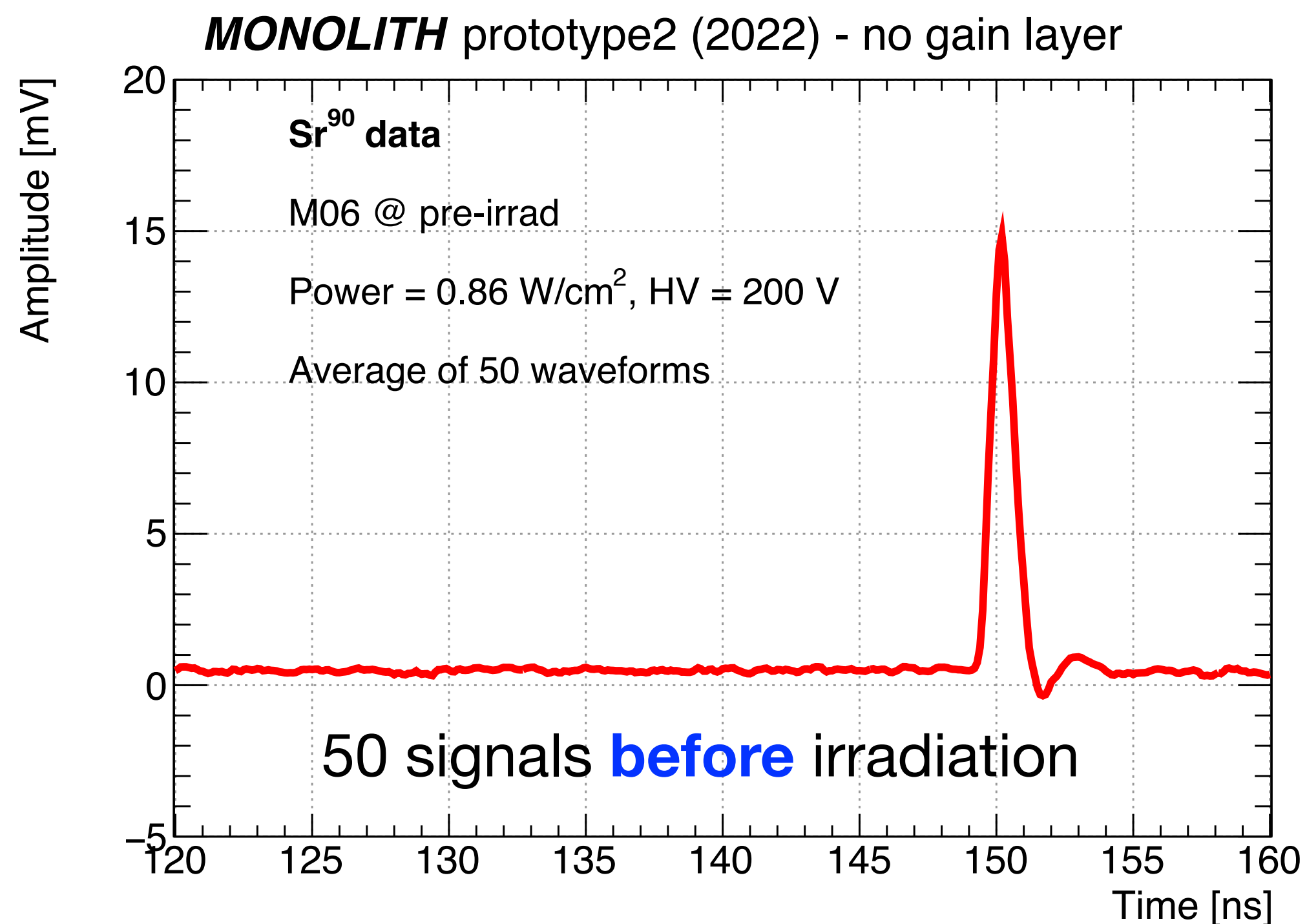
7 out of the 8 irradiated boards had
damaged voltage regulators:
bypassed with wire bonds

One board **not configurable** :
short on the digital logic. Not used

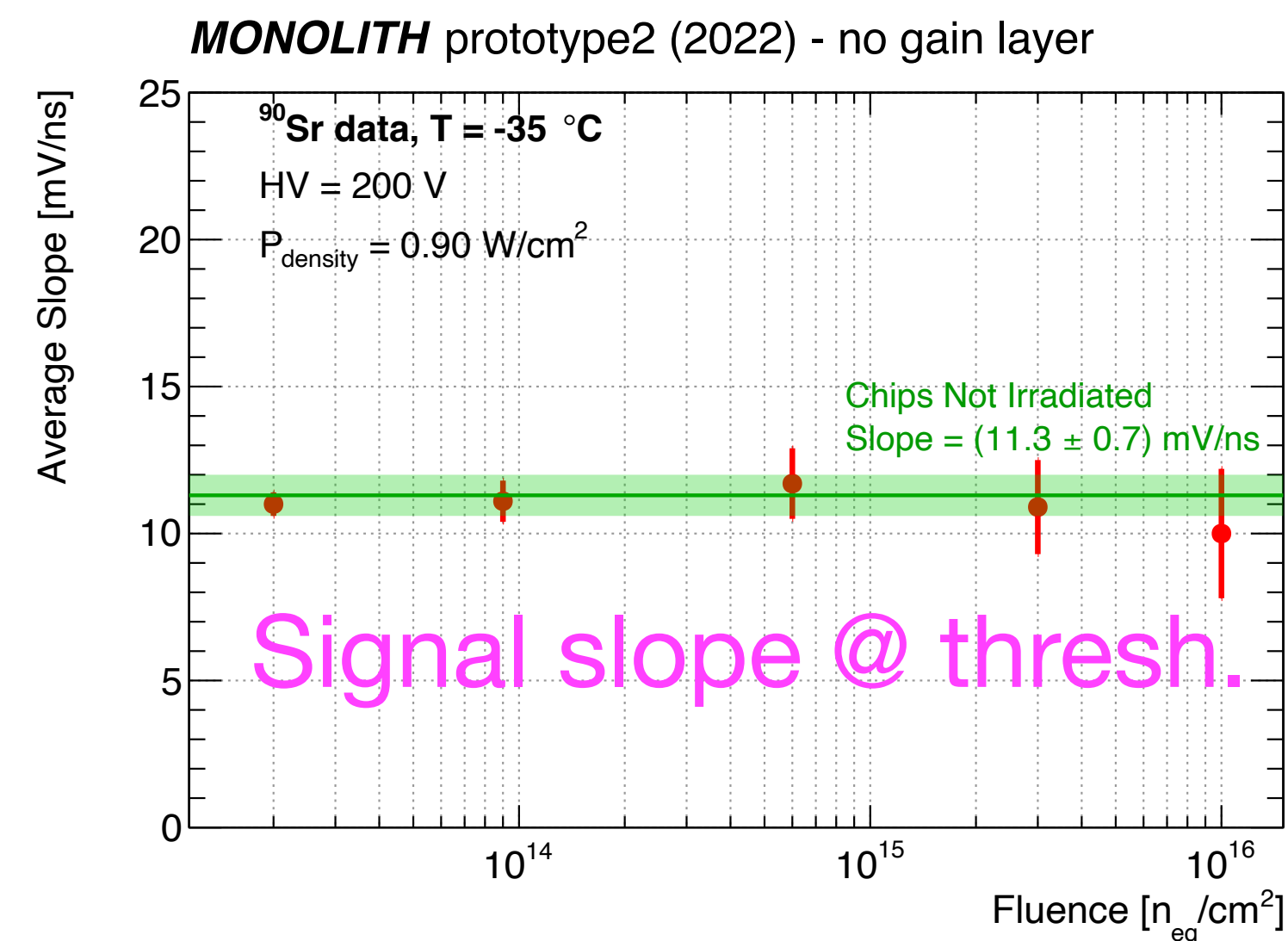
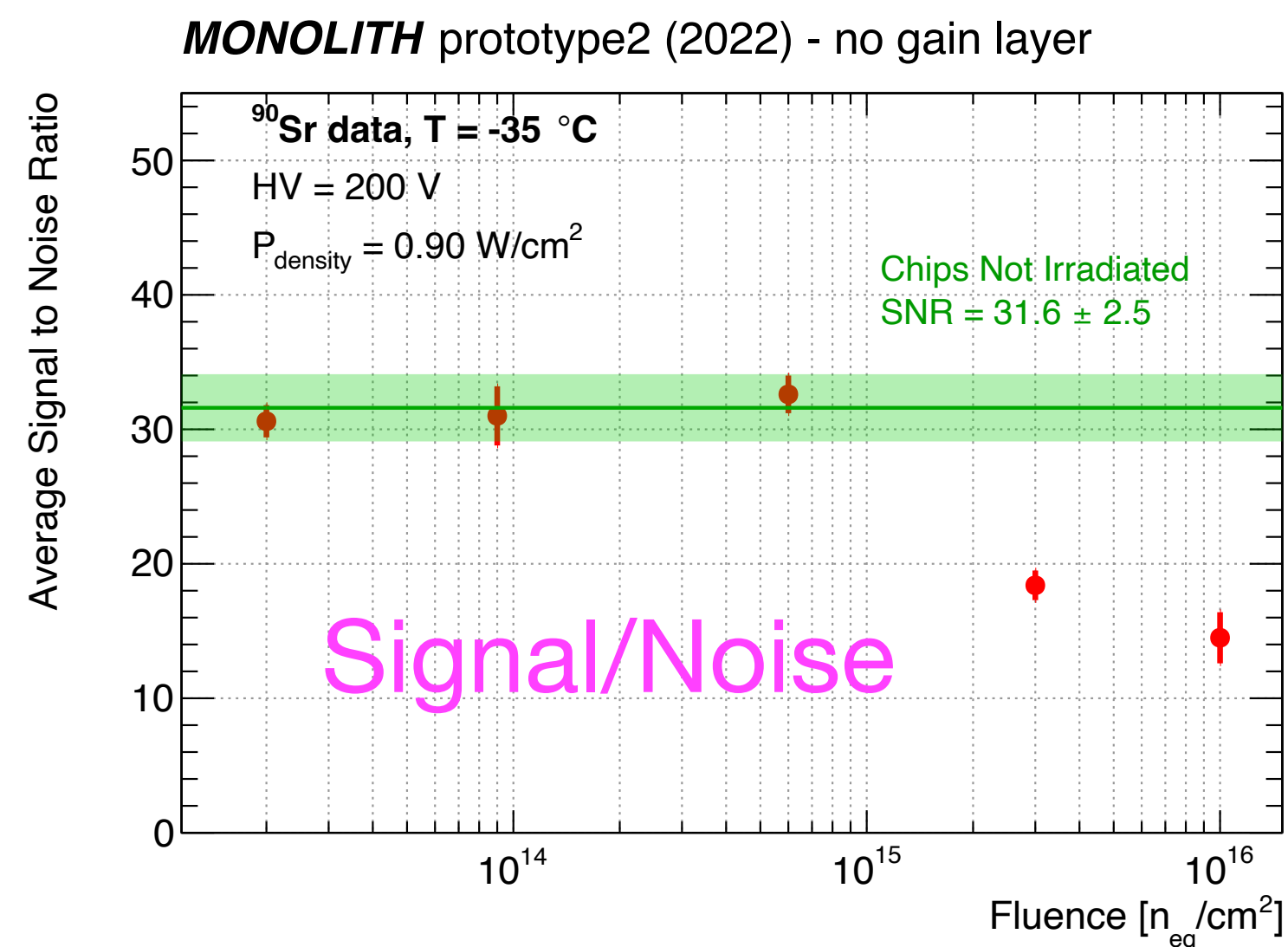
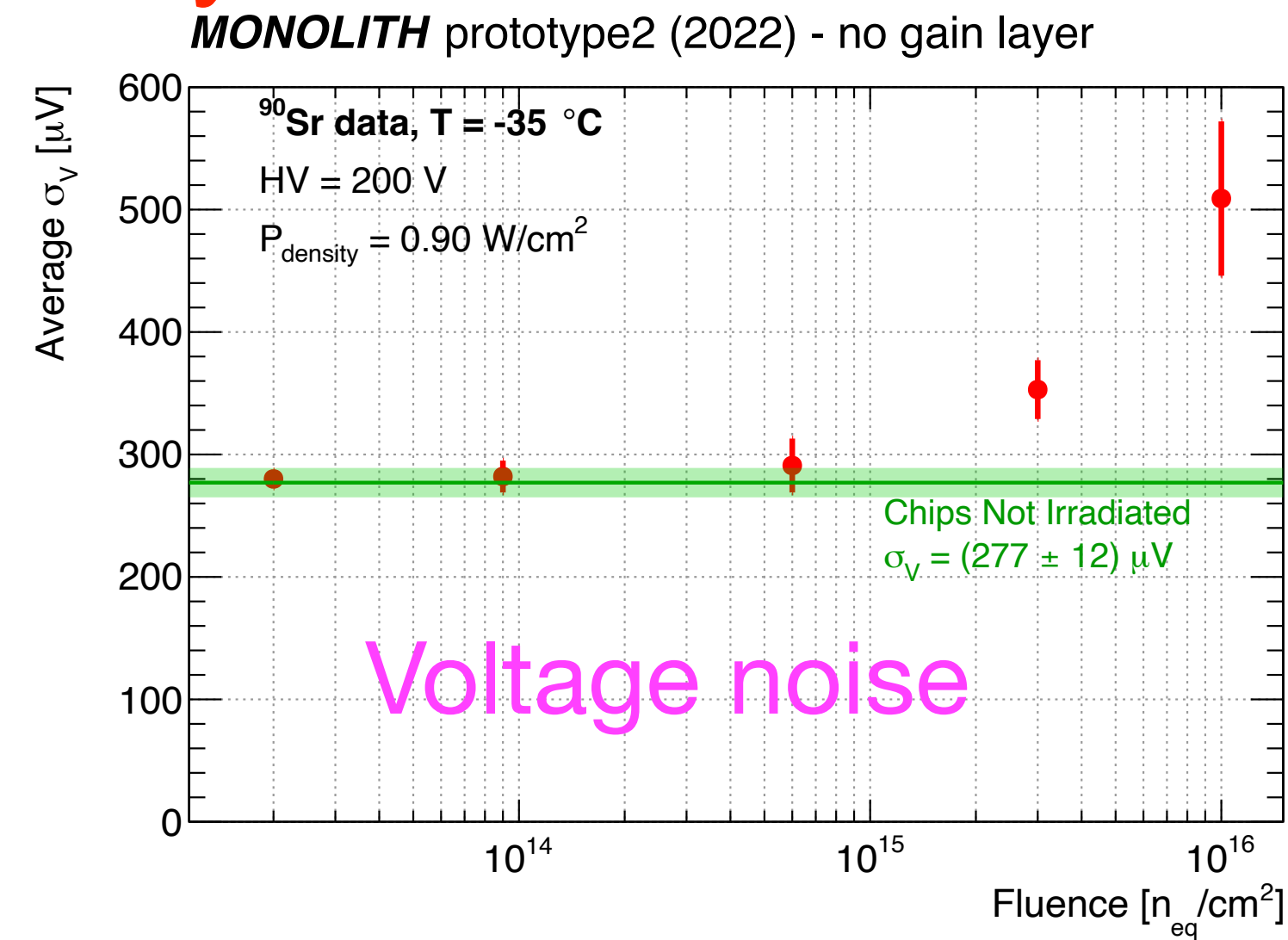
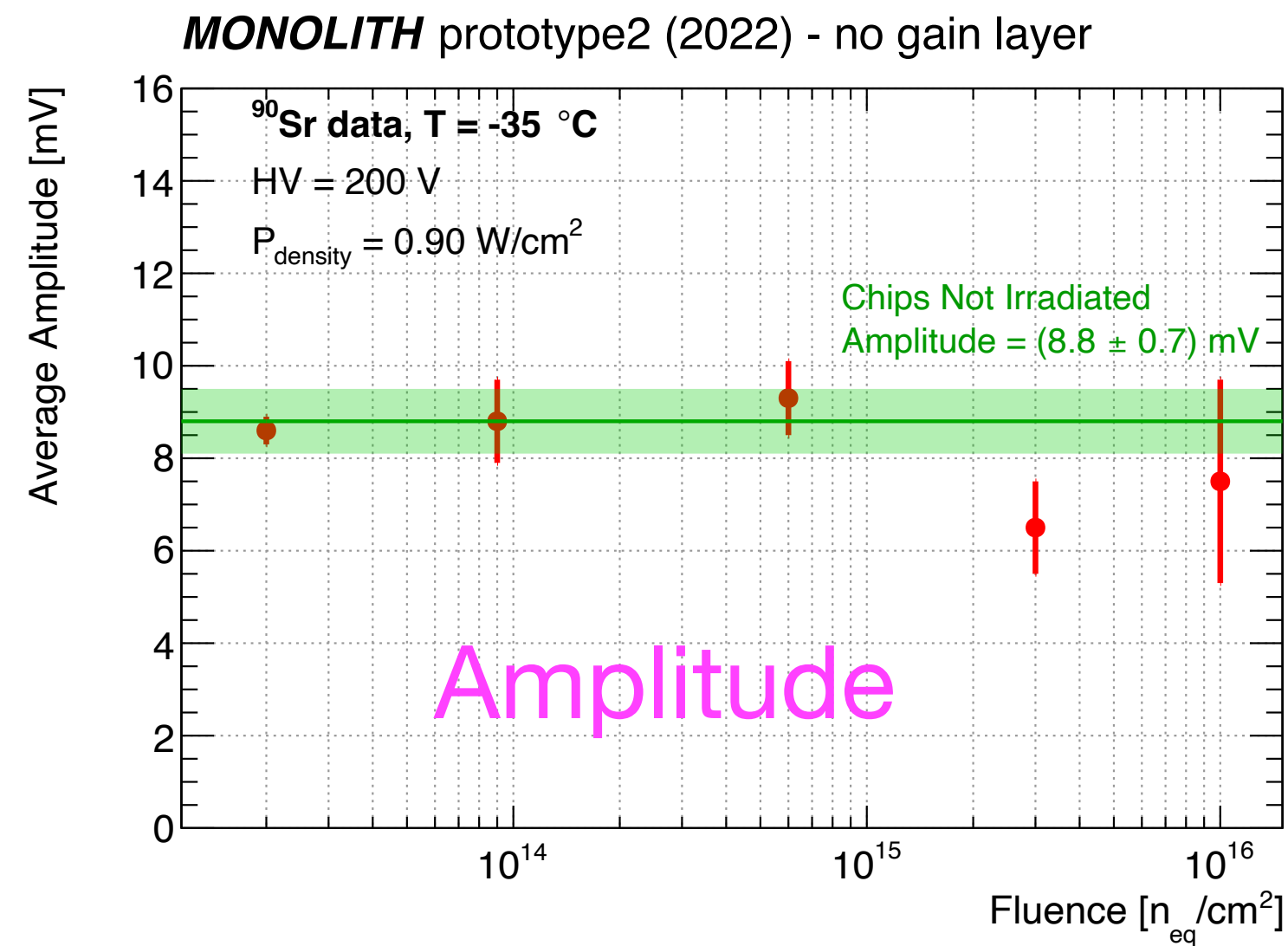
Three unirradiated boards.
(one is the **same of the CERN testbeam**,
results published in **JINST 18 (2023) P03047**)

Board Name	Fluence [1 MeV $\text{n}_{\text{eq}}/\text{cm}^2$]
M23	$2 \cdot 10^{13}$
M22	$9 \cdot 10^{13}$
M21	$6 \cdot 10^{14}$
M19	$6 \cdot 10^{14}$
M18	$3 \cdot 10^{15}$
M17	$3 \cdot 10^{15}$
M16	$1 \cdot 10^{16}$
M15	$1 \cdot 10^{16}$
M06	not irradiated – for comparison
M05	not irradiated – for comparison
M07	not irradiated – for comparison

Very good news:
even after $1 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$ the ASICs work !!!
although signals are clearly degraded



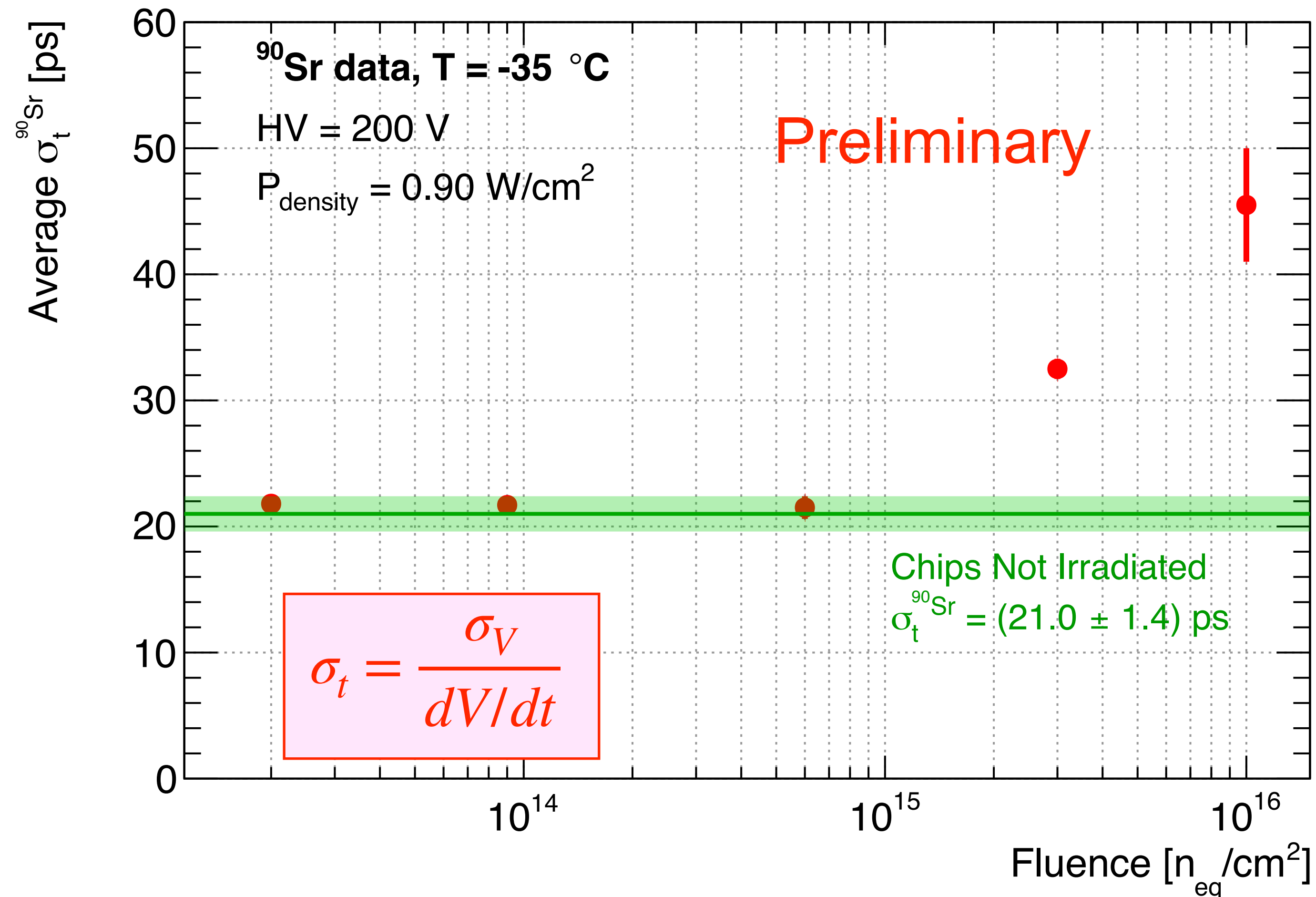
Preliminary



Characterisation with ⁹⁰Sr source
of boards irradiated
up to **10¹⁶ n_{eq}/cm²**

Averages of the 4 analog pixels
(HV = 200 V, T=-35°, 0.9 W/cm²)

MONOLITH prototype2 (2022) - no gain layer



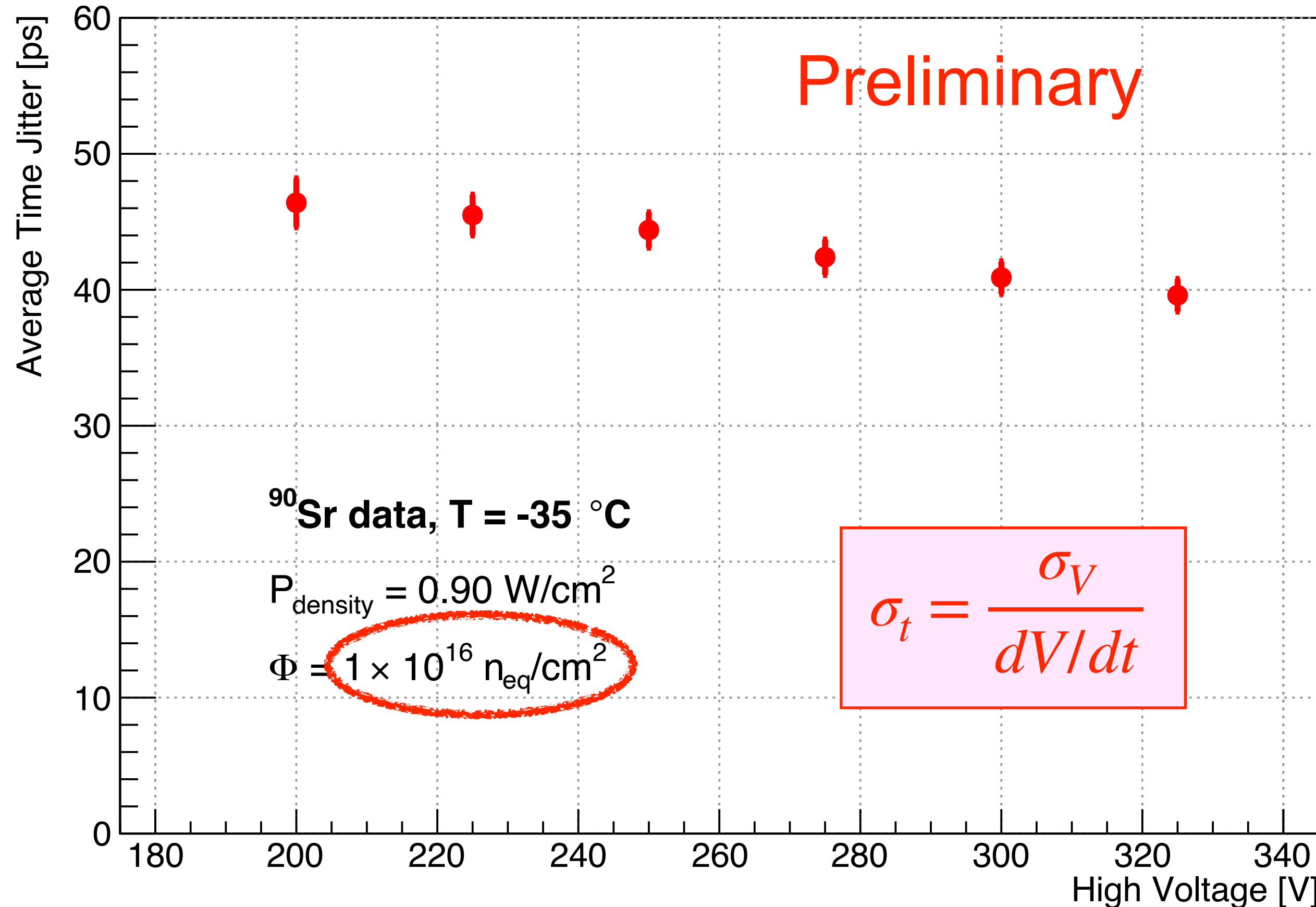
Excellent news from radiation tolerance studies:

The time jitter with ^{90}Sr increases
from 21ps (unirradiated)
to 46ps (at $10^{16}\text{ n}_{\text{eq}}/\text{cm}^2$)
 at **HV = 200V** and **0.9 W/cm²**

Total of **40 pixels studied** with **^{90}Sr** , at different proton fluence.
At a given proton fluence, pixel-to-pixel **time jitter variations within 20%**.
(quoted uncertainties on the averages are the standard deviations)

Fluence [$\text{n}_{\text{eq}}/\text{cm}^2$]	$\sigma_t^{90\text{Sr}}$ [ps]				Average $\sigma_t^{90\text{Sr}}$ [ps]
	pixel 1	pixel 2	pixel 3	pixel 4	
0	22.1	20.5	18.8	19.9	21.0 ± 1.4
	22.1	22.7	19.5	19.6	
	22.9	22.2	21.1	20.7	
2×10^{13}	21.4	22.2	21.2	22.4	21.8 ± 0.6
9×10^{13}	21.4	22.5	21.0	21.8	21.7 ± 0.6
6×10^{14}	21.5	22.4	20.2	20.9	21.5 ± 0.8
	20.7	22.3	22.6	21.3	
3×10^{15}	32.7	33.2	31.4	32.8	32.5 ± 0.8
1×10^{16}	43.3	50.9	44.0	47.5	45.5 ± 4.5
	49.7	53.0	36.2	40.0	

MONOLITH prototype2 (2022) - no gain layer



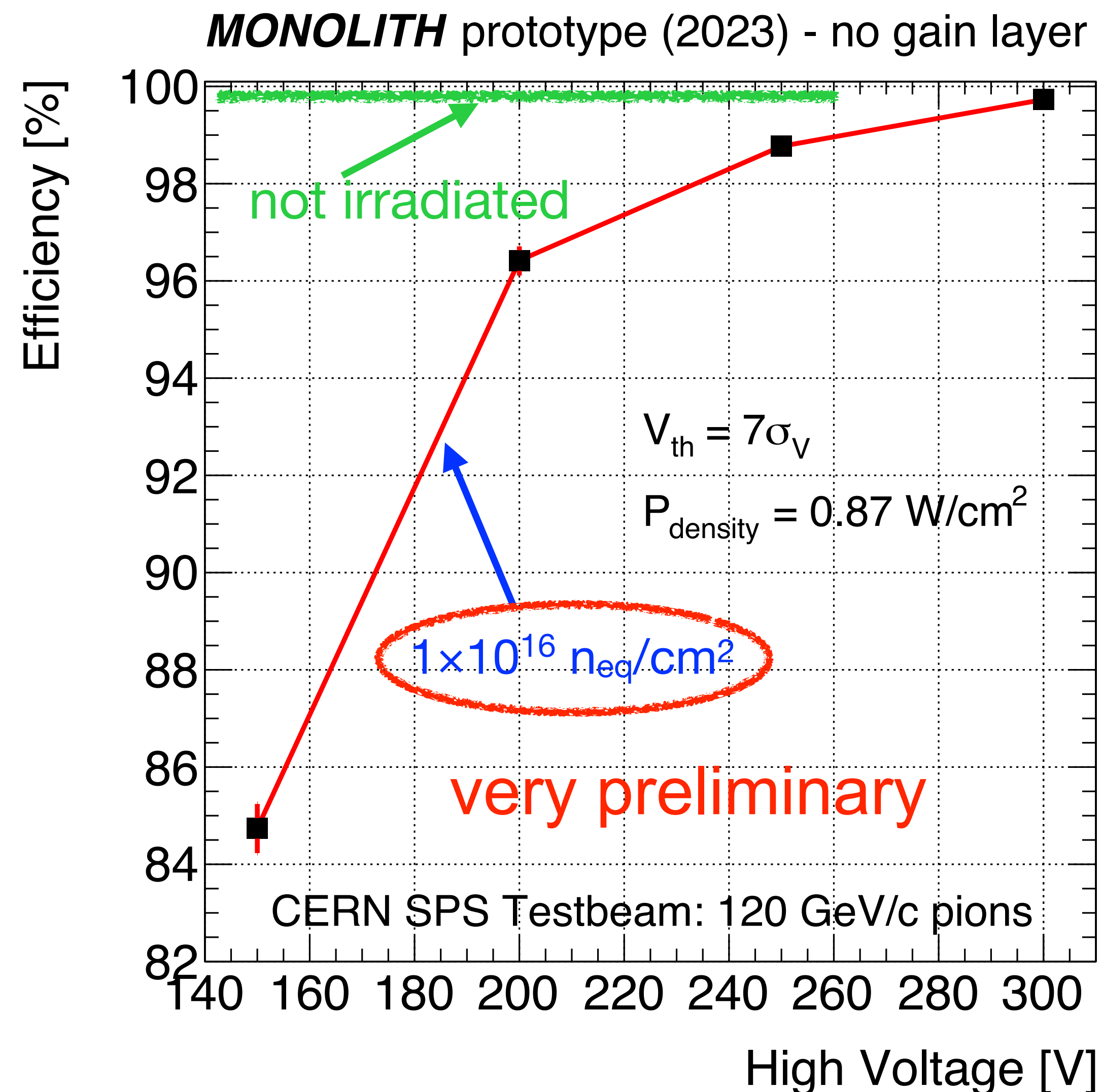
Rate measurements with ¹⁰⁹Cd source show that after 1 × 10¹⁶ n_{eq}/cm² the sensor is not fully depleted at HV = 200 V

At 0.9 W/cm² the time jitter with ⁹⁰Sr at Φ = 1 × 10¹⁶ n_{eq}/cm² decreases
from 46ps at HV = 200 V
to 40ps at HV = 325 V

Very preliminary

August 2023 testbeam at CERN SPS

Board irradiated $1 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$:
efficiency still $\gtrsim 99\%$
for $HV \gtrsim 250 \text{ V}$
at $0.9 \text{ W}/\text{cm}^2$

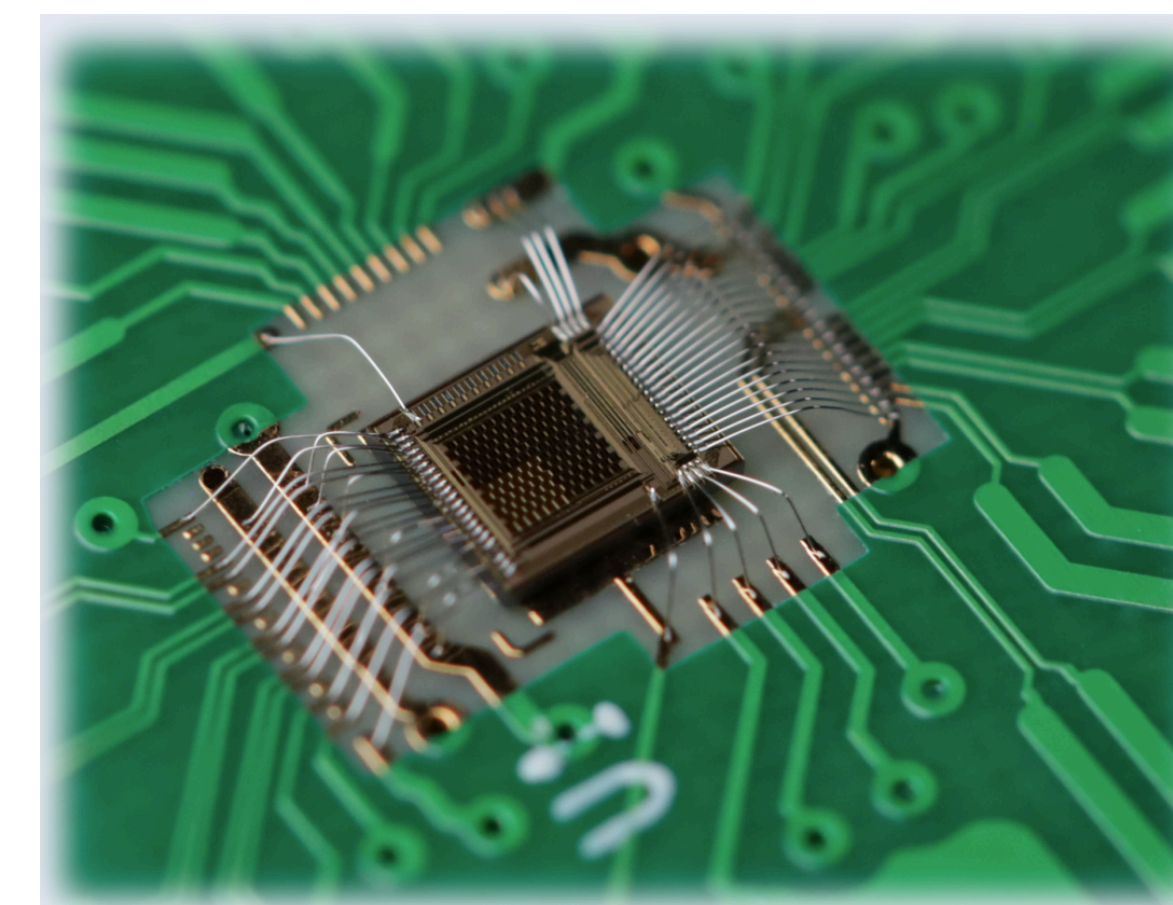


A monolithic prototype ASIC without gain produced in SiGe BiCMOS provided:

- ▶ **Efficiency of 99.8%** and **time resolution of 21 ps**
- ▶ **Laser** measurement: **down to 2.5 ps**.

After proton fluence of **10^{16} 1MeV n_{eq}/cm^2** :

- ▶ Increasing HV from 200 V to 325 V gives
Efficiency up to 99.7 % and **time resolution of 40 ps**



This performance was obtained **without gain layer**

SiGe BiCMOS seems to be a serious candidate for future 4D trackers (and much more)

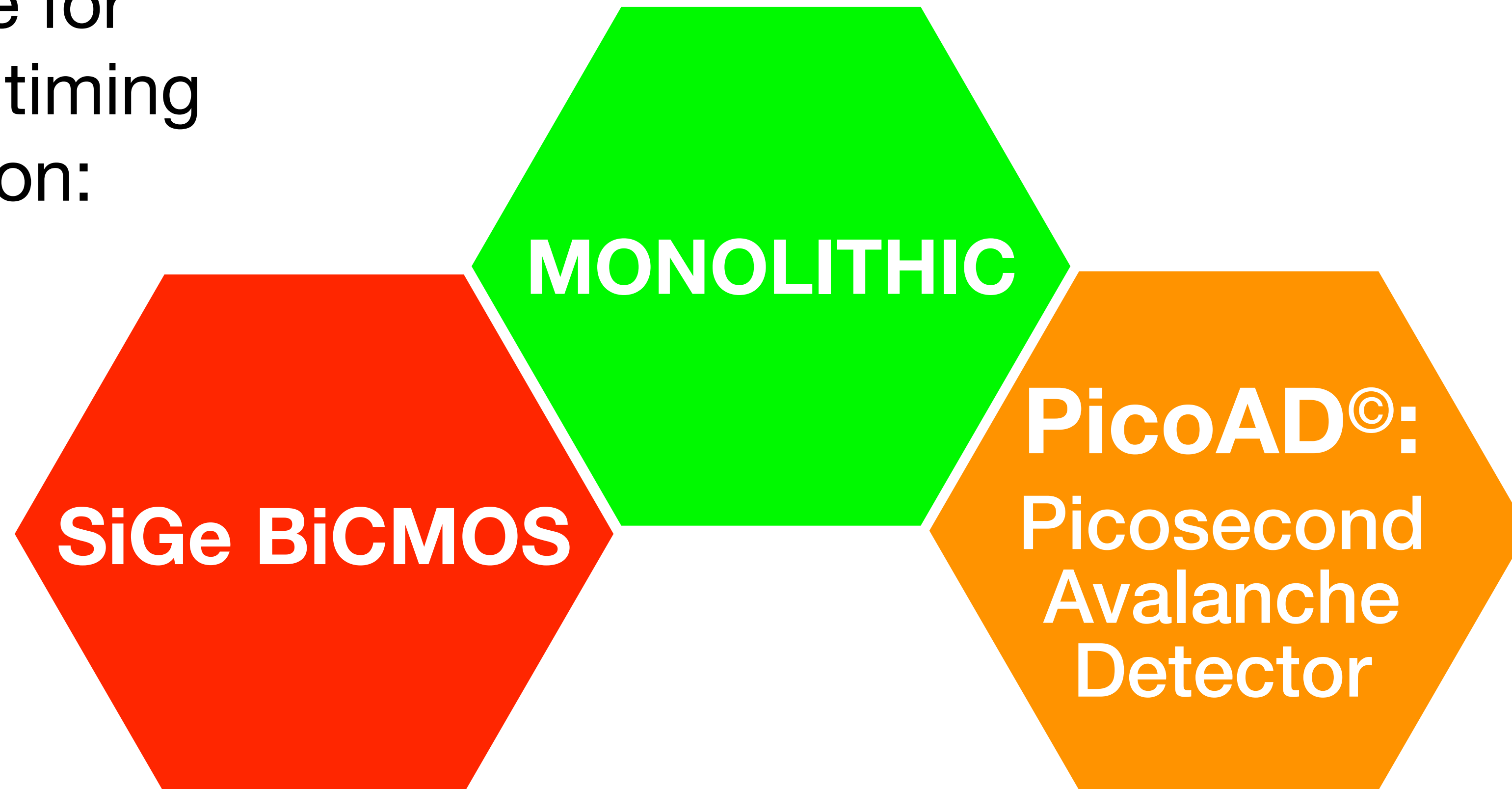
The **MONOLITH** Project



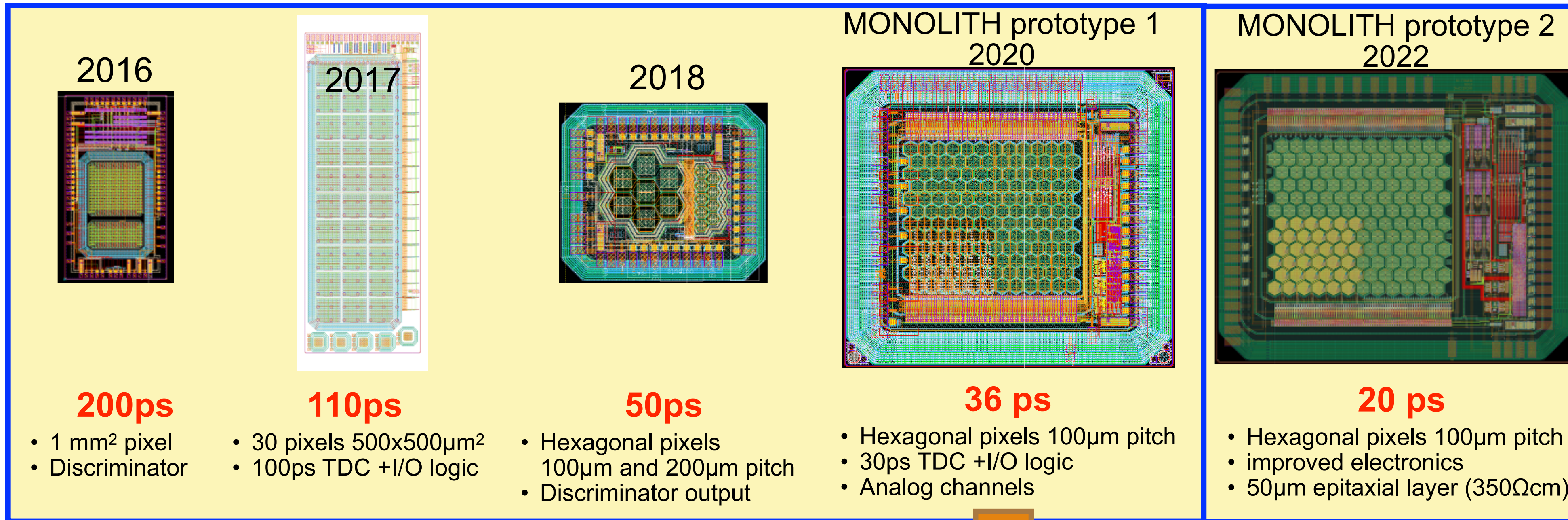
European Research Council
Established by the European Commission

Funded by the H2020 ERC Advanced grant 884447,
July 2020 - June 2025

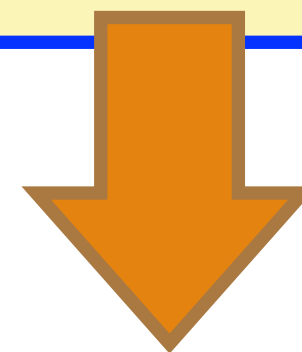
Our recipe for
picosecond timing
with silicon:



Monolithic prototypes with SiGe BiCMOS (IHP 130nm SG13G2) without internal gain layer



In 2022 : **proof-of-concept**
monolithic prototype
with internal gain layer
(using 2020 masks)



PicoAD
special wafers
produced internally by IHP
(not optimised yet)

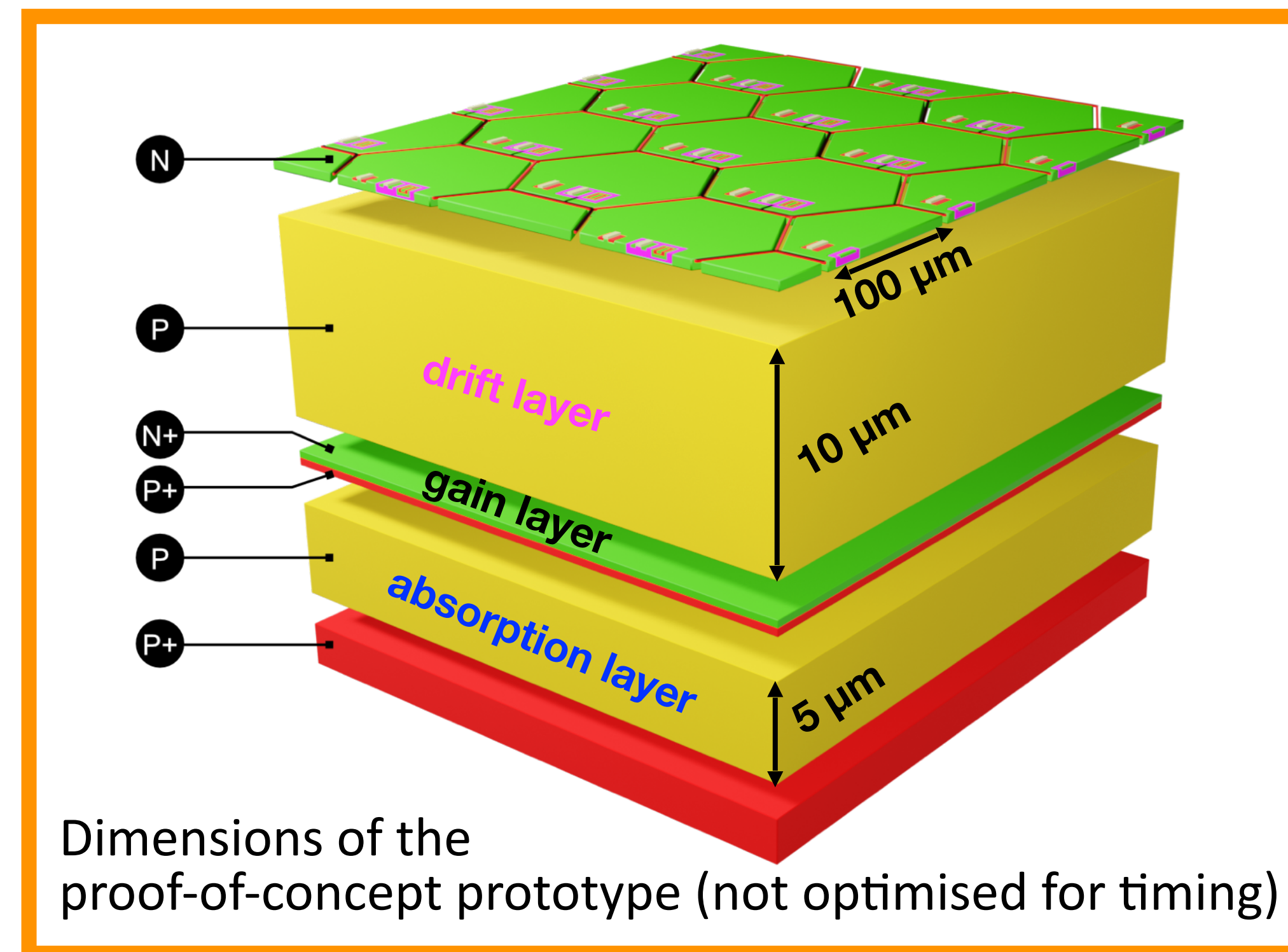
PicoAD:

Multi-Junction Picosecond-Avalanche Detector©

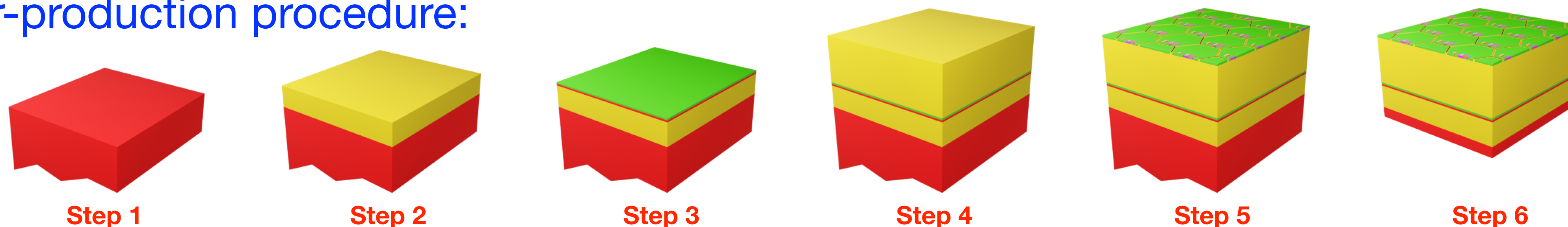
with continuous and deep gain layer:

- De-correlation from implant size/geometry
→ **high pixel granularity and full fill factor**
(high spatial resolution and efficiency)
- Only small fraction of charge gets amplified
→ **reduced charge-collection (Landau) noise**
(enhance timing resolution)

© G. Iacobucci, L. Paolozzi and P. Valerio. Multi-junction pico-avalanche detector;
European Patent EP3654376A1, US Patent US2021280734A1, Nov 2018



Wafer-production procedure:



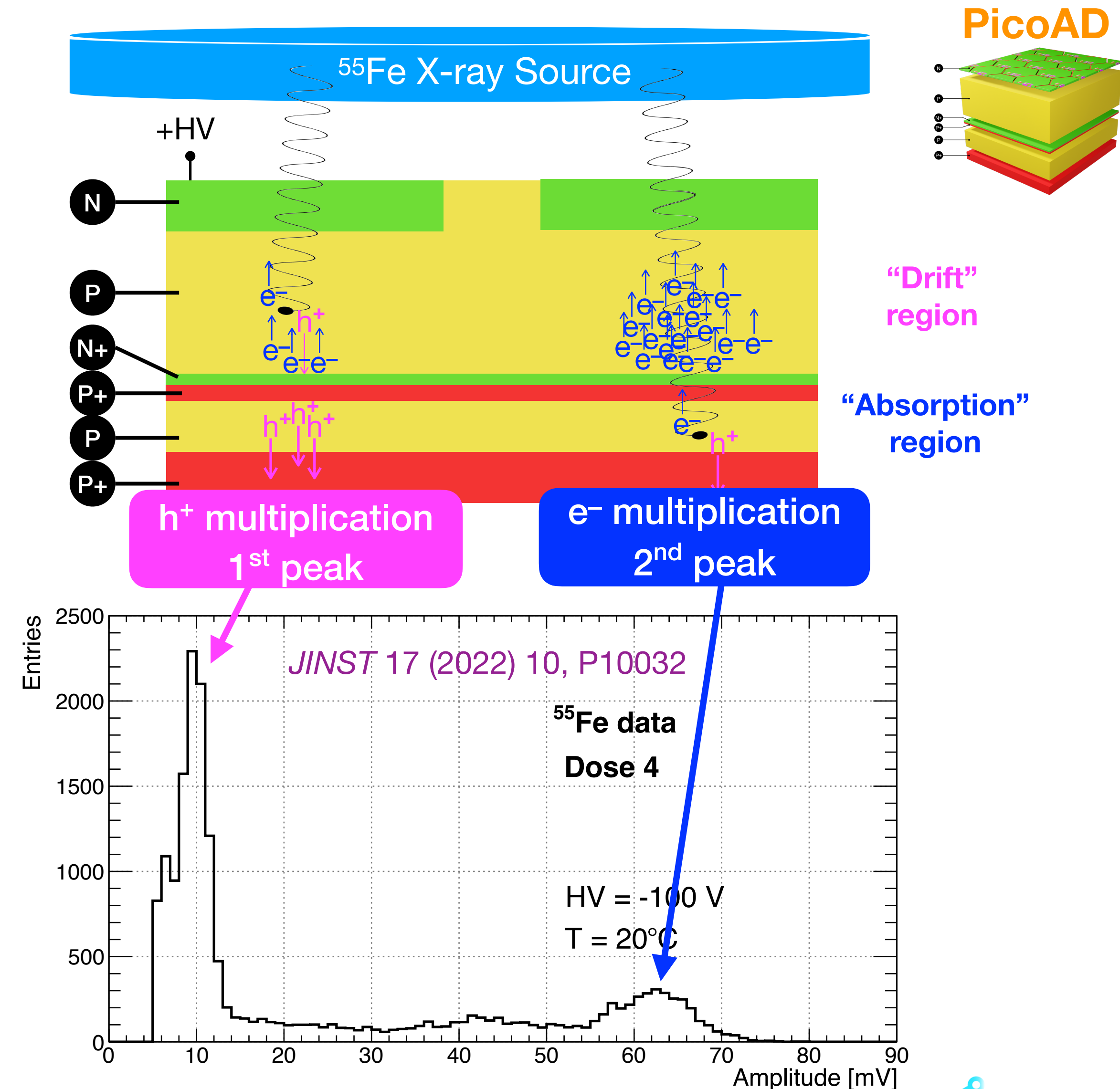
X-rays from ^{55}Fe radioactive source:

- ▶ mainly ~5.9 keV photons
- ▶ point-like charge deposition

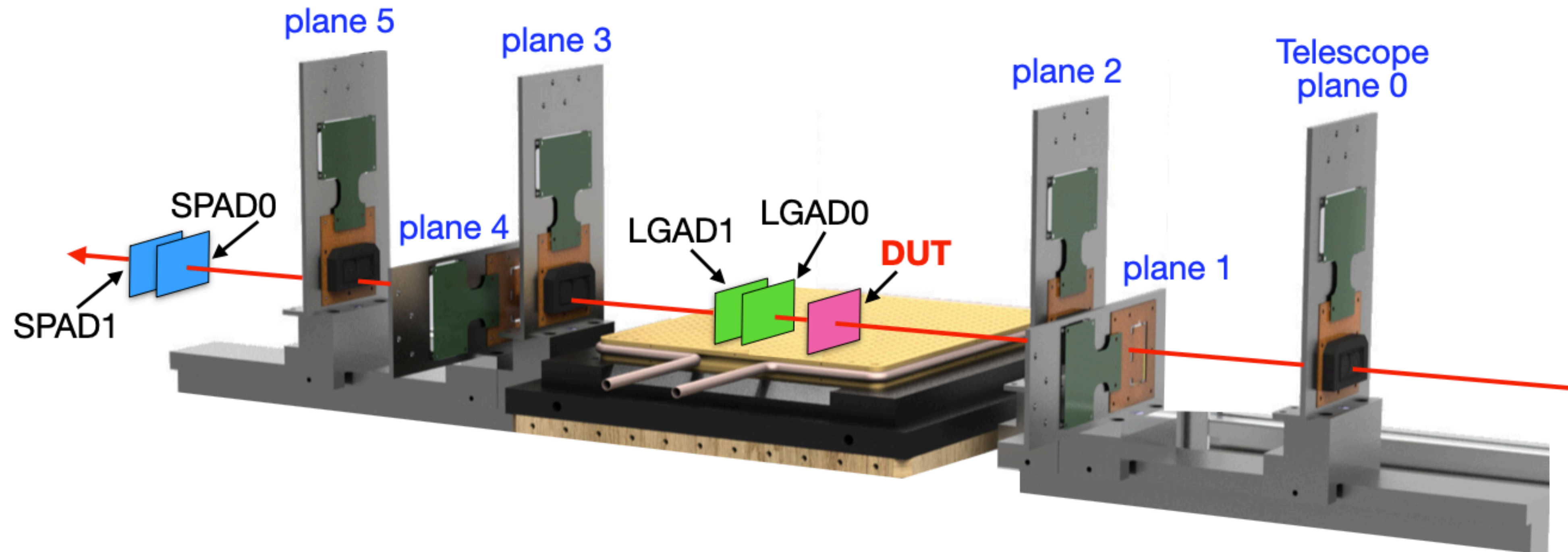
We found a **double-peak spectrum**

- ▶ photon absorbed in **drift region**
 - **holes** drift through gain layer & multiplied
 - **first peak** in the spectrum
- ▶ photon absorbed in **absorption region**
 - **electrons** through gain layer & multiplied
 - **second peak** in the spectrum

Gain measured: ~20 for ^{55}Fe
(corresponding to ~60 for a m.i.p.)

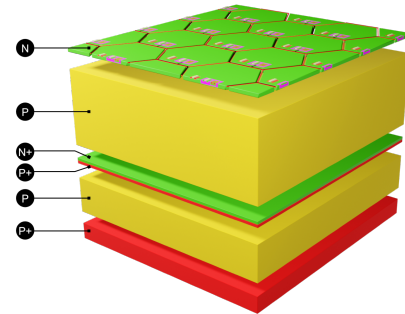


CERN SPS Testbeam with 180 GeV/c pions to measure **efficiency** and **time resolution**



UNIGE FE-I4 telescope to provide spatial information ($\sigma_{x,y} \approx 10 \mu\text{m}$)

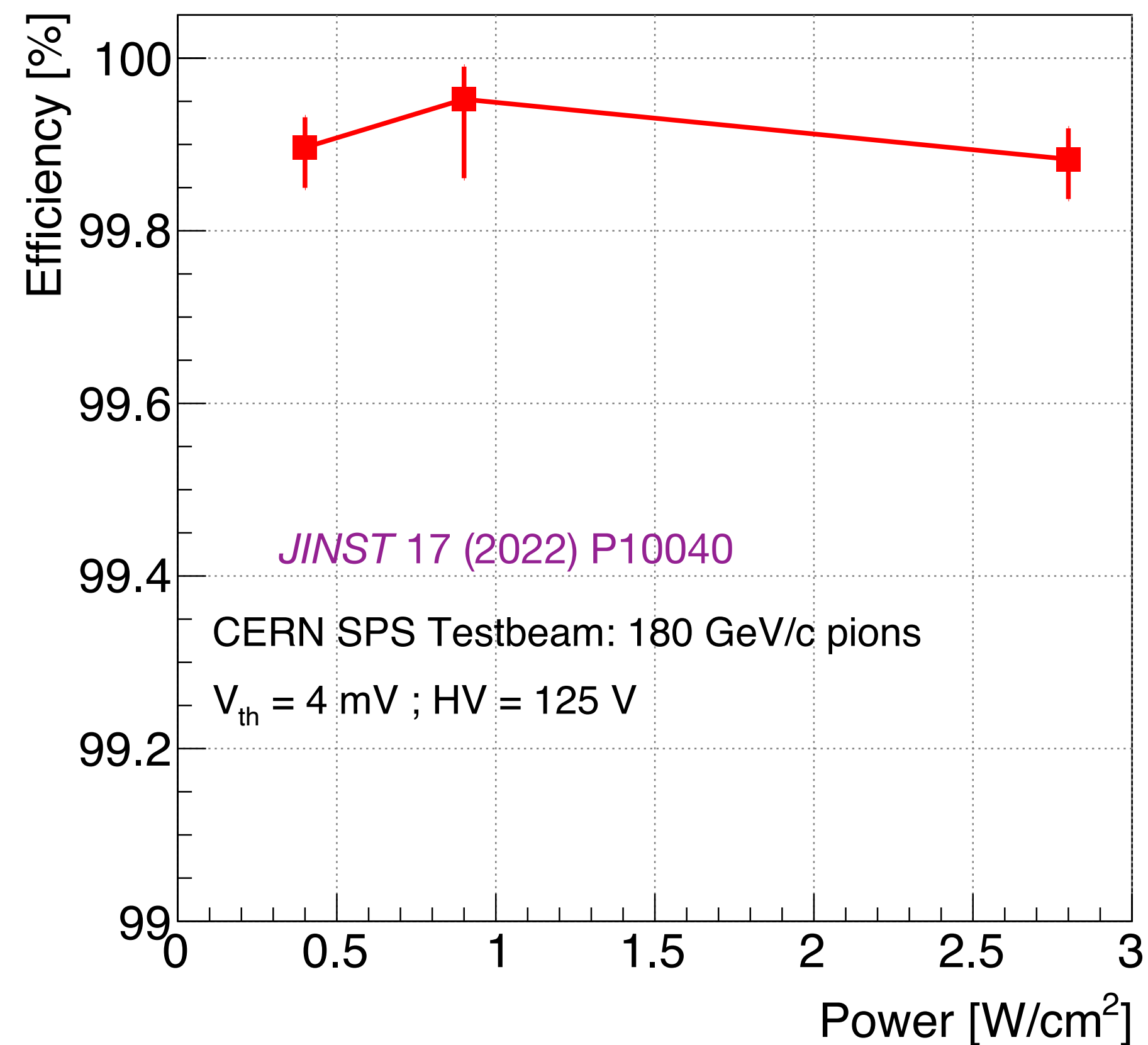
Two LGADs ($\sigma_t \approx 35 \text{ ps}$) to provide the timing reference (and **two SPADs** with $\sigma_t \approx 20 \text{ ps}$)



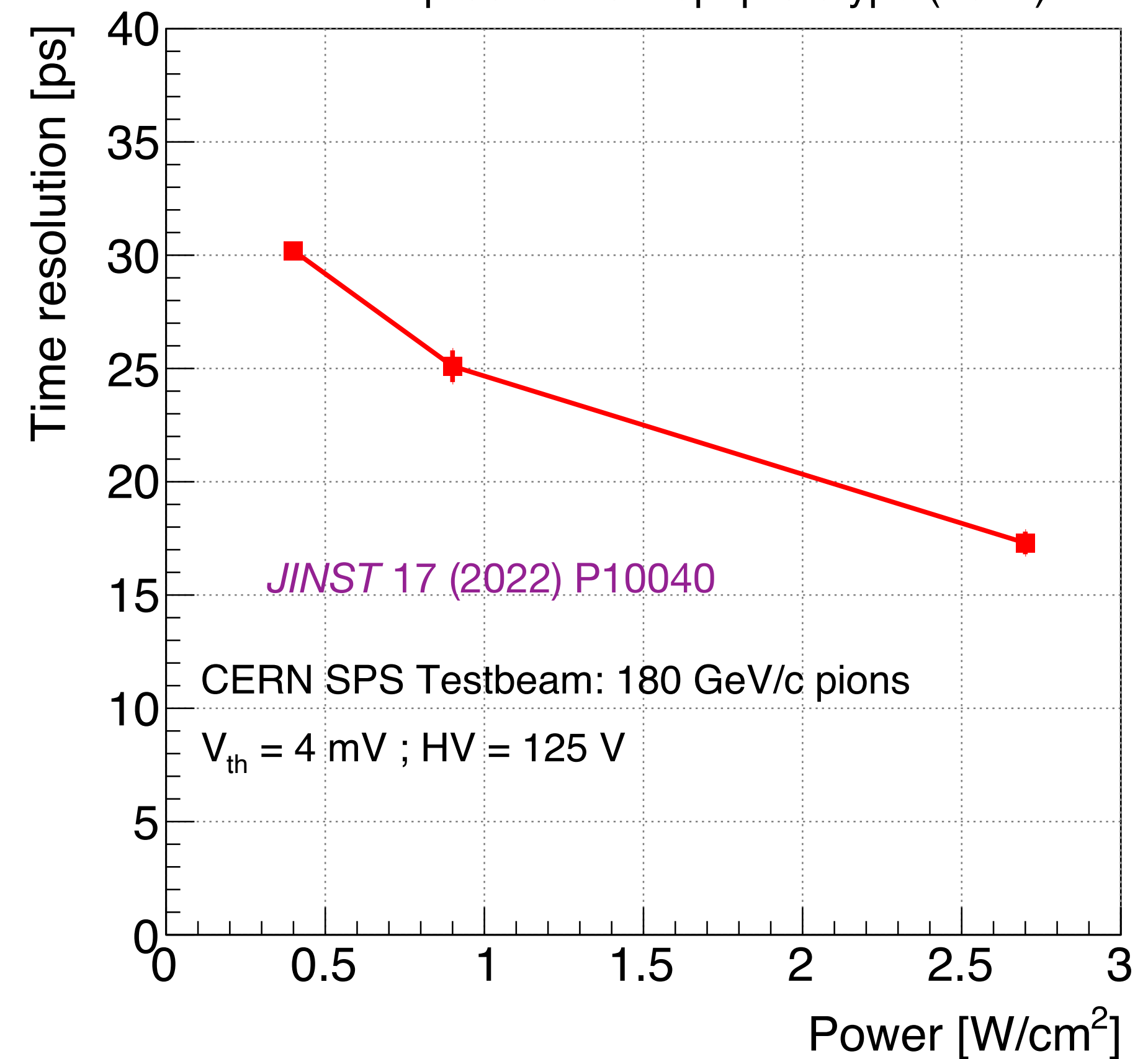
99.9% for all power consumptions

17 ps at 2.7 W/cm²
30 ps at 0.4 W/cm²

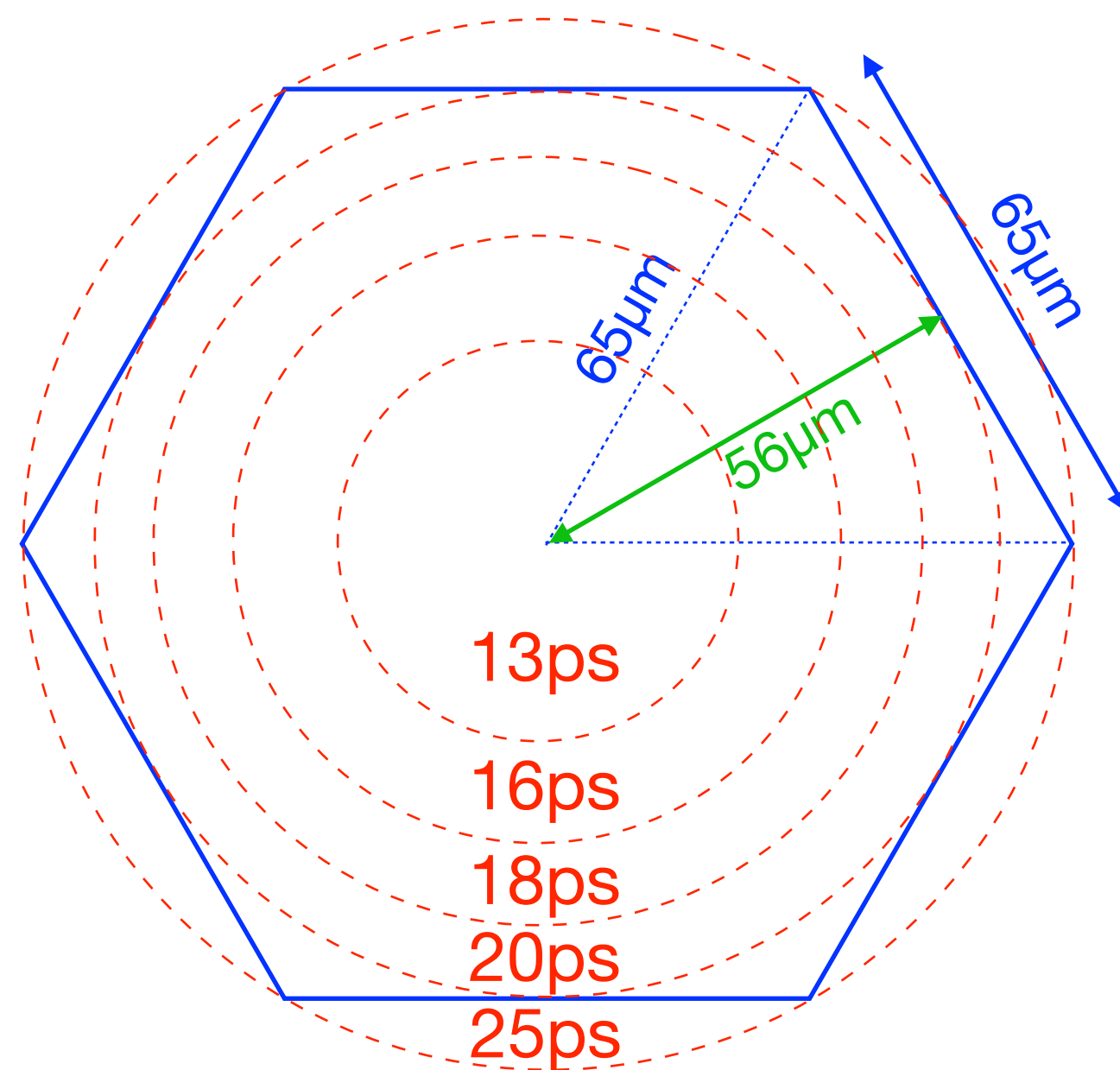
PicoAD proof-of-concept prototype (2022)



PicoAD proof-of-concept prototype (2022)

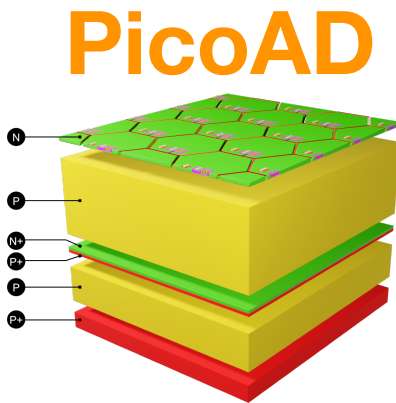
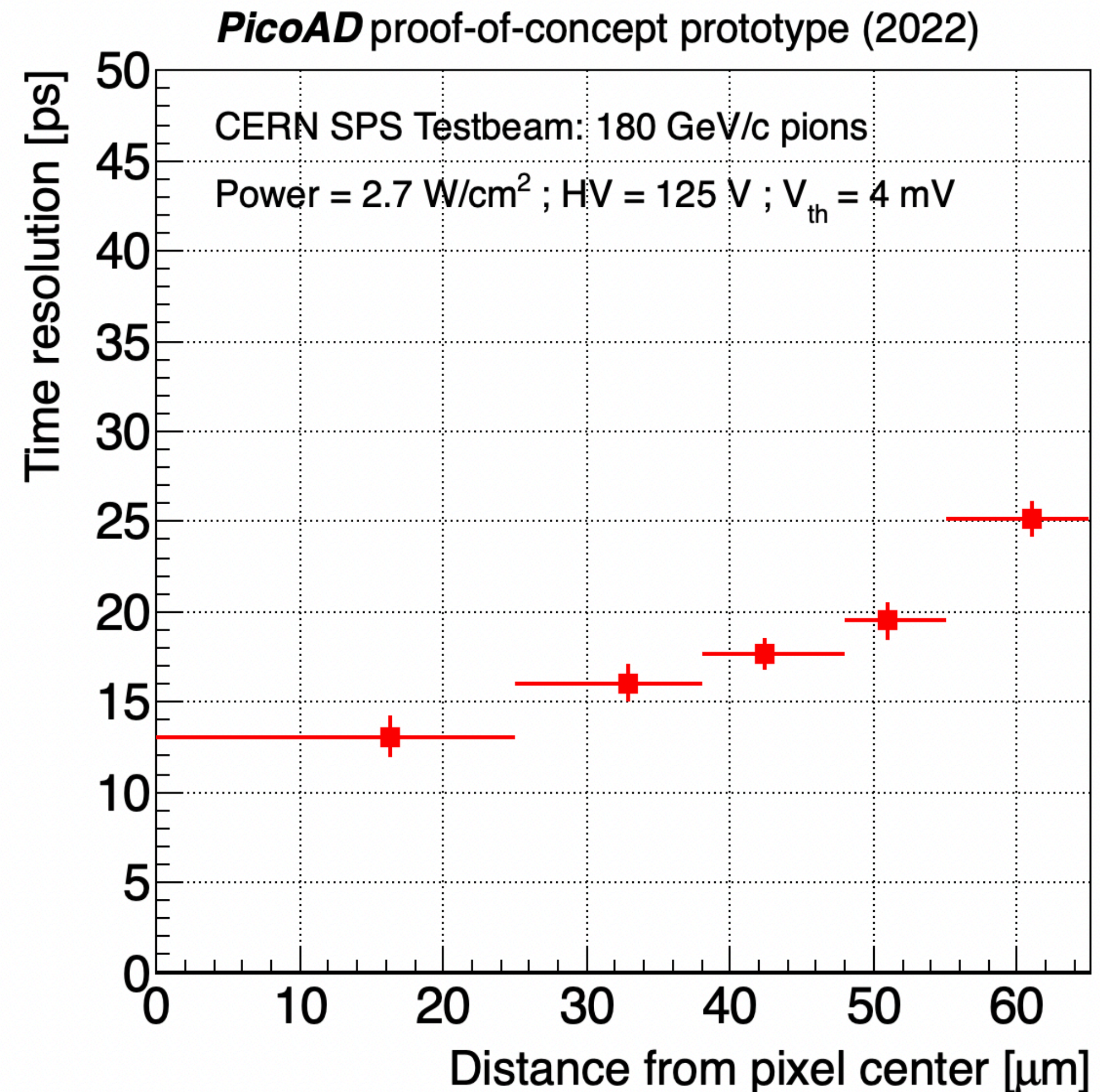


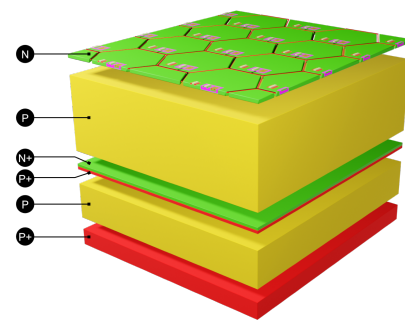
Pixel surface divided in 5 radial areas:



Time resolutions: **13 ps** at the pixel center
25 ps at the pixel edge

To be improved in future prototypes.





The **PicoAD[©] sensor works** (*JINST 17 (2022) 10 P10032 ; JINST 17 (2022) 17 P10040*)

Testbeam of the monolithic **proof-of-concept** ASIC provided:

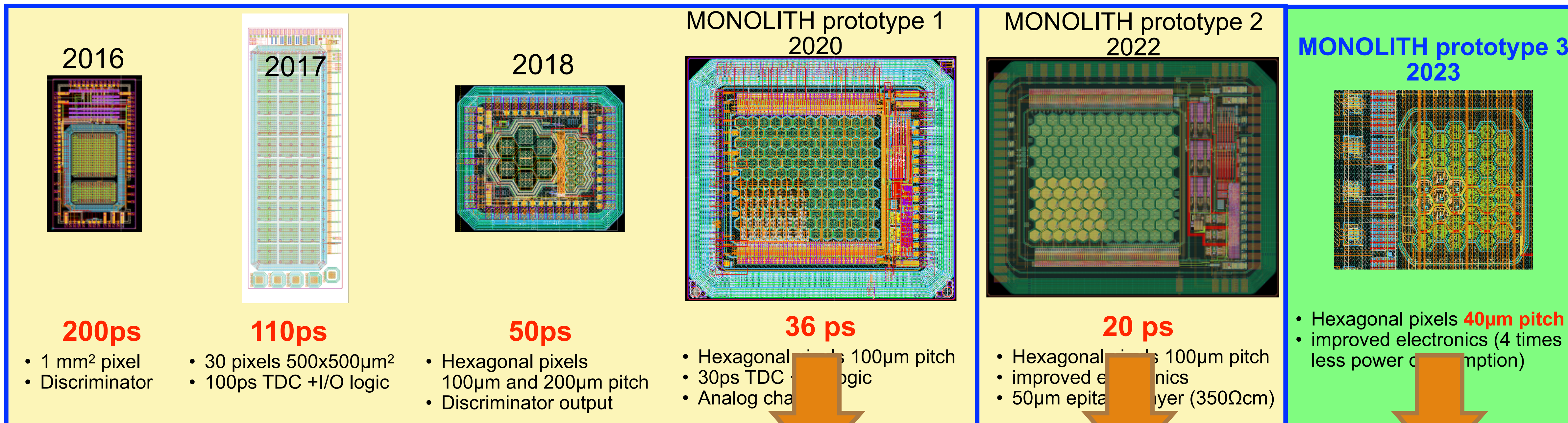
- ▶ **Efficiency = 99.9 %** including inter-pixel regions
- ▶ **Time resolution $\sigma_t = (17.3 \pm 0.4)$ ps**
13 ps at center and **25 ps** at pixel edge
(although sensor not yet optimized for timing)

New **PicoAD** prototypes optimised for timing back from foundry in **October 2023**

Deliverable of MONOLITH ERC project:

- ▶ Full-reticle monolithic ASIC in **Summer 2025** with 50 μ m pitch and 10ps timing

Monolithic prototypes with SiGe BiCMOS (without internal gain layer)



Monolithic prototypes
with internal gain layer:

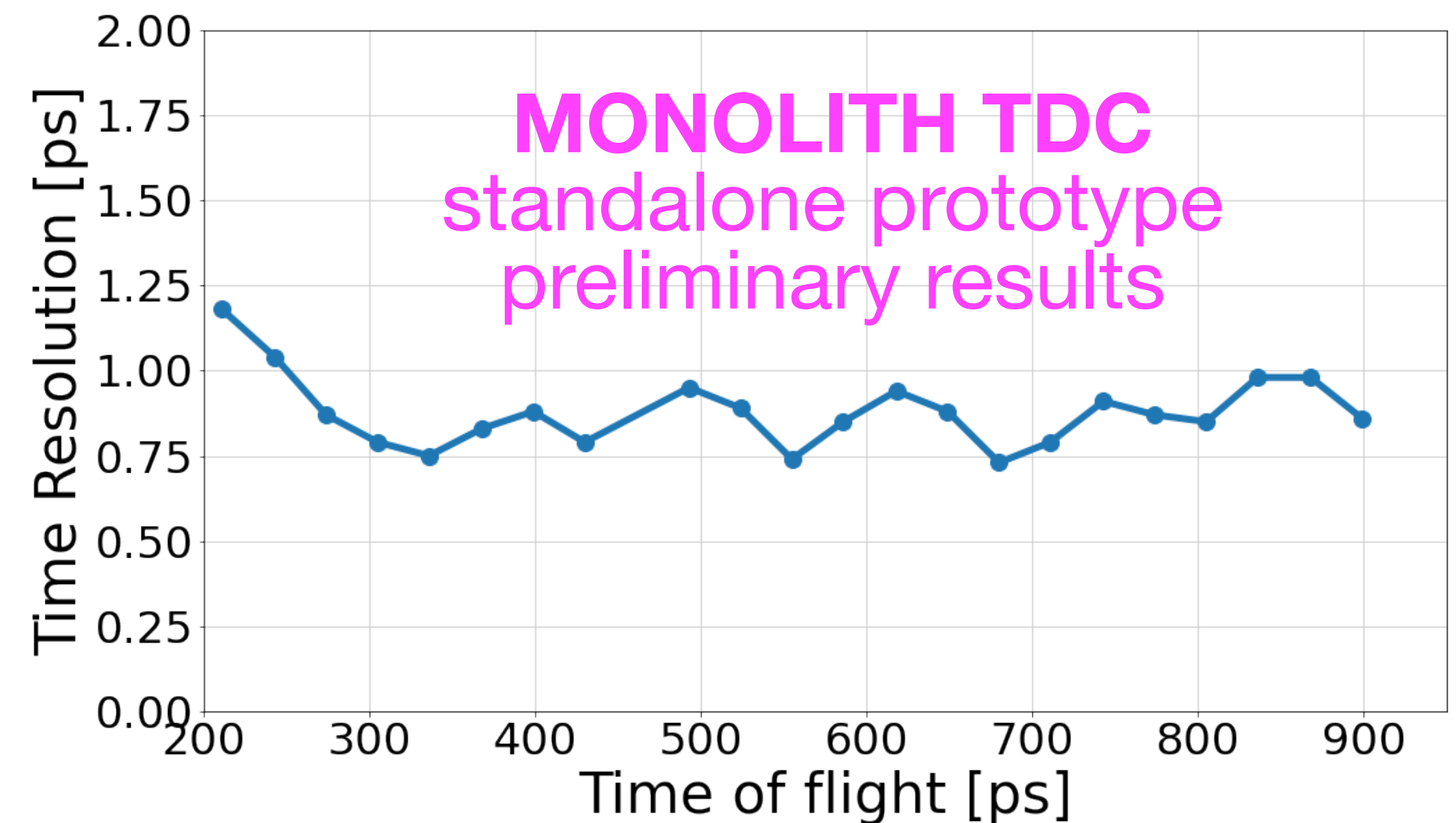
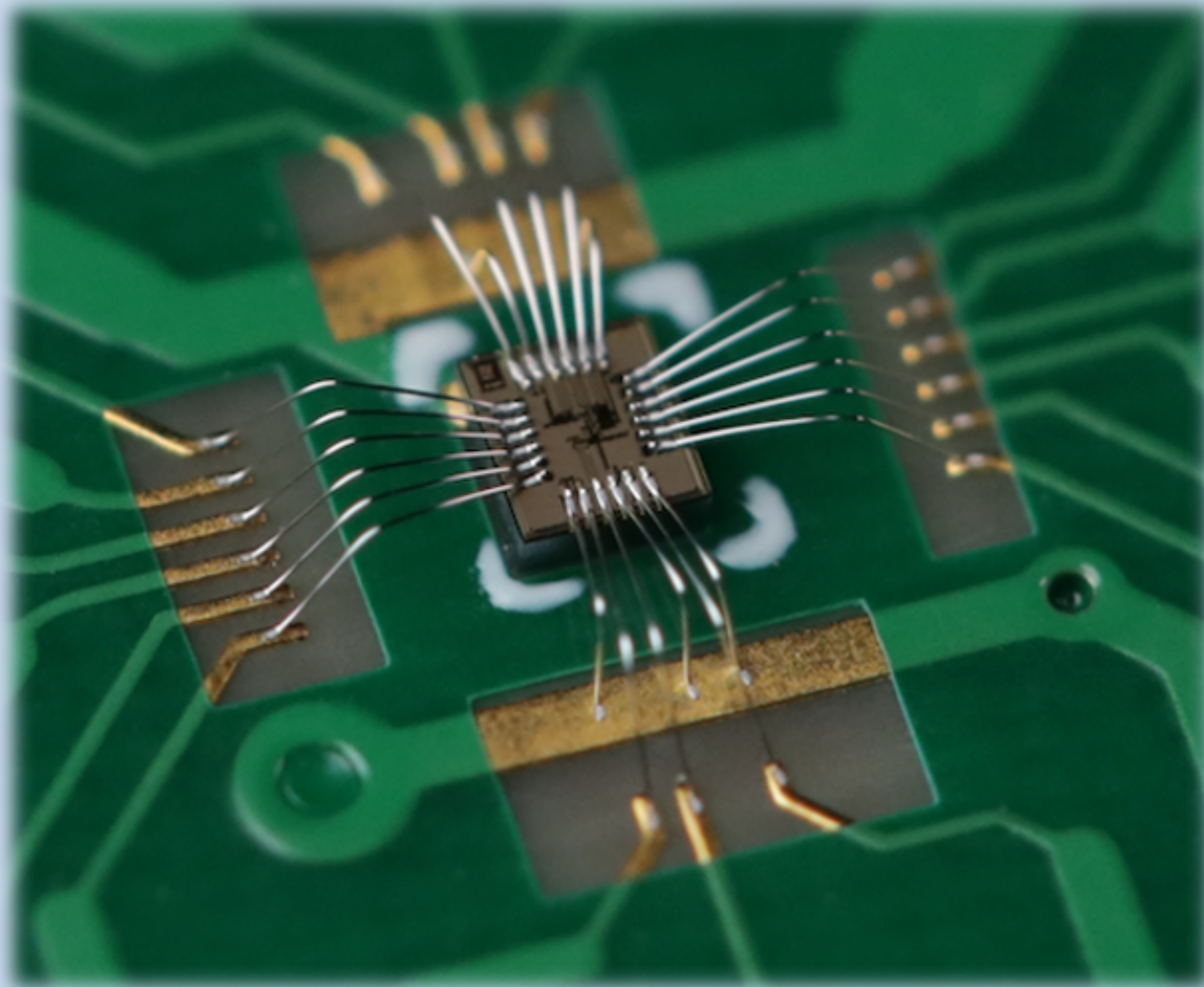
PicoAD version
(proof-of-concept)
17 ps

PicoAD version
in production
(back: **Oct. 2023**)

PicoAD version
expected
Summer 2024

We are developing a sub-picosecond TDC based on a novel design (our patent[©] & more):

© R. Cardarelli, L. Paolozzi, P. Valerio and G. Iacobucci, European Patent Application /
Filing - UGKP-P-001-EP, Europe Patent EP 18181123.3. 2 July 2018.



It was integrated in MONOLITH 2022 prototype2 ASIC